Application Report
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Texas Instruments GTLP Frequently Asked Questions

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ABSTRACT

Using a question-and-answer format, advantages of TI's GTLP devices, particularly for backplane applications, are presented, as well as differences between GTLP and GTL/LVDS devices. Applicable topics include data throughput rates, synchronous clocks, price and alternative sources, bus transceivers, live insertion, power consumption, backplane termination, voltage translation, IBIS and HSPICE models, and sample availability.

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Introduction

This information on GTLP and backplane design is presented in the frequently asked-question (FAQ) format. The GTLP FAQs allow the novice backplane user to learn more about parallel backplanes and allows the experienced backplane user to better design-in and use the higher performance of GTLP devices. Any questions not adequately addressed or applications you want highlighted can be sent to GTLP@list.ti.com for action and possible future insertion into the FAQs.

1 What is a backplane?

A backplane is a physical and electrical system bus that interconnects several printed circuit boards though a series of connectors. These buses can vary by the number of layers and traces and by electrical architecture. Generally, backplanes are passive, particularly in the telecom market, in which reliability concerns force designers to minimize the number of backplane components. Backplane transceivers/buffers drive data onto and receive data directed to PC boards located along the backplane.

2 What is a backplane protocol?

The protocol decides the electrical, logical, and mechanical characteristics of a backplane. In addition to the standard protocols, many backplane designers prefer to employ proprietary protocols and architectures. Some of the more popular standard protocols are BLT, MBLT, 2eVME, and 2eSST on VME64x backplanes, PCI, cPCI, PMC, ISA, Multibus, PC/104, and PC/104+. Of these, VME, PCI and cPCI, collectively, dominate the market. cPCI combines the robust, rugged VME backplane physical configurations with the electrical performance of the PCI backplanes.

3 Should I use a parallel or serial architecture?

Part of choosing a protocol is deciding which type of backplane architecture is suited best to your application. You must choose between parallel and serial architectures, or a combination of both, and select point-to-point, multidrop, or multipoint data-distribution methods. Parallel systems require less protocol overhead, which is useful when sending status or control bits over short distances. Serial implementations offer board saving through the reduction in the number of board traces (if SERDES devices are used) and supply higher data throughput over greater distances.

4 If I use a parallel single-ended backplane, why do I need to use backplane-optimized transceivers and not just typical LVT or FCT devices?

The physics involved with a distributed-capacitance load limits the maximum frequency, unless the device is optimized with slower edge rates that ring less in these environments. FCT or LVT can offer only up to about 25 MHz, and, even then, signal integrity might be poor. The new VME and GTLP families are optimized with slower edge rates and provide much better signal integrity in a backplane environment. VME devices can operate up to about 40 MHz and are compatible with existing TTL/LVTTL backplane logic. GTLP is a derivative of GTL, and can operate at up to 175 MHz.

5 What is VME?

VME is short for VERSA bus architecture and owes its heritage to the Motorola 6800 microprocessor. It is a standardized 21-slot, 64-bit backplane architecture, coordinated and controlled by the VMEbus International Trade Association (VITA). TI is working with VITA on the SN74VMEH22501, a new backplane-optimized device that supports the 2eVME and 2eSST protocols. More information on VITA can be obtained at http://www.vita.com. More information on the new VME device can be obtained at http://www.ti.com/sc/etl.

6 What is GTL?

GTL is a reduced-voltage-swing (<1 V), open-drain/collector, differential-input JEDEC standard that allows higher frequency operation than TTL devices in point-to-point and lightly loaded memory-interface-bus applications. The reduced voltage swing reduces EMI and allows higher frequencies. For best signal integrity, the open-drain/collector arrangement facilitates matching the termination resistor (R_{TT}) to the trace impedance (Z_O). As shown in Figure 1, the open-drain/collector pulls the signal low when the device is turned on, but when the device is turned off, the pullup termination resistor is required to pull the signal high to the termination voltage (V_{TT}). The GTL standard is V_{TT}/V_{OH} = 1.2 V, V_{OL} = 0.4 V, and V_{IH} and V_{IL} set ±50 mV around the GTL differential-input reference voltage (V_{ref}) of 0.8 V.

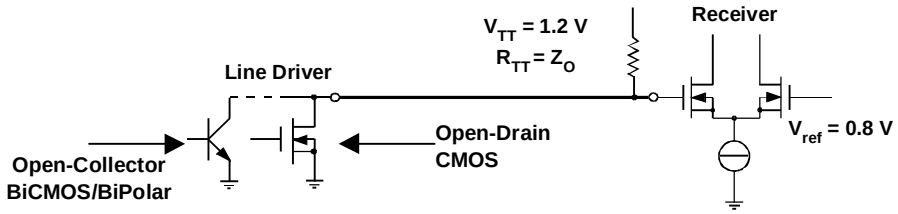

Figure 1. GTL Open-Drain/Collector Differential-Input Device

Open-drain and open-collector devices operate in exactly the same way to sink energy to ground. Open drain refers to CMOS transistors, while open collector refers to bipolar transistors. GTL devices can be manufactured using either process.

GTL+ is a variation on GTL that moves V_{ref} from 0.8 V to 1.0 V so that it is farther from the ground-bounce region. GTL+ voltage swing improves the upper and lower noise margins. Voltage swing is from V_{OL} = 0.55 V to the termination voltage of V_{TT}/V_{OH} = 1.5 V.

Any device that operates at GTL signal levels also can operate at GTL+ signal levels, and vice versa, with GTL+ being the preferred signal level due to its higher noise margins. In unusually noisy situations, V_{ref} can be adjusted to other than 0.8 V or 1.0 V in either standard to equalize, and, therefore, maximize both the upper and lower noise margins.

GTL devices are bidirectional translators (see Figure 2). A-Port (daughter-card side) input can be 5-V CMOS, TTL, or LVTTL logic levels; output is LVTTL, which is compatible with TTL logic levels. B-Port (backplane side) input and output is GTL or GTL+ signal levels.

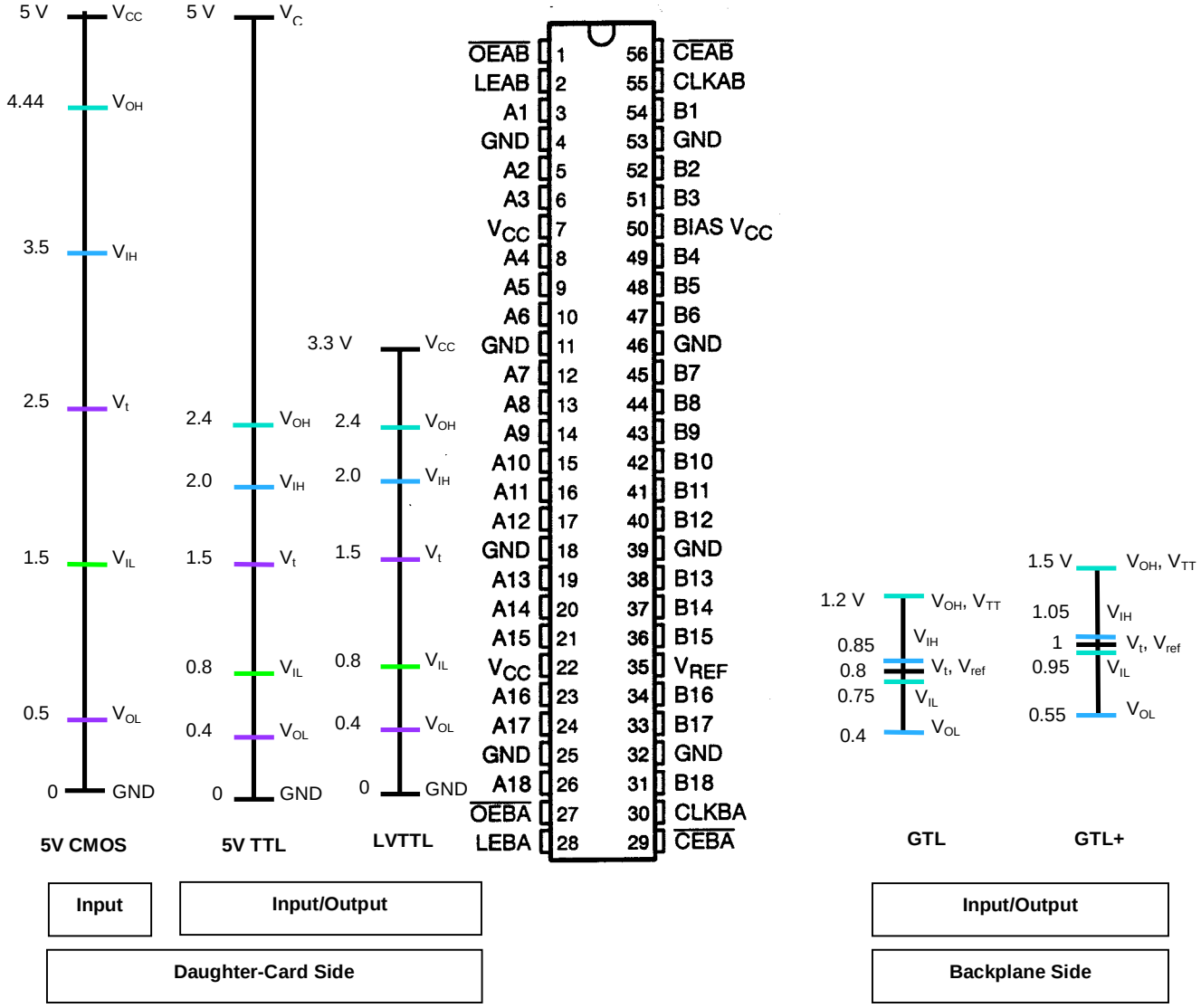

Figure 2. GTL Bidirectional Translator

As shown in Figure 3, V_{ref} is set by an R/2R resistor network between V_{TT} and GND. The resistor network maintains balanced upper and lower noise margins for any termination-voltage fluctuations. A 0.1- to 0.01-μF bypass capacitor buffers voltage fluctuations and should be as close to the V_{ref} pin as possible.

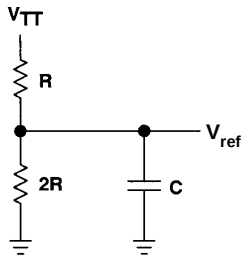

Figure 3. GTL R/2R Resistor Network

V_{ref} is generated locally on each card, using size 805 1-kΩ and 2-kΩ ±1% resistors. Each device V_{ref} input takes, at most, 10 μA, so one resistor network per card is acceptable. The card resistor network takes V_{TT} from the backplane through a connector power pin. Do not distribute the V_{ref} power across all cards from one resistor network.

7 What is the difference between GTLP and GTL?

TI introduced the GTL family of devices in 1993. GTL devices were designed with faster edge rates to drive a lumped load. Originally, these devices were designed for small buses on a board, e.g., memory applications, and did not support hot insertion. The devices rang excessively when used in larger multipoint distributed-capacitance backplane applications because of the faster edge rate. Maximum backplane frequency was limited to about 30 MHz.

GTLP devices were introduced in 1997 to serve distributed-capacitance backplane applications. GTLP is a subset of GTL devices, with one major difference. GTLP incorporates improved output edge-control (OEC) circuitry that slows the edge rate and reduces ringing, which allows maximum possible frequencies above 80 MHz in backplane applications. GTLP devices can operate at GTL signal levels, but are optimized for, and normally only specified at, GTL+ signal levels (V_{OL} = 0.55 V to V_{OH} = 1.5 V, with V_{ref} = 1.0 V). GTLP backplane-optimized devices normally refer to GTLP instead of GTL+ as the 1.5-V V_{OH}/1.0-V V_{ref} standard, while GTL lumped-load optimized devices refer to GTL+ at this voltage level.

The waveforms in Figure 4 demonstrate the difference between the TI SN74GTL16612 and the newer SN74GTLPH16612, and how the backplane-optimized edge rates improve signal integrity in a distributed load.

Test results for the competitor's GTLP16612, a pin-for-pin functional equivalent of the SN74GTLPH16612, is shown in Figure 4 for comparison. These receiver waveforms were obtained using a fully loaded 16-slot demonstration backplane, with Z_O = 50 Ω, R_{TT} = 24 Ω, slot spacing = 0.9 inch, and data frequency of 37.5 MHz. The driver card was in slot number 8 and the receiver card was in slot number 1.

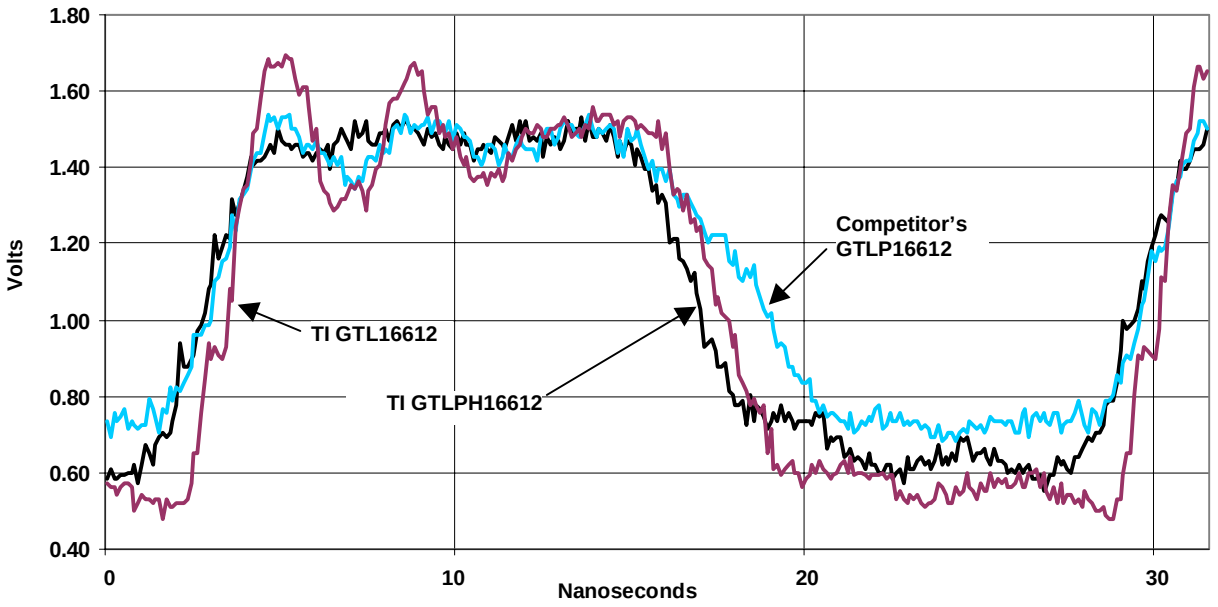

Figure 4. Demonstration of Output Edge Control

All three devices shown in Figure 4 have bus hold on the LVTTL A port. But, only the newer TI GTLP family uses H in the part number to denote bus hold, because there are several devices in the GTLP family without bus hold. All TI GTL devices have bus hold, while the competitor's GTL or GTLP family has some of both; the only way to determine the configuration is by referring to the data sheet.

A typical single-bit distributed-capacitance open-drain/open-collector backplane physical representation is shown in Figure 5. Normally, backplanes are 4, 16, 32, 64, 128, or more bits wide, with each bit identical to the representation in Figure 5. Both GTL and GTLP devices need a pullup resistor to pull the bus high. In this representation, the device in slot 1 is on, pulling the trace below 0.55 V, and providing a valid low. Receivers in slots 2 through 20 detect that the signal is low and, if not in the high-impedance state, transmit a low logic level to the A-port daughter-card side. Although not shown, each driver/receiver on the daughter card is a transceiver that can be configured to transmit or receive signals from the backplane. When the device in slot 1 is turned off, the bit is pulled high to 1.5-V by the 22-Ω termination resistors. The receivers in slots 2 through 20 detect that the signal is now high and transmit a high logic level to the daughter card. This process is repeated multiple times, with any card being able to transmit low signals onto the backplane. This can be done, even with multiple devices at the same time (wired-OR), without bus contention. This example assumes true logic.

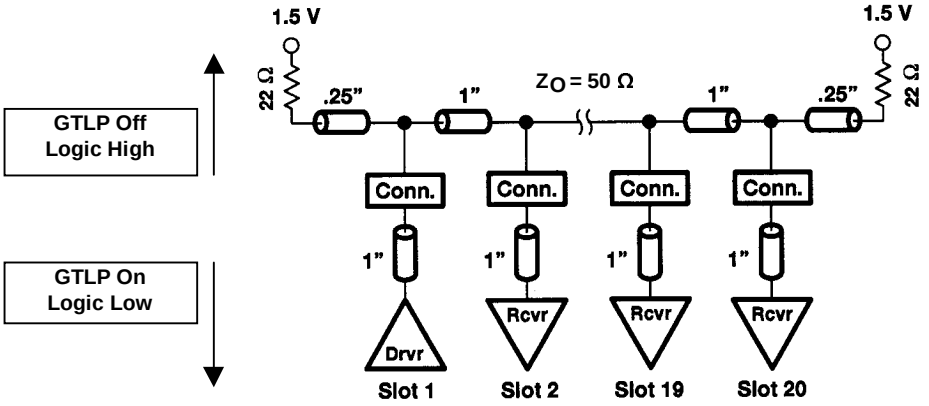

Figure 5. GTLP Open-Drain Backplane Physical Representation

GTLP devices are offered in two drive levels to match the termination-resistance value. For best signal integrity and incident-wave switching, the termination resistor should match or be smaller than the effective trace impedance. The effective trace impedance and, hence, the optimum termination-resistance value, varies, based on stub length, device C_{io}, slot pitch, and type of connector. Medium-drive (50 mA) devices are good replacements for existing TTL/LVTTL devices where higher frequencies are needed, but lower power consumption is a concern. These devices should be used with termination-resistor values ≥38-Ω. High-drive (100 mA) devices are best for replacing ABTE/FB+ devices where lower termination resistor values (22 Ω to 38 Ω) are required. Either medium- or high-drive devices can be used with higher resistance (e.g., 60 Ω) termination resistors, with the only outcome being the device pulls V_{OL} to a lower level, closer to GND, and probably poorer signal integrity, unless the effective trace impedance also is 60 Ω.

Incident-wave switching ensures that the first received signal during a transition (low to high or high to low) is valid, and reduces wait time. Reflected-wave switching requires additional wait time as shown in Figure 6.

	SWITCHING WITH THE INCIDENT WAVE	SWITCHING WITH THE REFLECTED WAVE
A⇒B	$t_{pd\ Driver} + t_{pd\ Receiver}$ = 5 ns + 5 ns = 10 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 10 ns + 5 ns = 30 ns
A⇒C	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns
Worst case	20 ns	30 ns

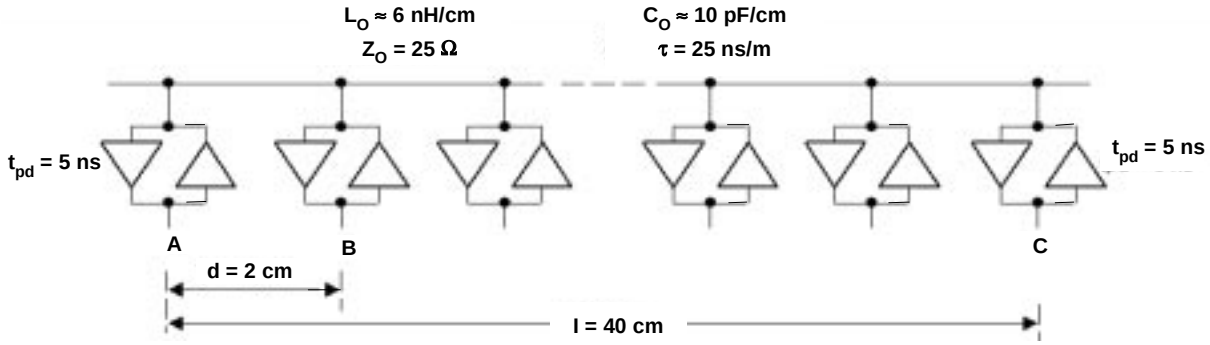

Figure 6. Reflected-Wave Switching

Additional information on incident-wave switching is in the *Fast GTLP Backplanes With the GTLPH1655* application report, literature number SCBA015A.

In summary, GTLP is a bidirectional translator (5-V CMOS, TTL or LVTTL to GTLP, and GTLP to LVTTL or TTL) that facilitates significantly higher frequencies (>80 MHz) and higher data throughput in multipoint, heavily loaded, distributed-capacitance backplane applications because the B-port GTLP output transistors produce these features:

- Reduced voltage swing (<1 V), which reduces EMI over TTL solutions.
- Optimized OEC with low slew rates (0.35 to 0.5 V/ns), which minimizes overshoot in distributed loads.
- Open-drain configuration with matched termination resistors (≥22 Ω high drive or ≥38 Ω medium drive), which ensures incident-wave switching and optimum signal integrity.
- I_{OFF}, PU3S, and BIAS V_{CC} precharge circuitry prevent data disturbance during card insertion or removal, permitting full live-insertion capability.

8 What is distributed capacitance?

Figure 7 is a simplified backplane physical representation, where an equivalent capacitive load of 12 pF replaces the receivers. The transmitter also has an equivalent capacitive load of 12 pF.

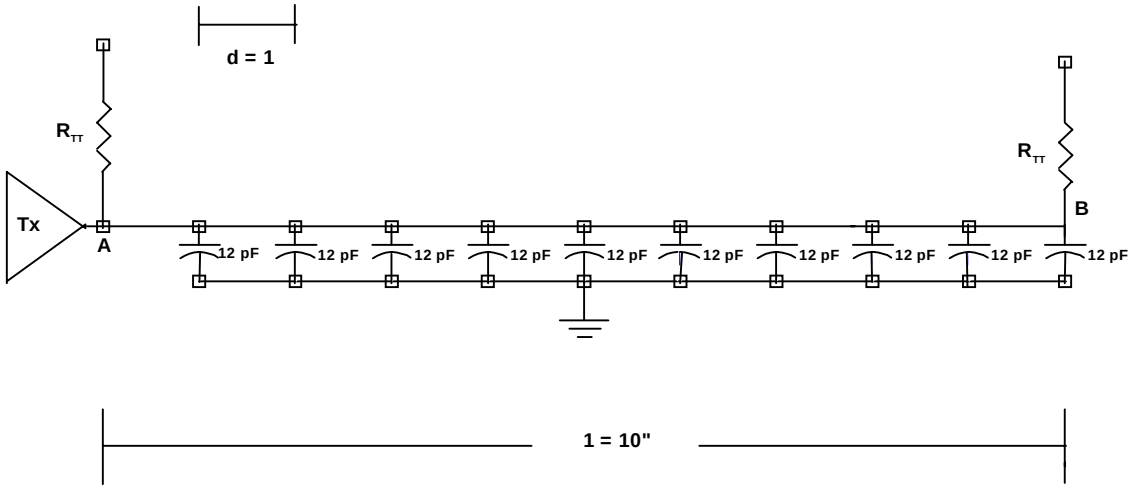

Figure 7. Simplified Backplane Physical Representation

The total capacitance (C_t) of each card is calculated by summing all the capacitive components associated with the transceiver and the connection to the backplane. Figure 8 shows a typical connection scheme between the backplane stripline and the transceiver device on the daughter card. Point C is the connection to the backplane stripline, and point D is the connection to a transceiver integrated circuit. The total capacitance at point C is the sum of each of the elements in the connection chain.

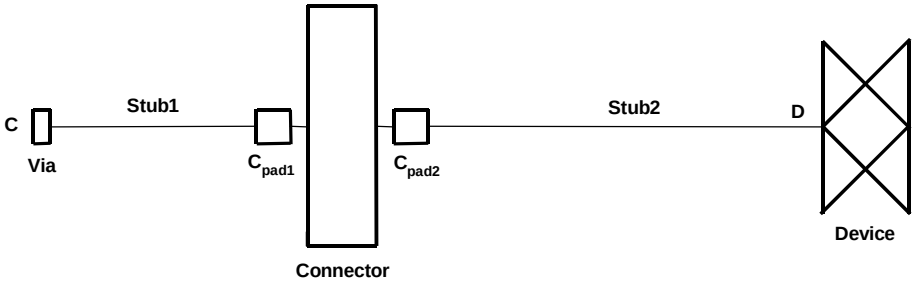

Figure 8. Typical Backplane Connection Scheme

The capacitance in the chain illustrated in Figure 8 is summed as follows:

C_{via} = capacitance of via = 0.5 pF

C_{stub1} = capacitance of Stub1 = 0.0625 inch $\times$ 2.6 pF/inch = 0.16 pF

C_{cpad1} = capacitance of C_{pad1} = 0.5 pF

C_{con} = capacitance of connector = 0.74 pF

C_{cpad2} = capacitance of C_{pad2} = 0.5 pF

C_{stub2} = capacitance of Stub2 = 1 inch $\times$ 2.6 pF/inch = 2.6 pF

C_{io} = typical input/output capacitance of device = 7 pF

$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io}$

$C_t = 0.5 + 0.16 + 0.5 + 0.74 + 0.5 + 2.6 + 7$

C_t = 12 pF

This total capacitance (C_t) of 12 pF is placed at point C on the backplane for every transceiver. With all the slots filled, the 10-inch transmission line has ten 12-pF capacitors and one transmitter (12 pF) distributed at 1-inch intervals.

Total capacitance then can be distributed uniformly across the transmission line at an equivalent rate of capacitance per inch (C_d). The total capacitance per distance is the distributed capacitance. The higher the total card capacitance and the closer the card spacing (slot pitch) the heavier the backplane loading.

The distributed capacitance equals the total capacitance divided by the separation, or $C_d = C_t/d$. In our example, C_d = 12 pF per 1 inch or 472 pF per meter. The new effective trace impedance $Z_{O(eff)}$ and effective propagation delay ($t_{pd(eff)}$) can be calculated using the following equations. C_o is the characteristic capacitance, which is dependent on Z_O and is fixed.

$$Z_{O(eff)} = Z_O \Big/ \sqrt{1 + (C_d/C_o)}$$

$$t_{pd(eff)} = t_{pd} \times \sqrt{1 + (C_d/C_o)}$$

The distributed capacitance (C_d) affects both the propagation delay and the characteristic impedance of the transmission line. A larger C_d (higher C_t and/or smaller d) results in lower effective trace impedance ($Z_{O(eff)}$) and a higher effective propagation delay ($t_{pd(eff)}$).

This illustrates why the termination-resistor values should be lower than the typical 50-Ω natural transmission-line impedance in multipoint applications. Matching the termination resistor with the effective trace impedance ensures incident-wave switching and better signal integrity. Higher-drive (100 mA) devices are offered because termination values lower than 38 Ω often are required.

For example, in a 20-slot, slot pitch = 0.94 inch backplane, the characteristics in Table 1 are observed.

Table 1. Backplane Characteristics, 20 Slots at 0.94-Inch Slot Pitch

Unloaded (Natural) Embedded Microstrip Trace			Trace and 20 Empty Connectors at 0.94 Inch		Fully Loaded With 20 Cards at 0.94 Inch		Card C_t† (pF)
Z_O (Ω)	t_{pd} (ns/in)	C_O (pF/in)	$Z_{O(eff)}$ (Ω)	t_{pd} (ns/in)	$Z_{O(eff)}$ (Ω)	t_{pd} (ns/in)	
48	142	2.99	37	183	18	382	15
90	165	1.84	62	239	26	570	16.2

† Different stub lengths provide a unique C_t for each bit on the same daughter card.

Table 1 clearly shows that, in a heavily loaded backplane with the 48-Ω natural Z_O, the termination resistance should go as low as 18 Ω, but is limited to 22 Ω by the GTLP high-drive maximum recommended I_{OL}. Increasing the natural Z_O to 90 Ω can change the termination resistor to 26 Ω, a value that is within the capacity of the high-drive devices and better approximates what the medium-drive devices can handle. The disadvantage is that the backplane time of flight is about 50% higher. Typical card capacitance will be between 12 pF and 18 pF, depending on device C_{io} and stub length, with stub length being most critical. Stub length always should be less than one inch for best backplane performance. Lower C_t always is better.

For best signal integrity, termination resistor R_{TT} should equal the loaded-trace impedance ($Z_{O(eff)}$). A lower value for R_{TT} could be used to compensate for possible variations of the device typical C_{io}, up to the maximum C_{io} value.

The waveforms in Figure 9 show the effect on signal integrity in over-matched and under-matched termination conditions. R_{TT} should be less than or equal to $Z_{O(eff)}$ for optimum signal integrity and upper noise margin.

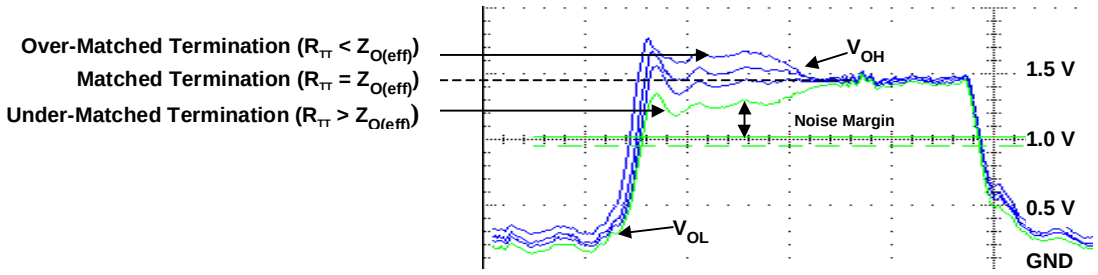

Figure 9. GTLP Waveform Under Different R_{TT} Conditions

The result of using an under-matched termination is that V_{OL} will be closer to ground and the upper noise margin will be less, as is clearly shown in Figure 9.

The result of a matched termination is optimal upper and lower noise margins.

The result of using an over-matched termination is that V_{OL} on the card farthest from the driver is higher and the lower noise margin is reduced.

More information on calculating distributed capacitance is in the *Basic Design Considerations for Backplanes* application report, literature number SZZA016A, at www.ti.com/sc/docs/apps/logic/appnotes.html under backplane logic.

9 What are you going to do with GTL now that you have GTLP?

TI will continue to support and expand the GTL family because these devices are well suited for voltage-level translations, point-to-point applications, and lightly loaded bus onboard-memory applications, e.g., Intel™ Pentium™ microprocessors operate at GTL+ signal levels. Customers can switch between GTL and GTLP families, but must be aware of the differences in the edge rates. GTLP devices can be used in memory applications, but, due to the slower edge rates, the device propagation delay is longer. GTL devices should not be used in high-frequency heavily loaded backplanes.

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10 How should I terminate GTL devices in short-distance applications?

GTL products are open drain, so they must be connected to V_{TT} via proper R_{TT} termination resistors. One question is that if GTL or GTLP is used to transmit signals on a daughter card, the distance is very short, about 4 cm to 6 cm. Do we need to position a R_{TT} termination resistor at both the driver and receiver? If so, can you provide the R_{TT} based on your experience? In such a condition, how can better results be obtained?

You need only to put the R_{TT} termination resistor at the receiver end of the transmission line. On the backplanes we recommend putting the termination resistors on both ends of the backplane because you do not know when slot 1 or 20 will be the transmitter or receiver, so you have to cover both cases. The R_{TT} value should equal the loaded-trace impedance whether or not you use one or two R_{TT} termination resistors. If two are used, the effective resistance is reduced by a factor of two (i.e., 50 Ω at either end, the driver will see 25-Ω effective resistance) which means simply that the driver has to be able to sink more current. For this short trace and lower loading you could probably use a single termination resistor at the receiver that is about 10 Ω less than the natural trace impedance (i.e., If Z_O is 50 Ω, use 40 Ω.). Using the GTLP EVM, we have removed the driver termination and the signal integrity was satisfactory, however, when the receiver termination was removed and only the driver side was terminated, signal integrity was poor. As you would expect, it did not work when both terminations were removed.

11 What is the advantage of using GTLP in my backplane?

Increasing bandwidth and data throughput speeds are major issues today for many systems, as our world becomes increasingly interconnected. TI has taken what it has learned about the use of GTL over the last four years and applied this expertise and knowledge to future backplane-based applications using GTLP devices.

TI's GTLP family has been designed specifically for optimum signal integrity in multipoint, heavily loaded, distributed-capacitance backplanes like those shown in Figure 10. These improvements allow higher data throughput in the same bit-width backplanes that are currently being used and provide an easy migration from current TTL/LVTTL and BTL/FB+ backplane drivers to GTLP devices.

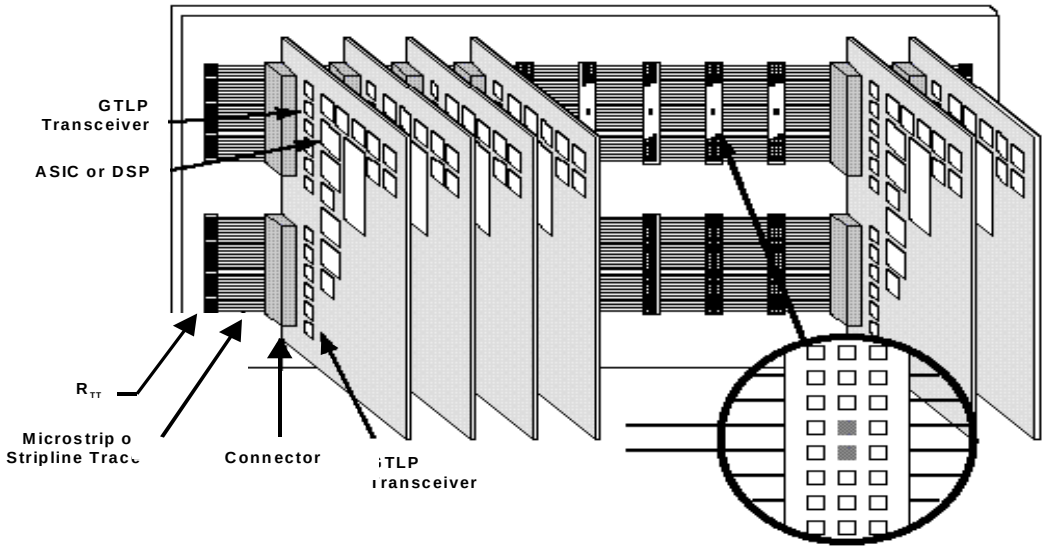


Figure 10. Heavily Loaded, Distributed-Capacitance Backplane Installation

GTLP devices allow higher frequencies on the backplane because of the improved signal-integrity/incident-wave switching the results from the reduced swing (<1 V), lower slew rate (0.35 V/ns to 0.5 V/ns), and matched termination resistors.

Additionally, GTLP fully supports live insertion, a capability that is imperative in high-availability communications and networking applications. I_{off} and PU3S provide hot-insertion capability, while the BIAS V_{CC} precharge circuitry precharges the B-port input/outputs to the threshold voltage. This protects active data on the backplane from voltage spikes or glitching, and provides true live-insertion capability.

GTLP devices are designed and manufactured in an advanced CMOS process that reduces static-power consumption.

GTLP devices are 5-V tolerant because, although most applications are migrating to 3.3 V, or lower, some existing circuits/devices on the board remain at 5 V.

GTLP is offered in a wide variety of packaging options and pinouts that are similar to previous-generation devices. This helps simplify the designer's task of migrating to a GTLP-based backplane. High-drive devices are identical to the comparable medium-drive devices, except for the addition of five ground, two V_{CC}, and one edge-rate control (ERC) pins. The additional ground and V_{CC} pins reduce ground and V_{CC} supply noise, thus providing additional noise margin. The ERC pin allows the selection of either a slow or fast edge rate by holding the control pin at V_{CC} or ground. The faster edge rate reduces the propagation delay and allows higher frequency operation in an optimally terminated backplane.

Lumped loads normally are associated with point-to-point applications. However, GTLP devices have been designed into actual backplane netlists and a resistance/inductance/capacitance (RLC) network that closely matches the results in a backplane. TI's GTLP devices are tested into a lumped load, as are all other devices offered by TI and other semiconductor manufacturers. Engineers are using GTLP devices in high-performance distributed-capacitance loads and the actual switching characteristics are radically different from the lumped loads that are specified in the data sheet. TI SPICE-modeled values using the RLC network are included in the data sheet to better help engineers understand backplane effects. In summary, the data-sheet switching-characteristics into the lumped-load parameter values are going to look ugly but the actual performance of the device in a distributed load is going to be beautiful.

12 What is the difference between GTLP and LVDS?

GTLP is a single-ended low-voltage-swing (<1 V) standard, whereas LVDS is a differential low-voltage-swing (350 mV, typical) standard. Single-ended devices require only one trace per bit of data, while differential devices require two traces for each bit of data. Differential devices, e.g., LVDS, LVDM (backplane optimized LVDS), SERDES, Wizard, etc., work well for high-speed data transmission over long cables, such as between cabinets, cards, or racks, as shown in Figure 11, but they do not fit all applications where simplicity and lower cost of implementation indicate that single-ended devices are better for use in multislot backplane applications.

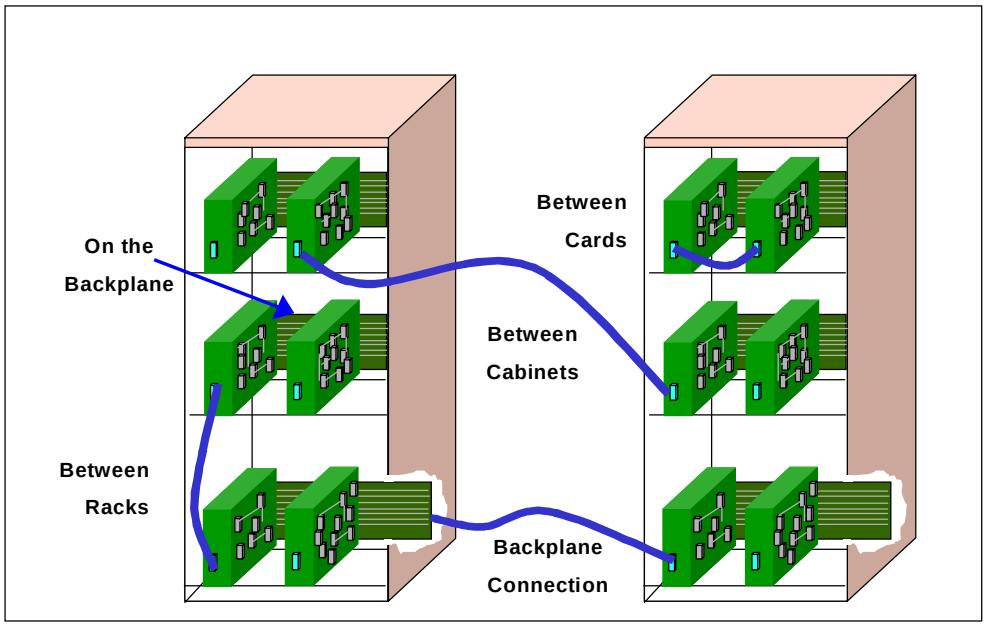


Figure 11. Various Equipment Connections

13 How does GTLP compare to other single-ended and differential bus solutions?

Reduced voltage swing, lower slew rate, and open-drain construction allow GTLP devices to operate at higher frequencies than TTL devices in parallel-backplane architecture. GTLP offers an alternative to high-data-throughput differential devices where parallel backplanes are the best solution and higher data throughput is now required (see Table 2).

Table 2. Comparison of Single-Ended vs Differential Bus-Interface Solutions

Device (typically 16245 function)	Bidirectional (B) or Unidirectional (U)	V_{CC} (V)	Tolerant to	Hot Insertion	Live Insertion	Number of Pins in the Package	Number of Bits	Cost ($ in DGG qty 999 Internet Price)	Card Interface Drive (mA)	BP Interface Drive (mA)	I_{CC} (mA - Output Low)	C_{io} (pF - max)	Freq. Max BP (MHz)	Data Throughput Per Package (Mbps - Transparent Mode)	Data Throughput per Bit-$ (Mbps/bit$)	Data Throughput per Bit (Mbps/bit)
Single-Ended Bus Interface Solution																
ABT	B	5	5	Y	N	48	16	$1.92	-32/+64	-32/+64	32	6 -typ	33	1,056	34	66
LVT	B	3.3	5	Y	N	48	16	$2.17	-32/+64	-32/+64	5	10 - typ	33	1,056	30	66
ALVT	B	3.3	5	Y	N	48	16	$3.09	-32/+64	-32/+64	5	6 - typ	40	1,280	26	80
GTLP Medium Drive	B	3.3	5	Y	Y	48	16	$5.00	-24/+24	50	35*	9	80	2,560	32	160
ABTE	B	5	5	Y	Y	48	16	$5.01	-12/+12	-60/+90	48	8	45	1,440	18	90
BTL/FB+	B	5	5	Y	Y	52	8	$10.47	-3/+24	100	70	5	50	800	10	100
GTLP High Drive	B	3.3	5	Y	Y	56	16	$5.85	-24/+24	100	35*	10	100	3,200	34	200
Differential Bus Interface Solution																
ECL/PECL	U	5	5	N	N	24	8	$10.20	-3/+24	-25	69		80	640	8	80
TLK2500	B	2.5	3.3	Y	N	64	16	$36.70	-1/+1	1 Serial	135	Serial		2,500	4	156
LVDS386/387	U	3.3	5	Y	Y	64	16	$9.58	-8/+8	16 - Serial	70	Serial		10,080	66	630
LVDS93/94 SERDES	U	3.3	5	Y	Y	64	28	$3.50	-4/+4	5 - Serial	84	Serial		1,820	19	65

The maximum backplane frequency is based on good backplane construction and termination techniques. The TLK, LVDS, and SERDES data throughputs are theoretical maximum values; actual data throughput rates are less.

Comparison of cost of GTLP versus other single-ended technologies shows that GTLP data throughput per bit-dollar is about the same as the most popular parallel technologies, such as ABT. Although GTLP costs about three times more than ABT, the GTLP data throughput is more than three times greater than ABT in heavily loaded backplanes. GTLP also is an excellent replacement for ABT or LVT in low-frequency applications where signal integrity is an important consideration.

Strong interest in point-to-point differential-backplane connections in high-end networking and 3G wireless base-station applications has been seen, although that requires dozens to hundreds of connections along a 19-inch backplane. Typically, telecom engineers dislike single-ended solutions because of past EMI, maximum system frequency, and power-consumption difficulties with older TTL solutions. The tradeoff is the ease of design of the single-end solution versus the low EMI, higher frequency, and lower power consumption of differential designs. GTLP provides massive throughput at lower EMI and power-consumption levels than TTL, which is what they're thinking of when they think single-ended. Throughput on the backplane using GTLP devices at lower cost and without serious EMI or crosstalk effects compares very favorably with point-to-point serial schemes.

Figure 12 allows you to pick the bus solution technology offered by TI that would be most appropriate, based on throughput and transmission distance.

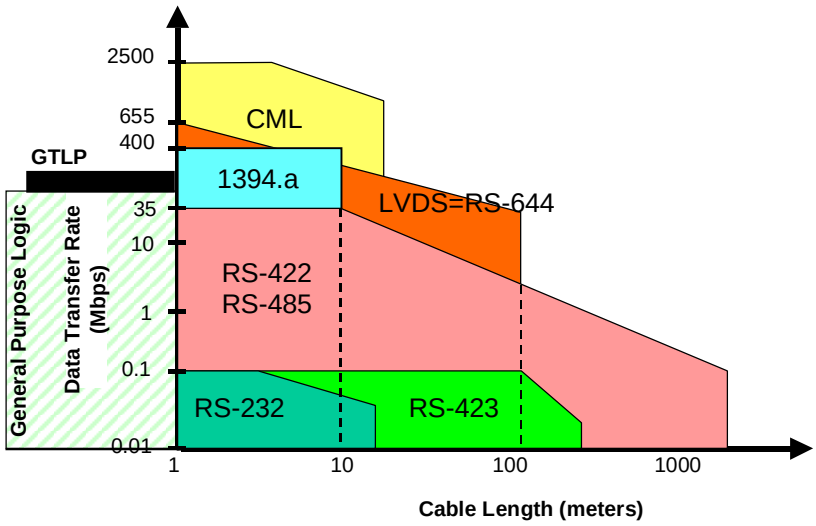


Figure 12. Data Transfer Rate (Mbps)

More information on TI's vast array of parallel and serial technologies can be found in the *Comparing Bus Solutions* application report, literature number SLLA067.

More information on LVDS, LVDM, SERDES, Gigabit CMOS, and 1394 can be found on TI's semiconductor internet home page at www.ti.com/sc.

More information on GTLP can be found on TI's GTLP internet home page at www.ti.com/sc/gtlp.

14 What is the maximum data throughput using GTLP?

Data throughput is a function of clock frequency times the bit width of the backplane. Increasing the maximum frequency or backplane bit width increases data throughput. GTLP devices can operate at speeds up to 175 MHz into a distributed load with good signal integrity.

A 32-bit backplane operating at 110-MHz clock frequency has a data transfer rate of 1.76 Gbit/s in single-edge latched-mode (data is transferred at one-half the clock frequency) applications to 7 Gbit/s in dual-edge transparent-mode applications.

Data throughput in GTLP backplanes is now limited by timing requirements, not signal integrity, as in past backplane devices. Maximum frequency is a function of device maximum propagation delay (t_{pd}), pin-to-pin skew, backplane construction or length, and how the clock is distributed (see Figure 13).

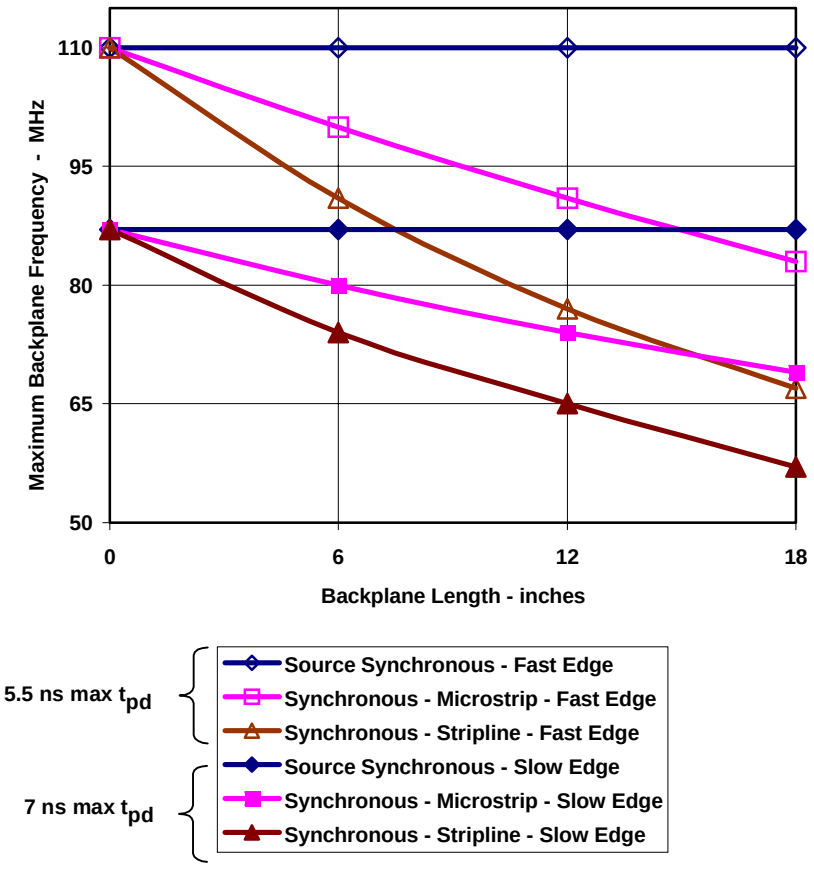


Figure 13. Maximum Backplane Frequency

Propagation delay is a function of the edge rate. Only high-drive GTLP devices are able to operate at both slow and fast edge rates, with a maximum t_{pd} of about 7 ns and 5.5 ns, respectively. Medium-drive devices operate only at the slow edge rate, with a maximum t_{pd} of about 7 ns. These are design goals, and actual values may be different.

Setup and hold times and skew are inherent in the device.

Backplane flight time depends on backplane length and construction (microstrip or stripline). Microstrip places the trace on top of the printed circuit board and does not reduce the flight time as much as stripline, but it is more susceptible to EMI. Stripline places the trace between printed circuit board dielectric layers and is less susceptible to EMI, but the signals are slower and, consequently, flight time is longer. Most high-quality backplanes use stripline construction to minimize EMI. Proper backplane layout and stub lengths of less than 1 inch help minimize backplane capacitance.

Most backplanes use a system clock that provides an absolute clock signal to all cards at the same time. Maximum system frequency is reduced based on backplane length, as shown in Figure 13, to accommodate the difference between the time-of-arrival of the driver card and receiver card clock signal (flight time), respectively. Source-synchronous operation is a technique in which the clock is sent with the system data as a relative clock signal. This means that there is no delay due to backplane flight time because the clock is sent along with the data. Flight time always is zero; therefore, maximum frequency is independent of backplane length.

Studies performed using the 19-inch 20-slot GTLP EVM with the SN74GTLPH1655 DGGR device show that the maximum frequency is 46 MHz in system-clock mode and 120 MHz in source-synchronous clock mode, and, for short time periods, 160 MHz in asynchronous mode.

In summary, maximum frequency (MHz) is the inverse of the maximum delay time (ns), i.e., 10 ns = 100 MHz. Maximum delay time depends on the sum of these factors:

- Maximum propagation delay
  - Fast edge (5.5 ns)
  - Slow edge (7 ns)
- Setup time (2.5 ns)
- Skew time (1 ns)
- Backplane flight time
  - Source synchronous - flight time is zero and is independent of backplane length because the clock is sent with the data
  - Microstrip (1 ns/6 inches)
  - Stripline (~2 ns/6 inches)

To improve backplane performance, review the *High-Performance Backplane Design With GTL+* application report, literature number SCEA011A, and *Basic Design Considerations for Backplanes* application report, literature number SZZA016A.

Additional information on calculating backplane impedance can be found at www.ultracad.com. There is detailed information on microstrip and stripline calculations and an impedance calculator that can be downloaded.

15 What is the difference between synchronous clock and source-synchronous clock?

Synchronous clock is an **absolute** clock in which each card receives the same clock signal at exactly the same time. A clock generator with clock lines running to each card provides this absolute clock. For the clock signal to arrive at each card at exactly the same time, the line length must be exactly the same. For cards closer to the clock board, the lines are mitered (run up and down, parallel to each other) to add distance to the line.

Source-synchronous clock is a **relative** clock. The driver card uses the incoming absolute clock signal for timing, but all receiver cards use the clock sent from the driver card. Since the driver card data and slightly delayed clock signal are sent at the same time, backplane length or flight time is not a factor in timing calculations, unlike the absolute clock, which has to account for the backplane length or flight time between the driver and receiver.

Additional information on source-synchronous operation was presented by Lee Sledjeski at DesignCon 2000, in which he discussed private source-synchronous clocks for every 16 bits of data to minimize delays due to device skew. The paper can be viewed at http://www.fairchildsemi.com/products/backplane/designcon/lsdcon2k.pdf. These private clocks can be implemented easily with the GTLPH16916 or the high-drive GTLPH1616; each has one delayed buffered clock bit for every 17 bits of data. This paper also discusses reducing the clock signal transmitted across the backplane by a factor of one-half as a way to transfer data at the full system clock rate, i.e., data rate equals clock rate, which is 110 MHz.

16 What GTLP devices are available and how much will they cost?

The first wave of TI's GTLP devices comprises seven medium-drive and six high-drive devices. They are offered in ultra compact (LFBGA/VFBGA), small (TVSOP), medium (TSSOP), or large (SOIC or SSOP) packages. Pricing is two to three times higher than standard LVTTL/TTL backplane drivers, but GTLP devices allow two to four times higher maximum backplane frequencies, providing higher data throughput without migrating to more complex serial devices. Because signal integrity is superior in distributed loads, it also makes sense to use GTLP in low-frequency applications where the noise margin using HC, ABT, or LVT is not acceptable because of the weaker drive and poorer signal integrity. GTLP pricing is the same or less than TI's current GTL pricing (see Table 3).

Obtain the data sheet at www.ti.com/sc/gtlp. Go to www.ti.com/sc/package for package drawings, symbolization, layout, and thermal-performance information.

Table 3. GTLP Family Offerings

SN74GTLP	Function	Bits	Pin Count	SOIC	SSOP	TSSOP	TVSOP	BGA	Suggested Resale Price (1000 Quantity)
Medium Drive (50 mA)									
H306	Bus Transceiver	8	24	DW		PW	DGV		$4.65
817	1:6 Fanout Driver	NA	24	DW		PW	DGV		$5.40
H16612	Universal Bus Transceiver	18	56		DL	DGG			$7.35
H16912	Universal Bus Transceiver	18	56			DGG	DGV		$7.90
H16916	UBT with Buffered Clock	17	56			DGG	DGV		$7.90
H16945	Bus Transceiver	2 x 8	48			DGG	DGV	GQL	$5.00
H32945	Bus Transceiver	4 x 8	96					GKE	$10.50
High Drive (100 mA)									
1394	Transceiver	2	16	D		PW	DGV		$3.75
H1612	Universal Bus Transceiver	18	64			DGG			$9.15
H1616	UBT with Buffered Clock	17	64			DGG			$9.15
H1645	Bus Transceiver	2 x 8	56			DGG	DGV	GQL	$5.85
H1655	Universal Bus Transceiver	2 x 8	64			DGG			$9.15
H3245	Bus Transceiver	4 x 8	114					GKF	$12.25

Relevant package application information is contained in the following reports:

Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C.

32-Bit Logic Families in LFBGA Packages 96 and 114 Ball Low-Profile Fine-Pitch BGA Packages application report, literature number SCEA014.

Comparison of Electrical and Thermal Parameters of Widebus SMD and LFBGA Packages application report, literature number SCYA007.

17 These function numbers are different. How do they compare to normal logic functions?

When the GTL family was introduced, it was decided to differentiate GTL function numbers from other similar logic functions because of the V_{ref} pin and the reduced B-port GTL signal levels. The first GTL device (SN74GTL16612) has exactly the same pinout as the 3.3-V V_{CC} '16601 universal bus transceiver, except that the two V_{CC} pins on the B-port side serve different purposes. Pin 34 is used for the GTL differential V_{ref} input and pin 50 is used for the 5-V V_{CC} that powers the GTL circuitry. The first GTLP device is the SN74GTLPH16612, which is identical to the SN74GTL16612, except for the improved B-port circuitry that allows better performance in distributed loads. Based on the SN74GTLPH16612, other existing GTL devices, and TI's device-naming convention, the names of the additional GTLP devices were selected as shown in the migration summary below.

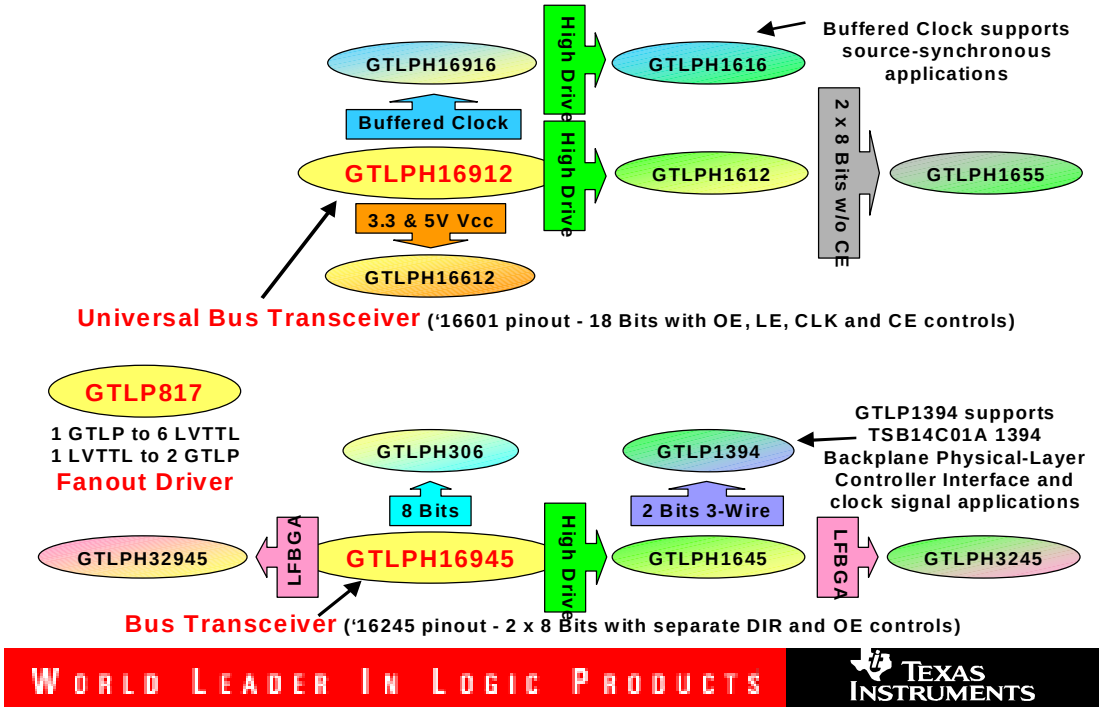


Figure 14. GTLP Migration Summary

GTLP device naming considerations are:

- The 16XXX and 32XXX function numbers signify Widebus™ (16 to 18 bits) and Widebus+™ (32 to 36 bits) bit widths. Typically, octals are XXX only.
- Function numbers of XX9XX signify single-V_{CC} operation and the incorporation of BIAS V_{CC}.
- Medium-drive devices are either three or five digits. High-drive devices have the "9" removed and are four digits long to conform to the prior BTL/FB+ high-drive device-naming convention.
- The 2-bit high-drive 1394 is designed uniquely to support the 1394 backplane physical-layer controller and, therefore, was named GTLP1394. Application information is included in the data sheet. The GTLP1394 is also very useful in providing 2-bit GTLP clock signals in backplane applications.
- "H" is added after the GTLP family name if bus hold is featured on the A-port I/O pins. Typical 1394 and 817 applications do not require bus hold, so bus hold was not included in these devices. Bus hold is not required on B port I/O pins because the termination resistors keep the bit high if it is not actively pulled low by the device.

18 I know what a bus transceiver is, but what is a UBT™?

A UBT™ device performs numerous functions that are done by other logic functions by proper selection of their OE, LE, and CLK control pins (‘16500 or ‘16501 functions) or their OE, LE, CLK, and CE control pins (‘16600 or ‘16601 functions). The ‘16601 logic function is shown in Table 4.

Table 4. '16601 Logic Functions

FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

UBT, Widebus, and Widebus+ are trademarks of Texas Instruments.

UBT devices can be used for many different logic functions, reducing the number of different devices you have to buy. This reduces the number of other types of devices that must be maintained in inventory. Ordering larger quantities of UBT devices can reduce the price. However, simpler functions normally are less expensive. Backplane applications usually require only bus-transceiver functionality. Other applications might need more complex functions. The functions available from a UBT device or UBT device with clock enable are listed in Table 5.

The GTLPH306 is a functional equivalent of the ‘245, the GTLPH16945 is a pin-for-pin functional equivalent of the ‘16245, and the GTLPH16912 is a pin-for-pin functional equivalent of the ‘16601.

Table 5. UBT Equivalent-Functions Table

Function	8 Bit	9 Bit	10 Bit	16 Bit	18 Bit
Transceiver	`**245**, `623, `645	`863	`861	`**16245**, `16623	`16863
Buffer/driver	`214, `244, `541		`827	`16241, `16244, `16541	`16825
Latched transceiver	`543			`16543	`16472
Latch	`373, `573	`843	`841	`16373	`16843
Registered transceiver	`646, `652			`16646, `16652	`16474
Flip-flop	`374, `574		`821	`16374	
Universal bus driver					`16835
Standard UBT					`16500, `16501
GTLPH1655 replaces above functions and is similar to the ’16501 standard UBT (OEAB, OEBA, LEAB, LEBA, CLKAB, CLKBA), but is at GTLP levels on the B port and is split into two 8-bit sections.					
Registered transceiver with clock enable	`2952			`16470, `16952	
Flip-flop with clock enable	`377	`823			`16823
Standard UBT with clock enable					`16600, `16601
GTLPH16612, ’169121/6, and ’1612/6 replace all above functions and are identical to the ’16601 Standard UBT with clock enable, but are at GTLP levels on the B port.					

19 I need an alternate source. Are there any?

Several companies manufacture GTL and GTLP devices. Fairchild (FSC) entered the market in 1997. Pericom and Philips also recently entered the market.

Pericom's two released offerings closely match the FSC GTLP data-sheet specifications, and it is assumed that their other planned offerings will also.

Philips markets their GTL devices toward the bus on the card/microprocessor interface market much like TI's existing GTL family. The GTL family has faster edge rates and is not optimized for backplane applications.

TI offers a wide range of medium-drive GTLP devices, a wider range of high-drive GTLP devices, and the widest range of packaging offerings. These devices support the needs of the emerging high-data-throughput parallel-backplane market. Additionally, TI has included a BIAS V_{CC} feature in the medium- and high-drive GTLP devices in place of one of the V_{CC} pins, to support true live insertion. The BIAS V_{CC} circuitry is disabled when V_{CC} is applied; therefore, except for the precharge feature, the TI device is fully functional in competitors' sockets.

All devices occupying the comparable bit width/drive box in Table 6 are pin-for-pin functional equivalents.

All 816/817 devices have the same pinout. They are one GTLP input to six TTL/LVTTL outputs and one TTL/LVTTL input to two GTLP outputs, but are various drives and V_{CC}. Refer to the data sheet, then test each device to pick the best one for your application.

Table 6. GTLP Device Cross-Reference

Bit Width	TI - SN74GTLP		Fairchild - GTLP		Pericom - GTLP	
	Medium Drive	High Drive	Medium Drive	High Drive	Medium Drive	High Drive
32	H32945	H3245				
18	H16912	H1612	*18T612*		*18T612*	
	H16612		16612		16612A	
17	H16916	H1616	*17T616*			
			16616		16616	
			16617		16617	
16		H1655		*16T1655*		*16T1655*
	H16945	H1645				
8	H306		8T306		8T306	
6	817		6C817			
			6C816A			
			6C816		6C816	
2		1394				

Legend	
H16612 (underline)	= 3.3- and 5-V or 5-V V_{CC} operation
	= Released to Market
H16912 (black)	= 3.3-V V_{CC} while *18T612* (blue italics) is 3.3-V V_{CC} but not 5-V tolerant
Medium Drive = 50 mA, High Drive = 100 mA	

20 Are the alternate-source devices identical?

While all GTLP devices operate in the same manner and have the same pinout and functionality, they are not all designed equally. The most important characteristic in GTLP devices is the B-port OEC circuitry and the corresponding edge rate. Faster edges perform poorly in backplane. In our demonstration backplane under the same conditions, the SN74GTLPH16612 had better signal integrity than the FSC GTLP16612, and the SN74GTLPH1655 had better signal integrity than the FSC GTLP16T1655. We believe that TI's GTLP devices exhibit excellent signal integrity due to the improved OEC and TI-OPC™ circuitry. If the design is optimized for the worst-case performance of all devices that are used, FSC or Pericom GTLP can be used as an alternate source.

Additional differences in other manufacturers' devices are shown in Table 7.

Table 7. Comparison of GTLP Features

Features	Number of Devices		
	TI	Fairchild	Pericom
Total number of GTLP devices	13	10	7
3.3-V V_{CC} operation	12	5	3
Inputs/outputs 5-V tolerant	All	6	5
I_{off} – Partial power down *(protect device)*	All	All	All
PU3S - Hot insertion *(protect equipment)*	12	4	1
LFBGA package option	3	None	None
Backplane (GTLP/B-Port) Options			
BIAS V_{CC} - Live insertion *(protect data)*	10	1	1
Output edge control	All	All	All
TI-OPC circuitry	11	None	None
Edge-rate control	7	1	1
Medium drive (34/50 mA)	7	9	6
High drive (100 mA)	6	1	1
Functionality			
Transparent mode	12	7	6
Clocked mode	5	6	5
Latched mode	5	6	5
Clock enabled mode	4	5	4
Buffered clock option	2	3	2
1-to-6 TTL/LVTTL fanout driver	1	3	1

TI-OPC is a trademark of Texas Instruments.

21 What is important about live insertion?

Many backplane systems in communications applications must remain operational 24 hours a day, 7 days a week. These systems cannot be shut down when a board is inserted or removed from the system, as frequently happens during regular maintenance or system upgrades, nor can active backplane data be disturbed.

GTLP devices fully support live insertion with I_{off}, PU3S, and BIAS V_{CC} circuitry.

BIAS V_{CC} circuitry allows easy internal precharging of the daughter-card backplane connections to mid-threshold levels to prevent glitching active data during card insertion or removal.

In the typical connection sequence shown in Figure 15, the GND and BIAS V_{CC} connections are made first to establish the GND plane and precharge the GTLP I/Os through the BIAS V_{CC} circuitry to the 1.0-V ±50-mV threshold voltage. Next, the GTLP I/O pins are connected. Because the outputs are precharged to 1.0-V before connecting with the backplane, they do not glitch any active backplane data as they are mated. Finally, V_{CC} is connected. As V_{CC} ramps up, the BIAS V_{CC} precharge circuitry is disabled and the device starts operating, presenting valid signals on the backplane.

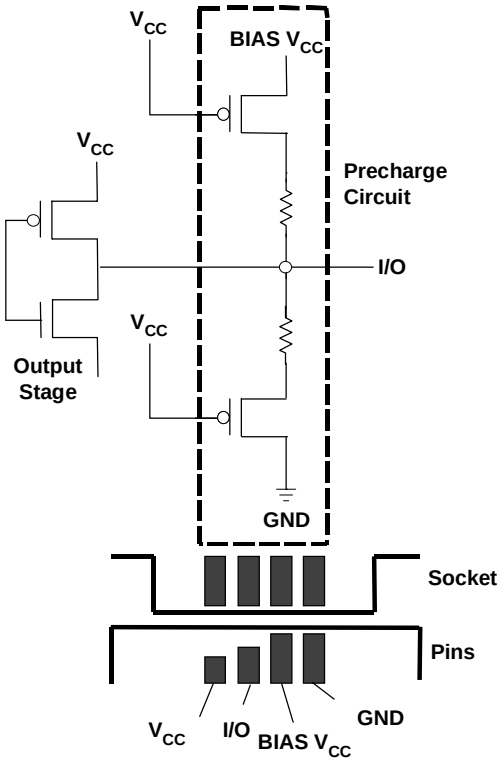


Figure 15. Typical BIAS V_{CC} Connection Sequence

22 What is the total power consumption of an 18-bit GTLP driver?

When you look at backplane performance, you must take into consideration static drive and dynamic drive. The static output drive is the current needed to maintain a steady-state dc voltage level on an output. Dynamic output drive is the current available when an output switches output states. This drive is necessary to overcome reactive loading effects and can determine the switching speeds in your applications.

Total power consumption is defined as the sum of the static (measured by the device I_{CC}), dynamic (measured by the device internal transistor switching), and output (measured by the external capacitive load) power of the device.

Static Power

$P_{STAT} = \Sigma \{V_{CC} [share_L(k) \times I_{CCL} + share_H(k) \times I_{CCH} + share_Z(k) \times I_{CCZ}]\} / n$

Where:

Σ = Sum of k = 1 to n

V_{CC} = Supply voltage

$share_L(k)$ = Average percentage share of the k^{th} output in a low state

$share_H(k)$ = Average percentage share of the k^{th} output in a high state

$share_Z(K)$ = Average percentage share of the k^{th} output in a high-impedance state

I_{CCL} = Device current consumption for static low at output

I_{CCH} = Device current consumption for static high at output

I_{CCH} = Device current consumption for high-impedance state at output

n = Total number of outputs in the device

Example 1:

A 50% duty cycle output waveform on all outputs force $share_L(k)$ and $share_H(k)$ to be 0.5 each. $Share_Z(k)$ is zero. Therefore, for an 18-bit device, sum k = 1 to 18, static power is:

$P_{STAT} = \Sigma [V_{CC} (0.5 \times I_{CCL} + 0.5 \times I_{CCH} + 0 \times I_{CCZ})]/18 = 0.5\ V_{CC} (I_{CCL} + I_{CCH})$

Example 2:

A 50% duty cycle output waveform on nine outputs and nine outputs at a fixed static low. $share_Z(k)$ is zero. Therefore, for an 18-bit device, sum k = 1 to 9, the static power is:

$P_{STAT} = \Sigma [V_{CC} (0.5 \times I_{CCL} + 0.5 \times I_{CCH} + 0 \times I_{CCZ})] / 18 + \Sigma [V_{CC} (1 \times I_{CCL} + 0 \times I_{CCH} + 0 \times I_{CCZ})] / 18$

$P_{STAT} = 0.5 \times 0.5 \times V_{CC} (I_{CCL} + I_{CCH}) + 0.5 \times V_{CC} (I_{CCL}) = V_{CC} (0.75 \times I_{CCL} + 0.25 \times I_{CCH})$

I_{CCL}, I_{CCH}, and I_{CCZ} are identical for CMOS devices, but different for BiCMOS/bipolar devices. Normally, these are combined in CMOS-device data sheets, but, because both the GTL and GTLP families include both CMOS and BiCMOS devices, all values are included to preclude questions about whether all values are the same or only the maximum value was included.

Dynamic Power

While switching the outputs, most of the dynamic power is generated in the output structure of devices that have totem-pole configurations. Because GTL and GTLP devices have open-drain/collector outputs and no active pullup transistors, dynamic power caused by current spikes due to internal charging and discharging processes within the GTLP circuit can be approximated as a very small value that, in comparison to the static and output power, is negligible.

The Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C, March 1997, at www.ti.com/sc/docs/psheets/abstracts/app/scba009.htm, provides more information on how to calculate dynamic power consumption for devices with totem-pole outputs.

Output Power

Output power per bit is:

$P_{OUT} = I_{OL} \times V_{OL} \times (1 – \text{output duty cycle})$

Where

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2)$

Example:

For an output duty cycle of 60% (output stays high 60% of the cycle),

assuming V_{TT} = 1.5 V, V_{OL} = 0.55 V, and R_{TT} = 38 Ω, then:

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2) = (1.5 \text{ V} – 0.55 \text{ V}) / (38 \Omega / 2) = 50 \text{ mA}$

$P_{OUT} = I_{OL} \times V_{OL} \times (1 – \text{output duty cycle}) = 50 \text{ mA} \times 0.55 \text{ V} \times (1 – 0.6) = 11 \text{ mW per bit}$

For an 18-bit device running all 18 bits at 60% output duty cycle,

$P_{OUT} = 18 \times 11 \text{ mW} = 198 \text{ mW}$

Total Power Consumption

Total power consumption for an 18-bit device operating at 3.3-V V_{CC} is calculated using the following equations. Nine outputs are switching at a 50% duty cycle with the other nine outputs at a fixed static low:

I_{CC} = 50 mA, V_{TT} = 1.5 V, V_{OL} = 0.55 V, and R_{TT} = 38 Ω

$P_{STAT} = V_{CC} (0.75 \times I_{CCL} + 0.25 \times I_{CCH}) = 3.3\ V\ (0.75 \times 50\ mA + 0.25 \times 50\ mA) = 165\ mW$

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2) = (1.5\ V – 0.55\ V) / (38\ \Omega / 2) = 50\ mA$

P_{OUT} switching = $I_{OL} \times V_{OL} \times$ (1 – output duty cycle) = 50 mA × 0.55 V × (1 – 0.5) = 13.75 mW/bit

P_{OUT} static low = $I_{OL} \times V_{OL} \times$ (1 – output duty cycle) = 50 mA × 0.55 V × (1 – 0) = 27.5 mW/bit

There are nine switching outputs and nine static low outputs, therefore:

P_{OUT} = 13.75 mW × 9 bits + 27.5 mw × 9 bits = 123.75 mW + 247.5 mW = 371.25 mW

The total power consumption is:

$P_{TOT} = P_{STAT} + P_{DYN} + P_{OUT} = 165\ mW + 0\ mW + 371.25\ mW = 536.25\ mW$

The junction temperature of the device never must exceed 150°C. To determine if the total power consumption exceeds the maximum junction temperature for a certain package, calculate junction temperature using the following equation:

$T_J = R_{\Theta JA} \times P_{TOT} + T_A$

In the previous example, assuming a 56-pin TSSOP (DGG) package with high-K board and no airflow, the junction temperature is:

$T_J = R_{\Theta JA} \times P_{TOT} + T_A = 64°C/W \times 0.53625\ W + 25°C = 34.32°C + 25°C = 59.32°C$

The $R_{\Theta JA}$ for all packages can be found at www.ti.com/sc/package

23 How should I generate the termination voltage?

GTLP backplanes require a high-current 1.5-V termination voltage that typically is driven from the 3.3-V V_{CC}. Typically, a 1.5-V, 7.5-A switcher provides the 1.5-V reference voltage. Currently, TI uses the LT1083CP (Linear Tech) for bus termination on our 48-bit high-drive SN74GTLPH1655 demonstration backplane. The high current is needed because there could be many open-drain GTLP outputs simultaneously sinking current on the bus, but, overall, it is less than Thevenin-terminated backplanes, such as are used with LVT devices. Unitrode also provides two devices that can be used. They offer low dropout at given current (500-mV dropout, maximum, at 5 A), ability to handle transients with tight regulation, high current capability, fast transient response, separate bias and V_{IN} pins, and 5-pin TO-220 and TO-263 packages with Kelvin sensing. The UC382 provides 3-A capacity; the UC385 provides 5-A capacity with fixed (1.5 V, 2.1 V, or 2.5 V) or adjustable output-voltage capability (see Figure 16).

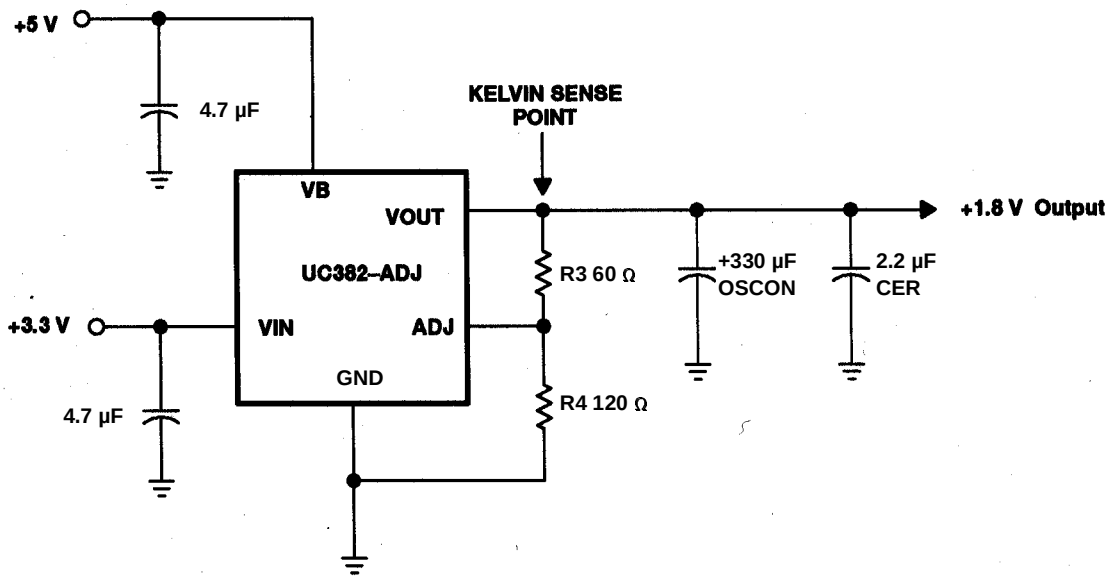


Figure 16. Kelvin-Sensing Circuit

24 Why not use Thevenin voltage dividers for termination?

Thevenin voltage dividers can be used as a termination scheme; resistors are easy to obtain and can be connected to the readily available 3.3-V power supply. However, this is not the optimal termination scheme. There are several reasons why voltage regulation is essential on GTLP backplanes:

- Static dc current through the termination - A Thevenin equivalent of two 50-ohm resistors to 3.3 V, with the backplane tied to the center connection, yields about 33 mA of constant dc current while the output driver is off (high state). Typically, terminations are the two extremes of the backplane, so the total is 66 mA for the backplane. When the device's output is on (low output state), current increases to about 112 mA because the lower termination resistor is bypassed through the 4-ohm GTLP device.

  Now, consider a 1.5-V regulated termination scheme. In the off output state, zero current flows because there is no path to ground from V_{TT} (termination voltage). While in the on state, this produces 80 mA of current. Therefore, as the output is switching states from low to high and vice versa, the average current flowing through the voltage-regulated termination is considerably lower than the Thevenin voltage-divider termination.

- Noise considerations - If the Thevenin voltage divider is tapped off the supply voltage of 3.3 V and the backplane termination voltage, V_{TT}, is taken from the center connection, any noise that is riding on the supply has now been coupled to V_{TT}. This could prove to be a problem because, if the noise is large enough, potentially it could interfere with the switching thresholds of the GTLP inputs. Voltage regulation eliminates this problem with a reliable voltage source. Ideally, a voltage regulator should be mounted at each end.

- Impedance matching – This probably is the most important reason for voltage regulation, because matching the loaded impedance of the backplane is essential to reduce or totally eliminate reflections that occur with improper termination. Using a Thevenin voltage divider is more difficult because one also has to adjust V_{TT} to be 1.5 V. The numbers used above are for V_{TT} of 1.65 V (half of 3.3 V), so the resistors have to be chosen to produce a 1.5 V V_{TT} and terminate the backplane properly. Although it sounds easy, in practice, it is not.

25 Tell me more about bus hold.

All GTLPH devices have bus hold on the A port and are described in the data sheet as "Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended." However, a note in the data sheet states "All unused inputs of the devices must be held at V_{CC} or GND to ensure proper operation." Don't these statements conflict?

No, A-port data inputs with bus-hold cells should not use a pullup or pulldown resistor, but, if required, a properly sized resistor that overrides the bus-hold cell can be used. The note refers to the control inputs, not the data inputs. The control inputs always must be tied low or high if unused or undriven and never allowed to float because the device would not operate properly. There is no bus-hold cell on any control input on any TI device.

26 Tell me more about power-up 3-State (PU3S).

Your GTLP data sheet states, "When /OEAB is low, the outputs are active." However, in the next paragraph about PU3S, the data sheet states: "To ensure the high-impedance state during power up or down, /OE should be tied to V_{CC} through pullup resistor," which means that /OE is high. This contradicts the previous statement. Should /OEAB be high or low?

The /OE should be pulled high to keep the device in the high-impedance state, even though it is featured with PU3S, which keeps the device in the high-impedance state, when V_{CC} is zero to 1.5 V, to prevent bus contention. The first statement assumes you are going to overdrive the pullup resistor when you want the outputs to be active and pull /OE to GND.

27 Should I tie GTLPH16612 control inputs to 3.3 V or to 5 V?

I need to tie the SN74GTLPH16612GR LEAB (pin 2) high for transparent operation and am not sure what voltage it should be tied to.

See the "V_I except B Port" specification in the data sheet, which is 5.5 V maximum. Confusion might arise because the GTLPH16612 has both a 3.3-V and 5-V V_{CC}. Other GTLP devices are 3.3-V V_{CC} only, and they list the nominal V_I as V_{CC} and maximum V_I as 5.5 V to show that the V_I normally is connected to 3.3 V, but you can go up to 5.5 V. In either case, you can use 3.3 V or 5 V, depending on which voltage is most convenient, but you would normally use 3.3 V for any GTLP device.

28 What do I do with unused or undriven GTLP A- or B-port I/Os?

As with any other logic device, it is important that unused or undriven inputs or inputs/outputs (I/Os) not be left floating. This prevents high current flow through the device if the input should reach the threshold level. There is no need to prevent the transistor outputs from floating as long as its input is tied to V_{CC} or GND. The following is recommended and summarized in Table 8:

- A port (LVTTL side of the device)
  - I/Os on all devices with bus hold
    Unused or undriven - No action required, bus hold will maintain last known logic state
  - Inputs on all devices without bus hold with inverted signals (currently, SN74GTLP817 only)
    Unused or undriven - Tie pin to V_{CC} with a 220-Ω up to 1-kΩ pullup resistor to maintain a logic high.
  - Inputs on all devices without bus hold with selectable true/complementary feature (currently, SN74GTLP1394 only)
    Unused or undriven - Tie pin to V_{CC} or GND with a 220-Ω up to 1-kΩ pullup resistor to maintain a logic high or low, depending on whether the device is in true or inverted mode of operation, and if signals are unidirectional or bidirectional, to keep the B port in its tied condition.

- B port (GTLP side of device)
  - I/Os on all devices
    Unused - Tie pin to ground with a 220-Ω up to 1-kΩ pulldown resistor to maintain a logic low.
    Undriven - No action required because the pin is pulled high to V_{TT} by the termination resistors.

Table 8. Control of Undriven or Unused Pins

	A I/O				B I/O	
	Bus Hold		No Bus Hold			
	True	Inverted	True	Inverted	True	Inverted
Undriven	No action required		Pull up to V_{CC}	Pull down to GND.	No action required	
Unused					Pull down to GND.	

Precharge - Each B-port I/O pin has its own precharge circuitry if the device is equipped with a BIAS V_{CC} pin. Because the precharge current is very low (<10 uA), if the pin is connected to GND, it does not reach 1-V precharge. However, other B-port I/O pins that are not connected to GND are properly precharged to 1 V.

29 Can I connect the SN74GTLPH16612GR unused I/O pins of the A ports and B ports directly to GND?

I have seen FSC's reference design and the unused pins were connected directly to ground. Per the GTLP FAQ, we cannot do that because there should be a resistor for safety purposes.

The A ports and B ports can be connected directly to GND on unused pins. Historically, there has always been a resistor used when tying the pin to V_{CC} or GND because it is required for bipolar inputs. It is not required for CMOS inputs (like those used on all GTLP devices) and the inputs can be tied directly to GND or V_{CC}. FSC's proposal to tie unused pins on both the A ports and B ports of the GTLPH16612 to GND is acceptable. Our GTLPH16612, is identical to the FSC GTLP16612, but with better B-port edge-rate slew control.

30 How does an extender card affect signal integrity?

I am designing a new card basket using GTLP and need to provide for an extender card. Should I leave it unterminated and hope it works OK, or terminate it lightly? How about terminating with a resistor in series with a capacitor? The dc pullup to 1.5 V will be taken care of on the backplane.

Leave it unterminated. There will be signal integrity problems if the extender card is used on the driver card, but the signal integrity will be OK if used on a receiver card. There will be about 20 pF extra loading and some additional line delay caused by the longer stub trace, but the receiver signal integrity should be close to what it was without the extender card, and other receiver cards should be mostly unaffected.

31 What is the transistor count for GTLP devices?

Table 9. GTLP Transistor Count

SN74GTLP	Function	Transistor Count
Medium Drive (50 mA)		
H306	Bus Transceiver	1246
817	1:6 Fanout Driver	266
H16612	Universal Bus Transceiver	3922
H16912	Universal Bus Transceiver	3325
H16916	UBT with Buffered Clock	3302
H16945	Bus Transceiver	2242
H32945	Bus Transceiver	4484
High Drive (100 mA)		
1394	Transceiver	367
H1612	Universal Bus Transceiver	3371
H1616	UBT with Buffered Clock	3371
H1645	Bus Transceiver	2062
H1655	Universal Bus Transceiver	3389
H3245	Bus Transceiver	4124

32 Can I use GTLP as a low-voltage translator?

Bidirectional voltage translations between 3.3-V LVTTL and low-voltage CMOS (LV-CMOS) are possible with GTLP devices. GTLP has a larger noise margin than general LV-CMOS interface devices and can support shift-up level conversion through the use of active transistors.

Two things must be considered:

- In the A-to-B (LVTTL to LV-CMOS) direction, V_{ref} must be within 0.6 V of the termination voltage because of the TI-OPC circuitry.
  - TI-OPC circuitry is featured on most GTLP devices (except '817, '16612, and GTL devices) and actively ports backplane energy to GND when the signal level is greater than 0.7 V above V_{ref}. This prevents large overshoots on improperly terminated or unevenly loaded backplanes during low-to-high signal transitions, which limits the subsequent undershoot that would reduce the upper noise margin. The TI-OPC circuitry is integrated into the design and cannot be deactivated, but is inactive when the B port is disabled. Except for the absolute maximum values, which must be met in all cases, there are no V_{TT} to V_{ref} voltage-difference restrictions in the LV-CMOS to LVTTL direction. Only in the LVTTL to LV-CMOS direction must V_{ref} be set within 0.6 V of the termination voltage.

- The data-sheet recommended termination voltage is limited to 1.14 V minimum and 1.65 V maximum to correspond to GTL and GTLP standards. So, these recommended data-sheet limits must be exceeded to translate at higher or lower voltages.
  - The GTLP design team reviewed the TI SPICE simulations at voltages outside the normal GTL/GTLP operating range and saw very little speed change when the termination voltage is out of the normal range. There should be no degradation in device reliability as long as the termination voltage does not exceed 2.75 V and the recommended current limit is observed. However, TI's policy is not to recommend applications outside of data-sheet recommended limits. For some TI devices, we are looking at expanding the GTLP data sheet dc limits to cover these level-translation applications.

Table 10 shows the LV-CMOS device levels and possible voltage-translation combinations using GTLP devices. The recommended GTLP device V_{ref} settings for bidirectional and unidirectional A-to-B cases are shown. Normally, V_{ref} should be equal to the LV-CMOS threshold voltage (V_t), but it is adjusted to be within 0.6 V of the termination voltage V_{CC} to prevent activating TI-OPC circuitry in a steady-state condition.

Table 10. Bidirectional or Unidirectional B-to-A Voltage Translations

LV-CMOS Device		GTLP Device
Supply Voltage (V_{CC})	Threshold Set Point (V_t)	Set V_{ref} To
2.5 V	1.25 V	1.9 V
1.8 V	0.9 V	1.2 V
1.5 V	0.75 V	0.9 V
1.2 V	0.6 V	0.6 V
1.0 V	0.5 V	0.5 V
0.8 V	0.4 V	0.4 V

Table 11 shows possible voltage-translation combinations and recommended GTLP device V_{ref} settings for the unidirectional B-to-A case where TI-OPC circuitry is inactive. Additionally, since TI-OPC circuitry is not featured in the GTLP817, GTLPH16612, or any GTL devices, this table also can be used in all cases.

Table 11. Unidirectional B-to-A Voltage Translations

LV-CMOS Device		GTLP Device
Supply Voltage (V_{CC})	Threshold Set Point (V_t)	Set V_{ref} To
2.5 V	1.25 V	1.25 V
1.8 V	0.9 V	0.9 V
1.5 V	0.75 V	0.75 V
1.2 V	0.6 V	0.6 V
1.0 V	0.5 V	0.5 V
0.8 V	0.4 V	0.4 V

A pullup termination resistor is required only if operating in the A-to-B direction and can be between 50 Ω to 1 kΩ, depending on the transition times needed for the circuit.

Normally, V_{IH} and V_{IL} are ±50 mV around V_{ref} but expands to ±200 mV at 0.4 V as V_{ref} is reduced below 0.7 V.

33 What is the voltage input range I can apply to the B port if V_{ref} is set at 0.8 V?

I'm using the SN74GTLP1394 to convert a 1.2-V GTL and 1.5-V CMOS signal to LVTTL. Signal direction always is B to A. V_{ref} is set at 0.8 V. I'm concerned that the 1.5-V CMOS signal will be too high and that it will forward-bias ESD diodes on the B-port input.

GTLP devices can be used over a range of V_{TT} and V_{ref} voltages and this application is perfectly acceptable, with no danger to the ESD diodes. In the B-to-A direction, TI-OPC is disabled and there is no restriction on V_{TT} vs V_{ref} if they are within data-sheet limits. In the A-to-B direction, V_{TT} vs V_{ref} should be maintained at less than 0.6 V.

34 Can I use GTLP as a replacement for FB+ devices?

BTL-signal-level applications are extensions of the voltage-translation application. Normally, GTLP devices are not compatible with FB+ devices, as shown in Figure 17. However, closer inspection reveals that the upper and lower noise margin is about the same, and only threshold and termination voltages are different.

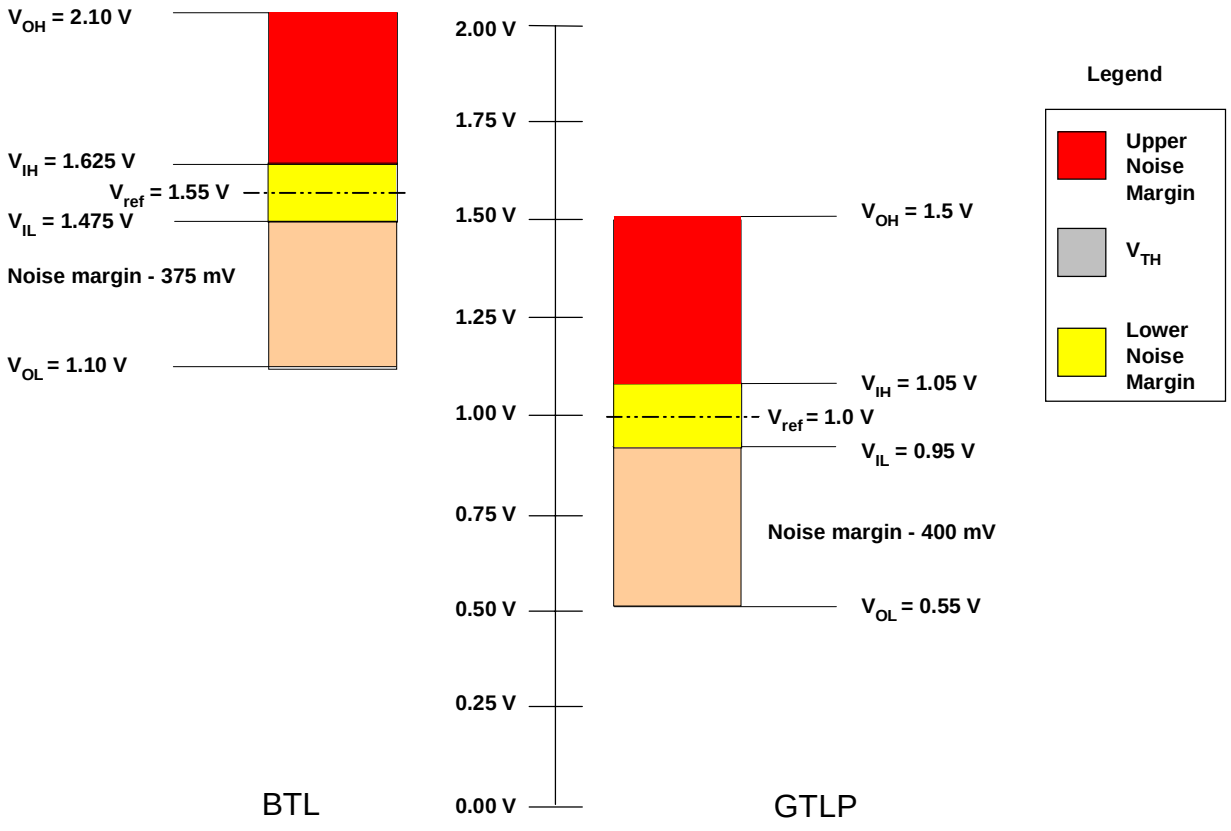


Figure 17. Comparison of BTL to GTLP Signal Levels

FB+ devices have a fixed differential input set at 1.55 V, whereas GTLP devices have a variable differential input that is set via the external V_{ref} control pin. GTLP V_{ref} is normally two-thirds of the termination voltage so that when V_{TT} is 1.5 V, V_{ref} is 1.0 V.

When GTLP devices are used in FB+ device applications, the resistor network is changed to R/3R so that V_{ref} is set at 1.575 V when V_{TT} is 2.1 V. The process is reversed easily from BTL to GTLP signal levels by changing the 3R resistor to 2R. Only high-drive GTLP devices should be used because FB+ devices also sink 100 mA of current. In actual applications, the high-drive GTLP device pulls the B-port V_{OL} lower than 1.1 V, with a corresponding increase in I_{OL}, so a higher-value termination resistor might be needed. SN74GTLPH1655 has been operated in the GTLP EVM at BTL levels with excellent signal integrity and a duty cycle of 50%.

TI's policy is not to recommend applications outside of data-sheet recommended limits, so, for some TI GTLP devices, we are expanding the GTLP data sheet dc limits to cover this application.

These expanded limits also will help in the cases where there may already be a 1.8-V or 2.0-V power supply on the board and the designer is hesitant to use GTLP because that means a 1.5-V power supply will have to be added. In this case, just use the 1.8-V power supply for V_{TT}.

35 I'm trying to determine which 3.3-V logic family will best fit my needs, and I'm still not quite clear on what choice I should make.

I'm looking for bus interface chips (e.g., 244s, 245s) to drive a backplane (tri-stateable bus). There will be five cards on the bus [one power-supply card, one microcontroller card (uC), one PCM card, and two fibre-channel interface cards (FCi)]. The bulk of the signals are between the two FCi cards and the PCM card. The FC data bus is the critical bus at 40 MHz, or maybe 80 MHz (undecided at this time). The data is sourced by one of the two FCi cards and passed to the PCM card. The data is synchronous with the system clock (40 MHz or 80 MHz) generated at the PCM card and goes to both FCi cards. It's important to maintain the phase relationship between this clock and the FC data-bus data. We will have a 72-bit unidirectional and 8-bit bidirectional bus, plus control signals. We have used FCT devices before and could get only up to about 25 MHz or so, and because this is a new design, there is a lot of flexibility on what we can choose. Other considerations include: 3.3-V power supply with some 5-V devices on the board, need industrial temperature range (prefer military) and desire high-density packages.

What device family would you recommend and why?

GTLP would work at both 40 and 80 MHz and is optimized for backplane applications. It uses a 3.3-V V_{CC} power supply and is 5-V tolerant. It is offered in industrial temperature ranges in several surface-mount and BGA packages. Military-temperature-range devices are being considered and can be requested at gtlp@list.ti.com.

What are the advantages and disadvantages?

There is excellent signal integrity at higher frequencies, pullup-resistor termination draws less power than totem-pole devices, there is no danger of bus contention on open-drain devices, and the BIAS V_{CC} pin provides for live insertion. The cost is two to three times higher than FCT or LVT, but, because these TIER-3 solutions didn't work, you need to move to a TIER-2 solution. Because you have so few cards, you could also consider a point-to-point solution with LVDS or SERDES devices. They will provide higher data throughput with lower skew, but at a higher cost. If you are comfortable with parallel single-ended devices, such as FCT, you will be very comfortable designing with GTLP, which provides a cost-effective solution at this performance node.

What devices would you recommend?

Use five SN74GTLPH16945GR (TSSOP) devices or two SN74GTLPH32945KR (LFBGA) and one SN74GTLPH16945KR (VFBGA) medium-drive devices. The SN74GTLPH16945GR is identical to the standard '16245 (48-pin 2 x 8 bit bus transceiver), except for the BIAS V_{CC} and V_{ref} pins in place of two of the V_{CC} pins. Out of the 80 possible bits, use 72 bits for the buffer (DIR is fixed) and 8 bits for the 8-bit transceiver. The minimum R_{TT} is 38 Ω for medium-drive devices and that should be acceptable for this backplane loading. If an even lower termination resistance is required to improve signal integrity or you need a slightly faster t_{pd}, the high-drive SN74GTLPH1645DGGR and/or the SN74GTLPH3245GKFR could be used. These are 100-mA versions of the medium-drive (50 mA) GTLPH16945/32945, with an edge-rate-control selection pin that allows for a slightly faster edge rate and reduced t_{pd}.

36 How do I get a GTLP data sheet?

GTLP product-preview data sheets, GTL production data sheets, and GTL1655/backplane design application reports are in the *GTL/GTLP Logic High-Performance Backplane Drivers* product information book, literature number SCED009, which can be ordered at http://www.ti.com/sc/gtlpbook or by calling the literature fulfillment center at 1-800-477-8924.

GTLP product-preview data sheets were revised in January 2001, with the latest copies available on the internet at http://www.ti.com/sc/gtlp. It is recommended that the most current data sheet be obtained after device selection.

GTLP product-preview data sheets do not contain ac specifications because the device is in development and the parameter values have not been finalized. Please contact your TI Technical Sales Representative, or the GTLP Team directly at gtlp@list.ti.com, if you need more specific information before the GTLP production data sheets are available on the internet.

GTL data sheets are available on the internet at http://www.ti.com/sc/gtl.

To conserve file space and save paper, package diagrams are included at the back of every data book and product information book, but are not included in the downloadable data sheets. Applicable package drawings can viewed, printed, or downloaded from the internet on the Logic Packaging Options page at http://www.ti.com/sc/package, under Package Drawings.

Also included on the Logic Packaging Options page are hyperlinks for Standard Packing Quantities, JEDEC Outlines, Package Thermal Data, Symbolization Guidelines, and PCB Design Guidelines.

37 When will GTLP models and devices be available?

GTLP devices are in various stages of development, with staggered HSPICE/IBIS model, preproduciton sample, and production sample availability. Please review the device summary table on the GTLP home page for model availability and the individual GTLP device data-sheet page on the Internet for device status (preview or active) or contact your TI sales representatives or the GTLP Team directly at gtlp@list.ti.com for the most up-to-date information and assistance.

38 How do I get IBIS Models?

IBIS models for all TI logic devices can be downloaded from the Internet at http://www.ti.com/sc/docs/tools/logic/models/ibis.htm.

Please ensure that the correct package and signal level (GTL or GTL+) is selected for GTL models.

IBIS models of the GTLP devices are available only at the GTLP signal levels, but all packages are included in the file, and they can be downloaded on the IBIS page.

39 How do I get HSPICE Models?

TI has pioneered new modeling technology and will offer encrypted Level-37 HSPICE models that can be downloaded directly from the internet without a confidentiality agreement. Encrypted HSPICE models for all GTLP devices will be available directly from the IBIS home page.

HSPICE models provide better device modeling capability than IBIS models. Generally, HSPICE is used for device simulation and IBIS is used for integrated board-level simulation. Unencrypted Level-37 HSPICE models require confidentiality agreements to protect TI device technology. Multiple files (device, package, process, other, readme, up to 12 total for each device) are sent for HSPICE models.

40 Why does the unencrypted Level-37 HSPICE model require a confidentiality agreement?

Confidentiality agreements are required because proprietary information that TI does not want disclosed to competitors is contained in the HSPICE model. The confidentiality agreement must be approved by both parties prior to sending a nonencrypted HSPICE model. Most GTL HSPICE models require a confidentiality agreement, whereas no GTLP HSPICE models do.

41 How should I request a confidentiality agreement?

Contact your TI Sales Representative or the GTLP technical team at gtlp@list.ti.com for assistance.

42 What does the encrypted HSPICE model zipped file contain?

The encrypted HSPICE model zipped file (for example, GTLPH16612) contains the following files:

GTLPH16612INC.INC
ASL2BSN37INC.INC
ASL2BSS37INC.INC
ASL2BSW37INC.INC
TSSOP56MOD
README.TXT
RUN.SP

Both encrypted and unencrypted Level-37 process models require a one-time patch from Avant!. for the HSPICE simulation software. Provide the following information to Jeff Brunson (jeffb@ti.com) (972-480-2481) and the patch will be provided at no charge:

Company Name:
Full Address:
Contact Name:
Contact E-mail:
Node ID:

43 If the file is encrypted, why do we need the one-time patch from Avant!?

Level 37 is a model TI created to work under HSPICE. Avant! licenses Level 37 to TI and requires TI to provide authorization to distribute the Level-37 model. This method gives TI and Avant! legal protection. The Level-37 patch is required, regardless of whether or not the model is encrypted.

The license process requires that:

- TI customer must have their own copy of Avant! HSPICE.
- TI requests that the Level-37 license be sent to the TI customer.
- The license is good for 1 year and is renewable.

44 How do I request preproduction samples?

There is no charge for preproduction samples. We generally try to limit the number to five or fewer, but you can request more if required for your application. Please contact your Texas Instruments Technical Sales Representative, the GTLP Team directly at gtlp@list.ti.com, or use the GTLP sample request form on the GTLP home page.

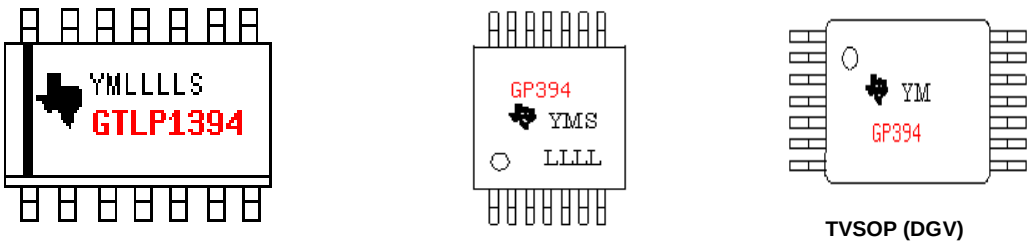
45 How do I request production samples?

Request production samples through the Extranet and your TI&Me account.

To sign up for TI&Me visit: https://www-a.ti.com/apps/ti_me/signin.asp?referer=corp

46 I requested the SN74GTLP1394, but the topside marking is GP394.

The 16-pin packages are too small to accommodate the full device name, so SN74GTLP1394 is shortened as shown in Figure 18 (not to scale or with correct pin count). Lot codes also are marked on the D and PW packages (Y = year, M = month, LLLL = lot code, S = assembly site). Only the year and month are marked on the DGV packages due to space constraints.



Narrow Body SOIC (D) TSSOP (PW) TVSOP (DGV)

Figure 18. SN74GTLP1394 Top-Side Marking

Device symbolization is explained on the Texas Instruments SLL Logic Package Options page at http://www.ti.com/sc/package under Symbolization Guidelines.

Package case assignment is found on the Package Name Rule Assignments page at http://www.ti.com/sc/docs/products/logic/package/pkrule.htm

Case A, B, and C symbolization names can be found on the Device Name Rules page at http://www.ti.com/sc/docs/products/logic/package/namerule.htm

As a convenience, GTLP device symbolization is listed in Table 12.

Table 12. GTLP Device Symbolization

SN74GTLP	SOIC	SSOP	TSSOP	TVSOP	LFBGA
Medium Drive (50 mA)					
H306	GTLPH306		GH306	GH306	
817	GTLP817		GT817	GT817	
H16612		GTLPH16612	GTLPH16612		
H16912			GTLPH16912	GL912	
H16916			GTLPH16916	GL916	
H16945			GTLPH16945	GL945	GL945
H32945					GM945
High Drive (100 mA)					
1394	GTLP1394		GP394	GP394	
H1612			GTLPH1612		
H1616			GTLPH1616		
H1645			GTLPH1645	GL45	GL45
H1655			GTLPH1655		
H3245					GM45

Updated GTLP data sheets include a new table that provides an orderable part number and top-side marking for every package combination.

47 How can I request additional technical support?

These and other helpful application reports to be released in the future are at http://www.ti.com/sc/docs/apps/logic/appnotes.html under Backplane Logic:

- Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C
- 32-Bit Logic Families in LFBGA Packages 92- and 114-Ball Low Profile Fine-Pitch BEA Package application report, literature number SCEA014
- Fast GTLP Backplanes With the GTLPH1655, literature number SCBA015A
- High-Performance Backplane Design With GTL+, literature number SCEA011A
- Basic Design Considerations for Backplanes, literature number SZZA016A

Specific technical questions not covered by the application reports, or any general question, can be sent directly to the GTLP team at gtlp@list.ti.com.

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