Application Report
SCEA028 - November 2002

VMEH22501 in 2eSST and Conventional VME Backplane Applications

Sagir Hasnain, Ernest Cox, and David Yaeger — *Standard Linear & Logic*

ABSTRACT

VMEbus™, one of the most widely used backplanes in the industry, has generated numerous end products by using third-party boards, mechanical hardware, software, and backplane driver chips. The VME double-edged source-synchronous transfer (2eSST) protocol needs an I/O driver to transmit signals along the VMEbus at significantly higher speeds than those achievable with the VME64 standard. TI addresses this need with the new VMEH22501 backplane transceiver that also can be used with older VME protocols. This application report discusses the TI VMEH22501 and its application in various VMEbus protocols.

Contents

List of Figures

List of Tables

Introduction

TI released the VMEH22501 to market in April, 2002. The VMEH22501 is the first VERSAmodule Europe (VME) backplane transceiver in the industry to target the double-edged source-synchronous transfer (2eSST) VME protocol. The 2eSST standard predicts 8× performance enhancement over the conventional VME64 standard. To achieve this performance, a new backplane driver was necessary. The definition of this device was a collaborative effort by TI and the VITA standards organization committee (the technical branch of the VITA that oversees the upkeep of the VMEbus technology). The VMEH22501 can be used in the VME64 and older VME protocols as well. The purpose of this application report is to identify key differences between the VMEH22501 and conventional VME drivers (for example, ABTE16245) and to help customers incorporate the VMEH22501 in their designs.

VMEbus Applications

The VMEbus architecture is a nonproprietary bus, and a number of third party VMEbus manufacturers are available. Affordable VME backplanes are available in different configurations and connector settings. Because there is an established base of proven hardware and software, system designers have fewer issues to deal with once they choose the VMEbus for their design.

Different industry automation and robotics applications use the VME backplane. It is used in military and aerospace control systems as well. In telecom, it is used in advanced intelligent node (AIN) and cellular telephone base stations. Medical equipment such as CAT scan and MRI imaging also use the VMEbus.

Brief History of the VME Standards

VMEbus is a flexible, open-ended bus system that originally was introduced by Motorola, Philips, Thompson, and Mostek in 1981. The intention was to define a bus system that would be independent of the microprocessor, easily upgradeable from 16-bit to 32-bit data paths, implement a reliable mechanical standard, and allow vendors to build compatible products. No proprietary rights were assigned, which enabled third-party product development.

The original VMEbus system used the master-slave architecture, with an asynchronous data-transfer scheme. In this architecture, multiple master cards and slave cards can reside in the same backplane. Both the master card and the slave card can transmit data, but the master card controls the direction of data transfer. A system controller assigns control of the bus to each master card. The maximum bandwidth was up to 40 Mbyte/s on a 32-bit data line. The VMEbus has evolved to meet the demand of higher-bandwidth data transfer over time.

VME64

In 1989, the VME64 protocol was introduced, with an 80-Mbyte/s data rate. This 2× improvement was made possible by multiplexing 32-bit address lines into a 64-bit data transfer. The VME64 requires handshaking between two control signals to transfer single-bit data. Figure 1 shows the data-transfer mechanism of the VME64 from the master to the slave.

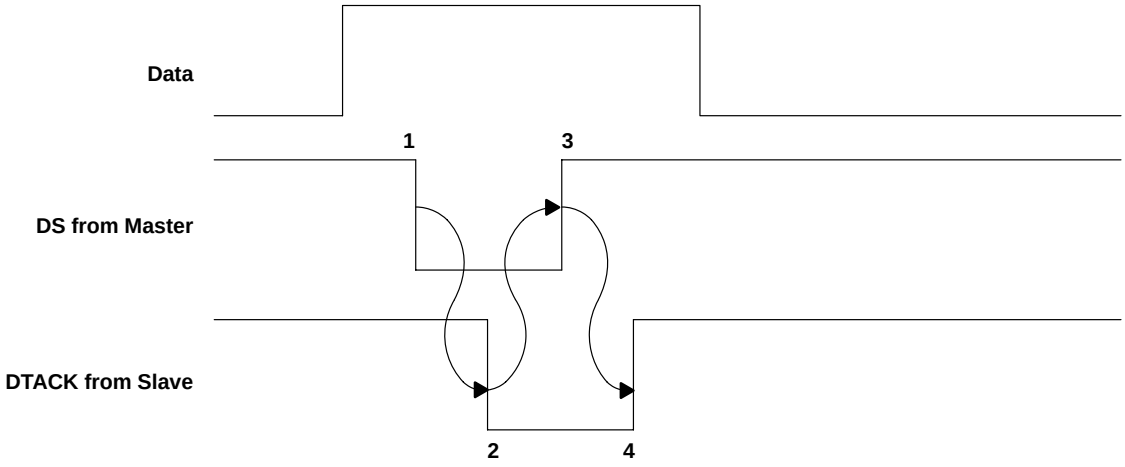


Figure 1. Timing Diagram of the VME64 Protocol

The VME64 protocol requires two control signals; data strobe from the master (DS) and data acknowledge from the slave (DTACK), to perform the handshaking. The master asserts DS low to let the slave know that data is valid. The slave acknowledges by asserting DTACK low. After receiving this response from the slave, the master asserts DS high at edge 3. The slave completes the cycle with edge 4 of DTACK. A total of four control-signal edges are required to complete a data-transfer cycle. It requires four delays through the driver, backplane, and the receiver, plus the settling time of the backplane. The specified delay is calculated on a fully loaded 21-slot backplane.

2eVME

In 1996, 2eVME provided a 160-Mbyte/s data rate. The 2eVME requires only two edges of the two control signals to complete a data cycle (see Figure 2). In effect, it can transfer data at both edges of the control signals. Even though the throughput is doubled, the bandwidth is limited by the fact that it still must wait for an acknowledgment from the receiver to complete a data cycle.

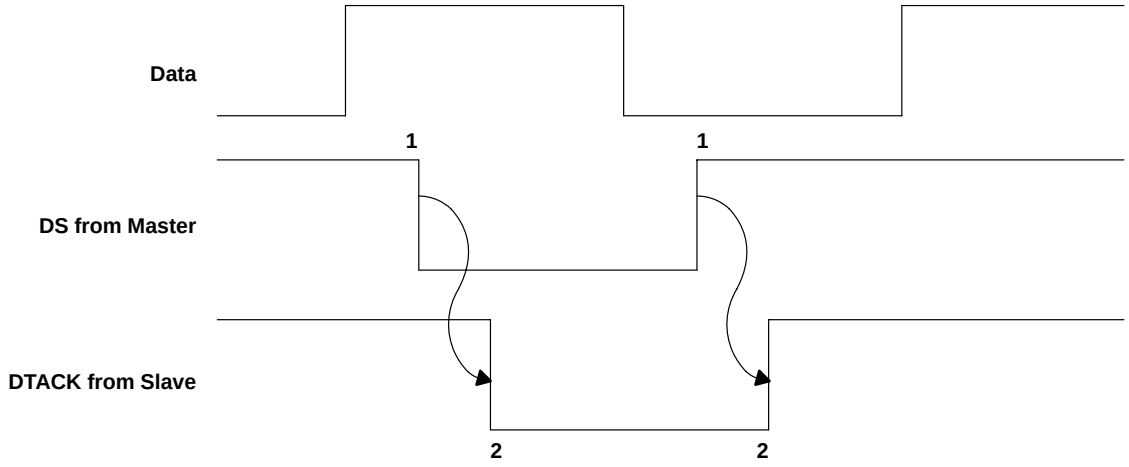


Figure 2. Timing Diagram of the 2eVME Protocol

2eSST

The new 2eSST protocol, which was introduced in 1999, calls for a minimum speed of 320 Mbyte/s. In the 2eSST, the driver does not wait for an acknowledge signal from the receiver (see Figure 3). It is, effectively, a source-synchronous type data transfer. Because both edges of the control signal are used, data throughput is virtually limited only by the skew values in the driver and the backplane. It is interesting to note that future advancements in the 2eSST need only to increase the source-synchronous data throughput by closely controlling the skew values.

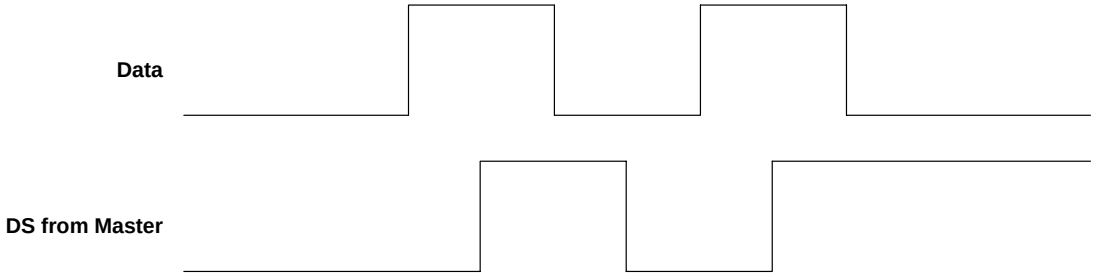


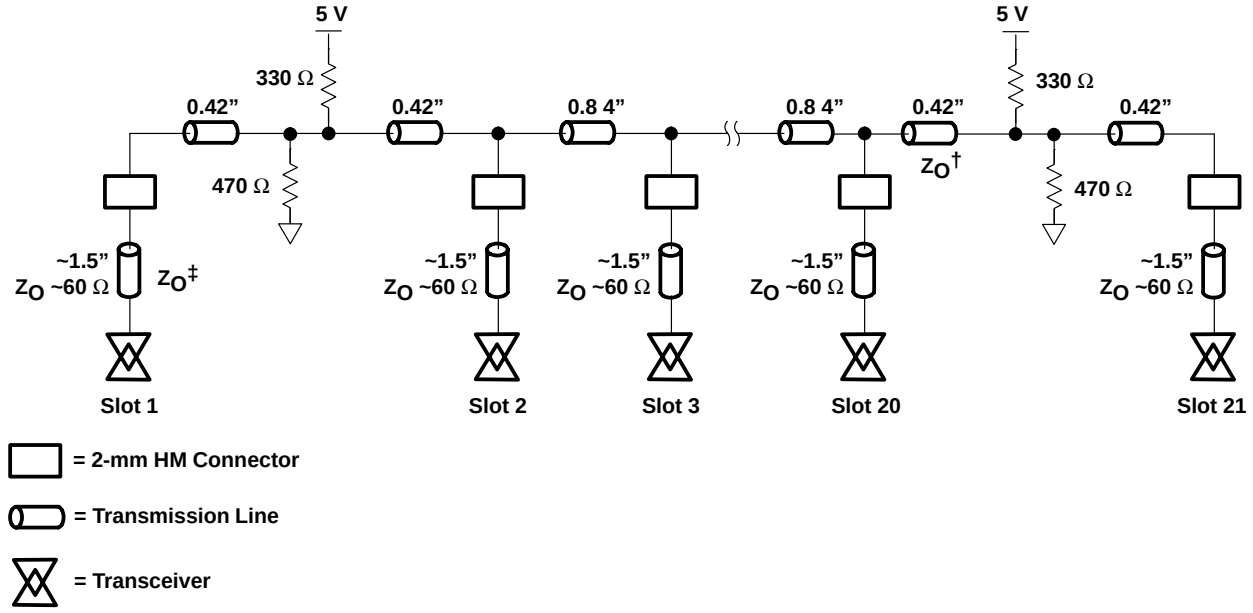
Figure 3. Timing Diagram of the 2eSST Protocol

VME320

In 1997, Arizona Digital made an important breakthrough with a new proprietary backplane, called the VME320. In the standard VME backplane, all the slots are connected through a common trace. To transfer data from slot 1 to slot 21, it traverses from slot 1 to slot 2, slot 2 to slot 3, and so on. In the VME320 backplane, each slot is connected to slot 11 in a star configuration. Data from any slot is transferred to slot 11 first, then transferred to the receiver slot. If the driver is at slot 1 and the receiver is at slot 2, data will go to slot 2 via slot 11. This star configuration effectively makes the data transfer over a point-to-point load, instead of a distributed backplane load. Data can be transferred at a much higher speed on the VME320 backplane.

Challenges For Transferring Data at Higher Frequency

The VME backplane is a double-terminated backplane. The termination is a 330-Ω and 470-Ω Thevenin equivalent between 5 V and GND. Typical spacing between the two adjacent slots is ~0.84 inch. The backplane trace impedance can vary between 45 Ω and 60 Ω, the stub impedance is about 60 Ω, and the connector impedance is about 67 Ω. The stub length is specified as 1.5 inch. These relationships are illustrated in Figure 4.



† Unloaded backplane trace natural impedance (Z_O) is 45 Ω. 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.
‡ Card stub natural impedance (Z_O) is 60 Ω.

Figure 4. Typical VME Backplane

When all the slots are populated with the daughter cards, the equivalent impedance may range from 30 Ω to as low as 20 Ω. If the backplane is lightly populated, this impedance will increase, but still does not approach the parallel combination of 330 Ω and 470 Ω (194 Ω). This results in a significant mismatch between the termination impedance and the equivalent line impedance. This mismatch causes reflections over the backplane, which results in longer settling time after the low-to-high and high-to-low transitions. In the VME64 protocol, a complete data transfer depends on mutual handshaking between the driver and the receiver. The longer settling time delays this handshaking process and slows down the data throughput. In the 2eSST protocol, data is required to be transferred at each edge of the control signal. So, it is absolutely necessary that the VMEbus signals have monotonic rising and falling edges and that the reflections do not cross the input threshold of the receiver.

The VMEbus is a flexible-length bus system. Data can be transferred from any of the 21 slots to any other slot, with the presence of any number of daughter cards on the backplane. Although the standard is defined for a maximum of 21 slots, a number of different backplane sizes, such as 5, 7, 9, 12, and 15 slots are popular across the industry. Since the reflections are inherent in the VMEbus due to improper termination, it is very difficult to design a backplane driver that will be optimized for the numerous combinations of data-transfer settings.

Connector pin assignments and the physical dimensions are defined clearly in the VME architecture. There is a specified number of GND and power pins in the connector configuration. Unlike a custom-built backplane, it is not possible to add many GND pins to reduce the EMI noise and crosstalk in high-frequency operation. The 1.5-inch stub length between the driver and connector is a concern for signal integrity.

SN74VMEH22501 to Meet the Challenge

The VITA committee approached TI because the existing logic drivers were not capable of driving the VMEbus with monotonic transient-wave switching. The development of the VMEH22501 started with prespecified electrical requirements, including drive strength and rise/fall times. The objective was to perform incident-wave switching, instead of waiting for the reflection to settle down. Another important criterion was to achieve minimum system skew over the VME backplane by controlling the driver ac drive across the variations of process, temperature, and operating V_{CC}. TI devised a process and design that met the VITA requirements.

The SN74VMEH22501 is a combination of 8-bit universal bus transceivers (UBT) and two-bit transceivers, with split LVTTL ports for control and diagnostic monitoring purposes. For the UBTs, 3B1 to 3B8 are the VME-side I/O ports and 3A1 to 3A8 are the LVTTL-side I/O ports. For the two split LVTTL-port transceivers, 1A, 2A are the LVTTL-side input ports, 1Y, 2Y are the LVTTL-side output ports, and 1B, 2B are the VME-side I/O ports (see Figure 5). The UBTs allow transparent, latched, and flip-flop modes of data transfer. It operates at 3.3-V V_{CC}, but can accept 5.5-V input signals at both VME and LVTTL ports. The LVTTL 3A ports and Y outputs have 26-Ω series resistors to reduce the line mismatch on the daughter-card LVTTL side. With the help of I_{off}, power-up 3-state, and precharge (BIAS V_{CC}) features, the VMEH22501 supports live insertion.

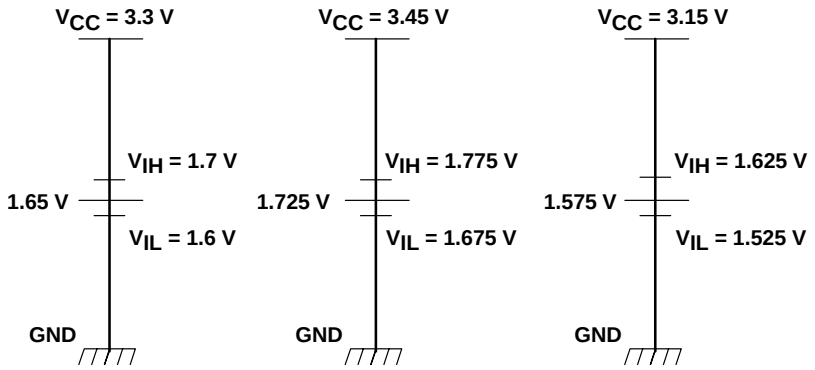


Figure 5. Input Threshold Levels of the VMEH22501 at Different V_{CC} Levels

NOTE: Please see the TI application note, *Logic in Live Insertion Applications With a Focus on GTLP* [2] for an explanation of I_{off}, precharge circuits, and live insertion. For information about the power-up 3-state circuit, please see the TI application report, *Power-up 3-State Circuits in TI Standard Logic Devices* [3].

The VME-side input port has tightly controlled input-switching thresholds of 1/2 V_{CC} ±50 mV for increased noise immunity. In the VMEbus, this input threshold is a clear advantage over the normal TTL or LVTTL type inputs, where V_{IH}(min) is 2.0 V and V_{IL}(max) is 0.8 V. Because the input threshold follows the $V_{CC,}$ data transfer is more immune to the fluctuation of supply voltage, as opposed the ABTE family, where the input threshold is fixed at 1.5 V ±100 mV.

To optimize performance, the VMEH22501 has been designed into a distributed VME backplane. The OEC™ circuitry, for output edge-rate control, helps reduce reflections as well as electromagnetic interference. The OEC circuitry and high ac drive strength are instrumental in achieving the goal of incident-wave switching. The VME port can source and sink very high transient currents, which effectively helps to overdrive the reflection on the backplane during transition.

The VMEH22501 is offered in TSSOP (DGG), TVSOP (DGV), and VFBGA (GQL) packages. The flow-through architecture of DGG and DGV packages helps to minimize the stub length on the daughter card (see Figure 6). Due to connector pin layout (refer to Appendix A), the GQL package gives more flexibility to the board designer for multilayer board routing (see Figure 7), and is most effective in reducing simultaneous-switching noise.

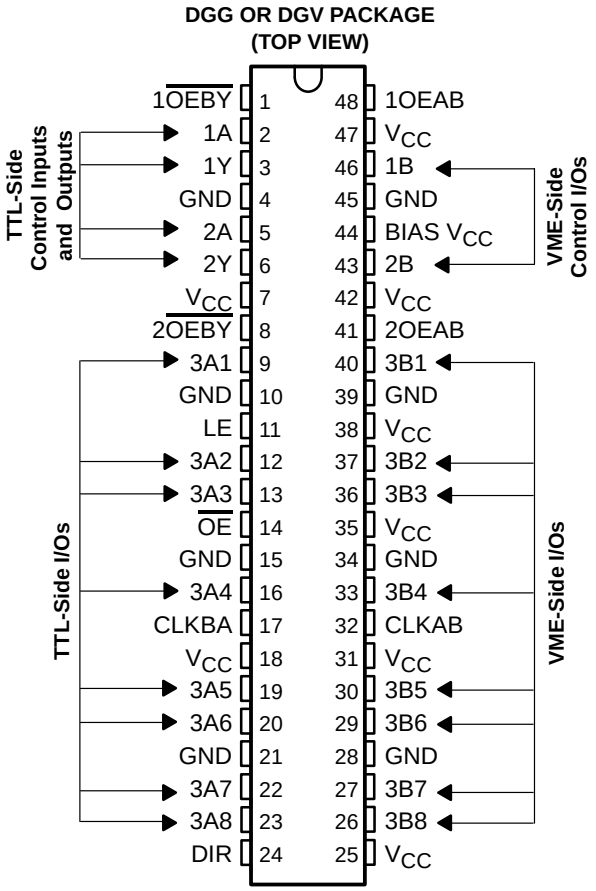
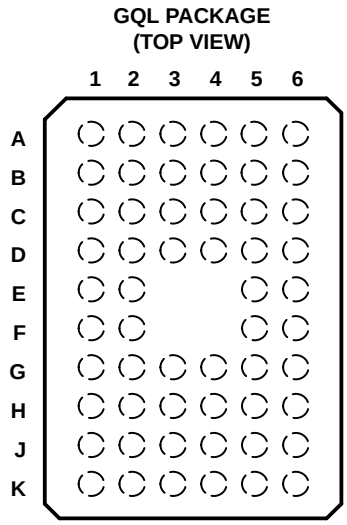


Figure 6. VMEH22501 Pin Assignments for DGG and DGV Packages



terminal assignments for GQL Package

	1	2	3	4	5	6
A	1$\overline{OEBY}$	NC	NC	NC	NC	1OEAB
B	1Y	1A	GND	GND	V_{CC}	1B
C	2Y	2A	V_{CC}	V_{CC}	BIAS V_{CC}	2B
D	3A1	2$\overline{OEBY}$	GND	GND	2OEAB	3B1
E	3A2	LE			V_{CC}	3B2
F	3A3	$\overline{OE}$			V_{CC}	3B3
G	3A4	CLKBA	GND	GND	CLKAB	3B4
H	3A5	3A6	V_{CC}	V_{CC}	3B6	3B5
J	3A7	3A8	GND	GND	3B8	3B7
K	DIR	NC	NC	NC	NC	V_{CC}

NC – No internal connection

Figure 7. VMEH22501 Pin Assignments for the GQL Package

AC Timing Data

In the VMEH22501 data sheet, ac data are provided both with a lumped load and with the distributed backplane loads. Figure 8 provides a comparison of propagation delays from the LVTTL side (A port) to the VME side (B port) for three different loading conditions. It is obvious that low-to-high and high-to-low transitions are more balanced in the backplane loads than in the lumped load. The balanced high-to-low and low-to-high propagation delays of the backplane driver help reduce the overall system skew over the backplane.

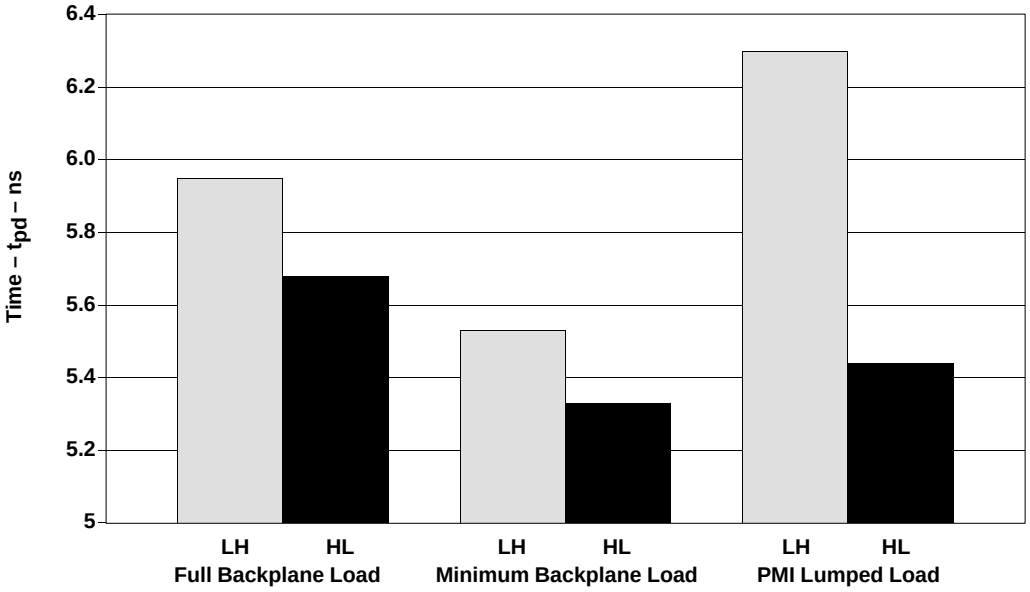
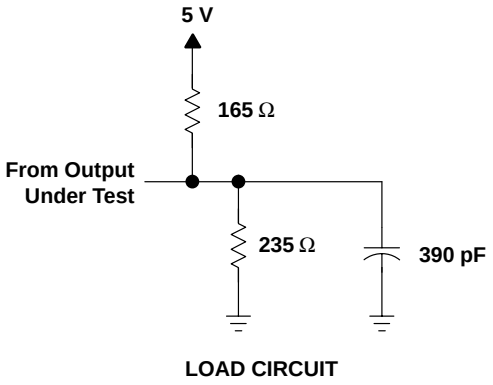


Figure 8. Propagation Delay of VMEH22501 Across Different Loads

NOTE: In Figure 8, the Full Backplane Load means all the slots of a 21-slot VME backplane are populated with daughter cards and the driver is at slot 1. Minimum Backplane Load means only slot 1 and slot 21 are populated and the driver is at slot 1. The PMI Lumped Load is the data-sheet load shown in Figure 1 of the VMEH22501 data sheet.

Peak AC Current

Figure 9 shows the peak ac current (measured in actual silicon under nominal process material) from the VME port of the VMEH22501 while driving the load circuit. This specific load was chosen to represent the peak ac current in the actual VME bus at the most severe loading condition. The 165-Ω and 235-Ω resistors are the dc equivalent of the two Thevenin terminations on the VME bus line. To obtain the capacitor value, a number of simulations were performed on a 21-slot conventional VME backplane. The goal was to find a lumped-capacitor range that makes the VMEH22501 VME port source and sink the same amount of ac peak current as it would do in the actual VME backplane under the most severe condition. It was found that the edge rate of the driver had a profound effect on the capacitance value chosen. A driver with a relatively faster edge rate (ABTE16245) did not see the same amount of capacitance as the driver with a slower edge rate (VMEH22501). The most heavily loaded case was driving from slot 11 on a fully loaded 21-slot backplane. In this loading condition, the equivalent capacitance for the ABTE16245 and the VMEH22501 were ~150 pF and ~390 pF, respectively.



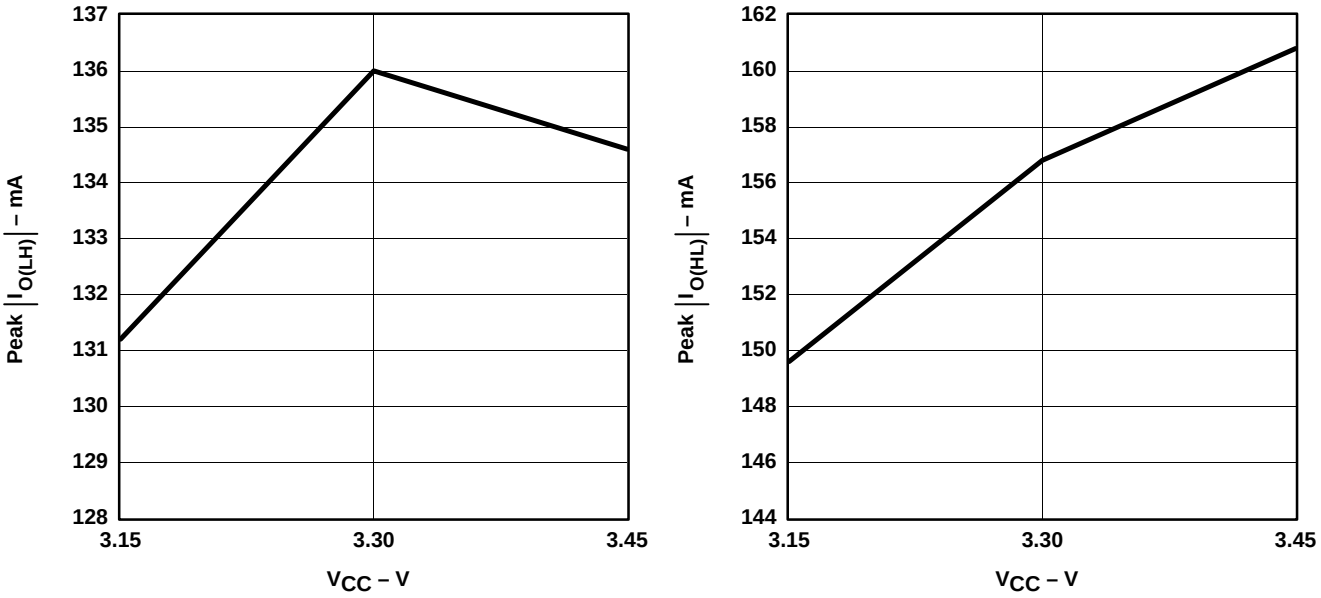


Figure 9. Peak AC Source and Sink Current of VMEH22501

Laboratory measurements show that the peak ac source and sink currents at 3.3-V V_{CC} are 137 mA and 157 mA, respectively. This excess ac current during the transition helps to overdrive the reflection and achieve incident wave switching. However, the steady-state dc current is much lower than this peak value. With the same load and nominal material at 3.3-V V_{CC}, the steady-state source current is 3.28 mA, and the sink current is 28.4 mA.

Why the VMEH22501 is Compatible with the Older VME Protocols

One of the key features of the VMEH22501 is the backward compatibility. In older VME backplanes, some of the control lines were terminated with pullup resistors only. In the 2eSST, all the lines are Thevenin terminated. To maintain backward compatibility, the VME side I_{OL} specification of the VMEH22501 is maintained at 64 mA. This high current allows the faster high-to-low transition, with pullup termination.

In older VME backplanes, some data bits are only 16 bits wide. It always is a challenge to populate the same backplane with daughter cards that are both 16 and 32 data bits wide, simultaneously. The dual existence of both 16-bit and 32-bit data lines causes a serious system skew problem because of the loading difference in different lines. The VMEH22501 was tested in this scenario. With tightly controlled process skew and high drive strength, it was able to overcome this serious system skew problem.

In most of the VME applications, the backplane driver and receiver operate at 5-V V_{CC}. Although the VMEH22501 operates at 3.3-V V_{CC}, it can handle 5-V input at both TTL and VME ports. This is why there will not be any voltage-level-translation problem interfacing with existing VME transceivers, as long as the output and the input signals are TTL/LVTTL compatible.

Comparative Simulation Among Several Backplane Drivers

Comparison Over a VME Backplane

A comparative study was performed in HSPICE simulation to see the signal integrity of a number of backplane drivers on the VME backplane. The backplane configuration and size are similar to that shown in Figure 4. The backplane trace impedance is 55 Ω, the stub trace impedance is 60 Ω, and the connector model is 2-mm HM. In Figure 10, the signaling rate is 20 Mbps. The signal is measured at the receiver at slot 10, while the driver is at slot 11, under full-load condition. The ABTE, LVT, and ALVT drivers show the rising-edge glitch at the transition region of the LVTTL receiver, which disappears with the VMEH22501. The overall signal integrity also looks better with the VME chip. The ABTE16245 switches at about 4 V because the operating V_{CC} is 5 V.

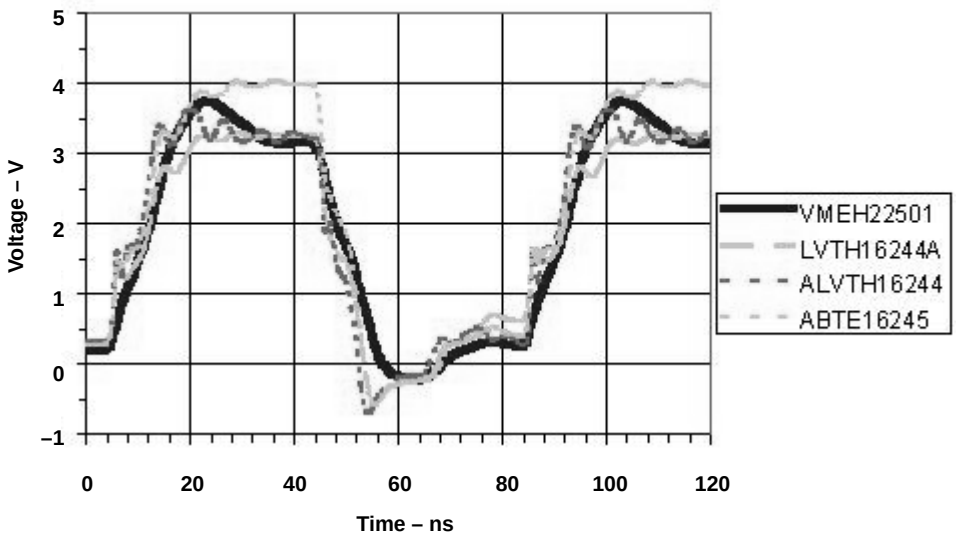


Figure 10. Signal Integrity of Different Drivers on a VME Backplane

Comparison of Rise and Fall Edges

The VME port of the VMEH22501 has very controlled rising and falling characteristics during transition, compared to the existing VME backplane drivers. Figure 11 compares the rise and fall time of the above devices with a resistive load in HSPICE simulation. The load is 500 Ω between the driver output and GND. The slower edges of the VMEH22501 help to maintain good signal integrity as shown in Figure 10.

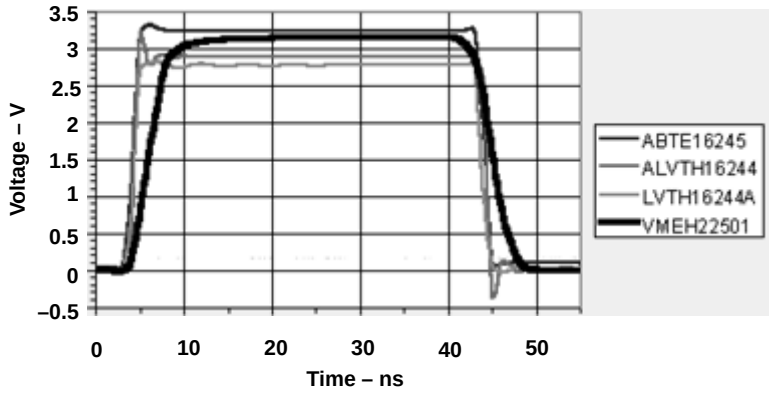


Figure 11. Rise- and Fall-Time Comparison of Various Backplane Drivers

Comparison Over a Custom-Built Backplane

Many applications use a custom-built backplane with closely matched terminations, other than that specified in the VME protocol. The most feasible type of termination with a push-pull type backplane driver is the Thevenin termination. The lower limits of the resistor values are set by the dc drive capability of the driver and the input threshold level of the receiver.

Figure 12 shows a standard backplane used for HSPICE simulation to compare the performance enhancements of several drivers due to better impedance matching. The connector type is 2-mm HM on this 10-slot backplane.

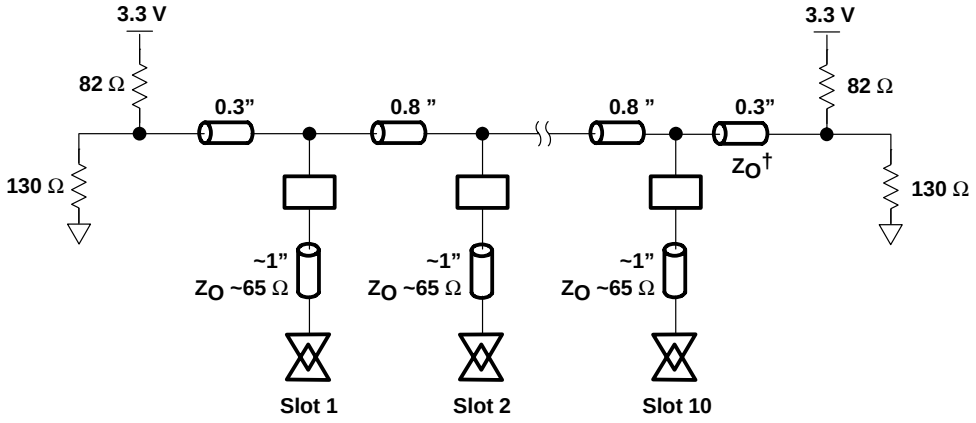


Figure 12. Standard Backplane With Closely Matched Terminations

Figures 13 and 14 compare the signal integrity on the backplane in Figure 12 at a 100-Mbps data rate. This specific loading condition is simulated, with all the slots populated with daughter cards and the driver at slot 1. Signal integrity at the adjacent slots of the driver is worst in this loading configuration. The LVT driver has nonmonotonic transition below the LVTTL receiver input threshold level (V_{IH} = 2.0 V). The nonmonotonic transition of the VMEH22501 enables glitch-free signaling, even with LVTTL-type receiver input.

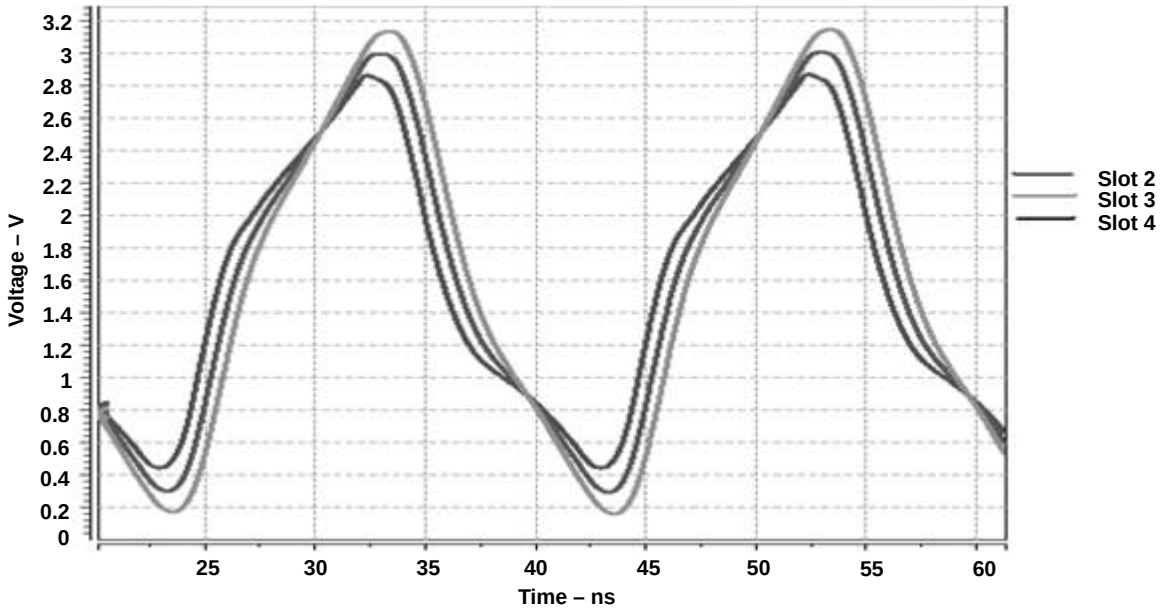


Figure 13. Signal Integrity With the VMEH22501

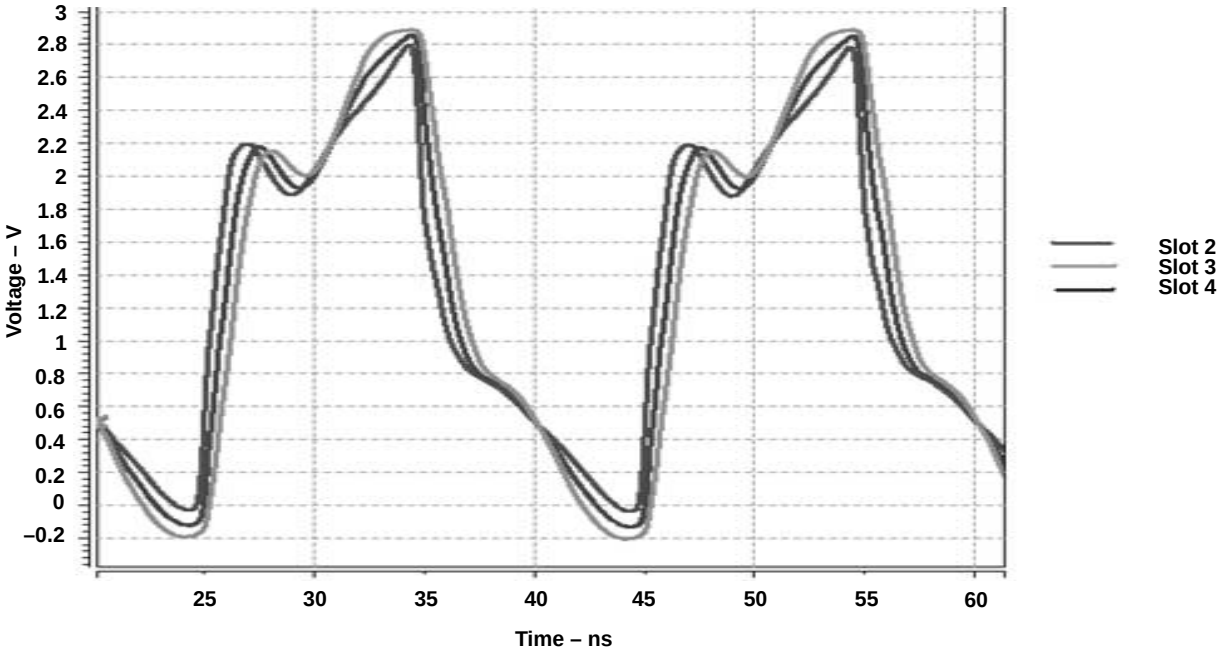


Figure 14. Signal Integrity With the LVTH16244A

Evaluation Board

To test actual silicon performance of the VMEH22501, a set of daughter cards was designed and manufactured (see Figure 15). Each card has three VMEH22501 chips to accommodate 24-bit data lines, the data-strobe lines, and some other controlling-signal lines. The cards used standard 6U dimensions, with 5-row, 160-pin P1 and P2 connectors (see Appendix A). The 24-bit data lines were selected to comprehend the worst crosstalk and electromagnetic interference (EMI) noise on the VMEbus. These are D00 to D15 from the P1 connector and D16 to D23 from the P2 connector. The controlling signal lines are DS0, DS1, DTACK, and BBSY.

NOTE: Please see the VITA web site at http://www.vita.com for detailed pin functionalities of the P1 and P2 connectors.

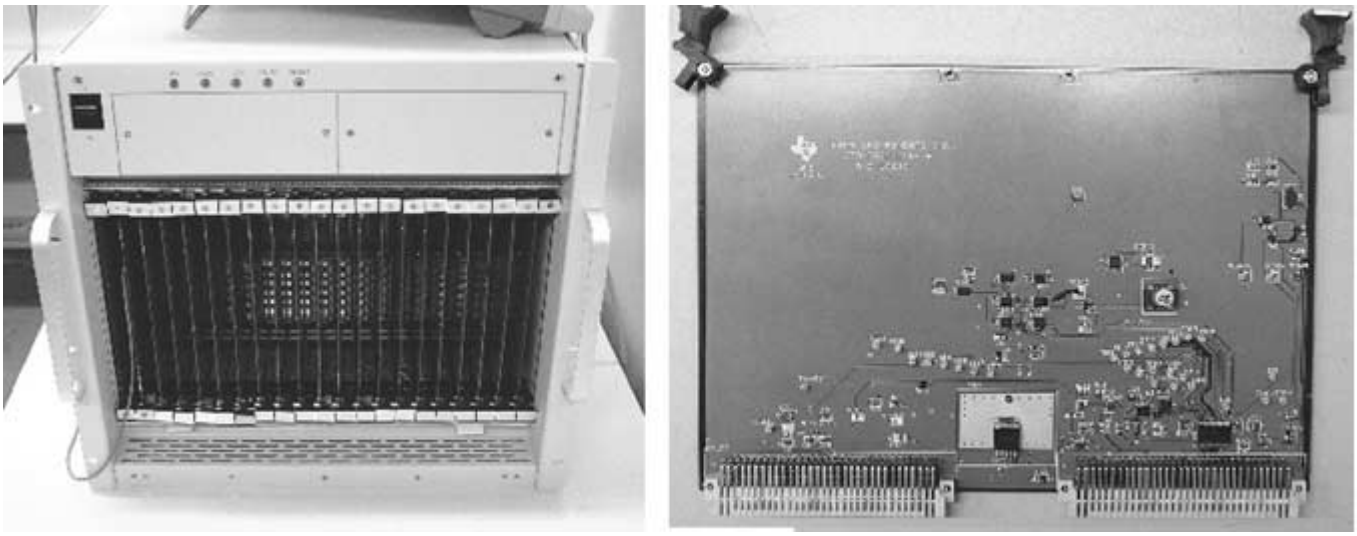


Figure 15. 21-Slot VME Backplane and the Evaluation Board Used in Silicon Tests

The daughter cards were inserted in a 21-slot off-the-shelf VME backplane to emulate the 2eSST and the VME64 protocols. Signal integrity, crosstalk, and EMI noise were observed at the key areas of concern. In the 2eSST, the target data rate is 320 Mbyte/s over a 64-bit data line. This is equivalent to a 40-Mbps data rate on a single data line for the 2eSST protocol. The VME64 mode was tested at a maximum speed of 20-Mbps data rate per line.

The VITA committee identified the following cases as the possible candidates for the worst signal integrity on the VMEbus. Because only the nominal material for the VMEH22501 was used to build the evaluation boards, the process variations were not tested with the silicon. The boards were tested for extensive correlation between the silicon data and the simulation. Based on a very good correlation, the simulation data were extended across the process, voltage, and temperature. Please consult TI web site at www.ti.com/sc/VME for more detailed simulation results.

Signal Integrity at 20-Mbps Data Rate

A series of tests were performed at 20 Mbps at different slots for the cases described in Table 1. In all the cases, the worst-possible signals were observed. For example, when the driver is at slot 11, the worst reflection should be at slot 10 and at slot 12. Figures 16 and 17 represent the signal integrity for case 1 and case 7, respectively. Case 1 has the heaviest ac load because it is driving from the middle and all the slots are occupied. At 20-Mbps data rate, case 7 is considered to generate the worst-possible valley due to ring back from the overshoot. With the VMEH22501, this valley did not go below 2.7 V (see Figure 17).

Table 1. Proposed VITA Test Configurations

Case	Backplane Loading	Driving Slot	Silicon Material
1	All slots	11	Weak
2	All slots	1	Weak
3	All slots	1	Strong
4	All slots	11	Strong
5	Slots 11 and 12	11	Strong
6	Slots 1 and 21	1	Strong
7	Slots 1, 11, and 17–21	1	Strong

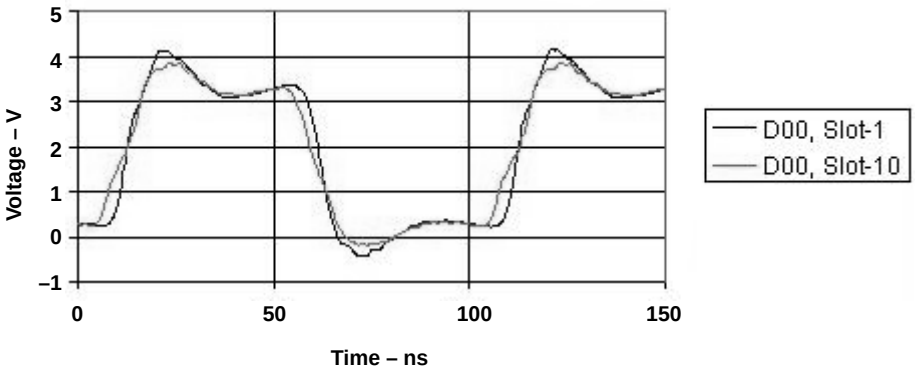


Figure 16. Signal Integrity for Case 1, 20 Mbps

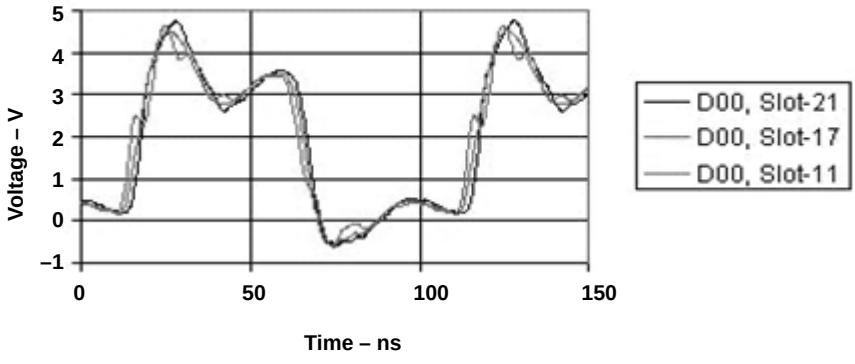


Figure 17. Signal Integrity for Case 7, 20 Mbps

Time Delay Over the Backplane

Because the loading condition varies on the VME backplane, system designers need to know the variation of flight time across different loading conditions. This information is needed to plan the overall system skew. To compare the time delay over the backplane, the full-load case 2 and the minimum-load case 6 rising waveforms were compared. In Figure 18, the data of full-load case and minimum-load case are not represented at the same time reference. The signal delay was measured at 1.65 V. The flight times to travel 16.8 inches were 6.8 ns and 3.74 ns for case 2 and case 6, respectively.

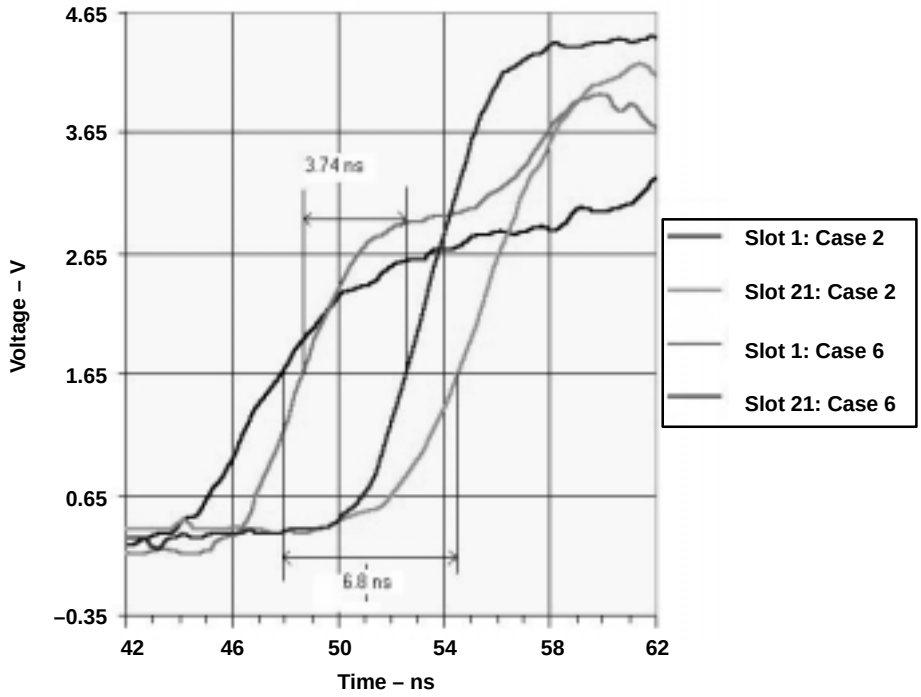


Figure 18. Time-Delay Comparison Over a Full-Load and Minimum-Load Cases

Signal Integrity at 40 Mbps

Because the 2eSST protocol calls for a maximum data rate of 320 Mbyte/s (or, equivalently, 40 Mbps per data line), measurements of the cases in Table 1 were repeated at a 40-Mbps data rate. In general, all the cases showed good signal integrity. Case 2 and case 7 show the worst signal integrity among all the cases (see Figures19 and 20). Under full-load conditions, driving from slot 1, the signal at slot 2 maintains monotonic rise and fall edges right at the transition region. As the signal propagates, it improves (as seen in slot 11 and slot 21). Case 7 creates a nonmonotonic glitch in the rising wave at 2.5 V, which is essentially above the switching threshold.

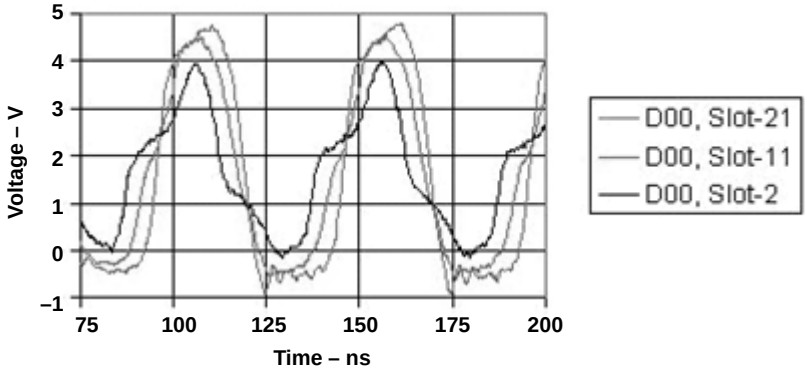


Figure 19. Signal Integrity for Case 2, 40 Mbps

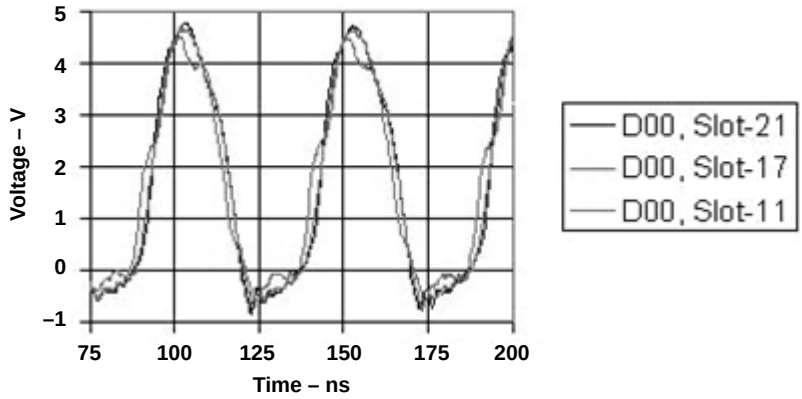


Figure 20. Signal Integrity for Case 7, 40 Mbps

It is noticeable that the high-level signal starts transitioning to low level at ~4.5 V. This indicates that the signal did not have enough time to settle down before starting another transition. A direct comparison between Figure 17 and Figure 20 can be made in this regard. The nonmonotonic transition between 1-V and 2-V levels ensures glitch-free data transfer.

Interference at BBSY

The BBSY signal in the VME protocol is used to assert control of the bus to each card. It asserts a low signal if the bus is occupied. Due to its physical position in the P1 connector, it is susceptible to interference noise. At 20-Mbps data rate, case 1 generated the worst noise performance at the BBSY line (see Figure 21). At a 40-Mbps data rate, case 2 showed the worst noise at BBSY (see Figure 22).

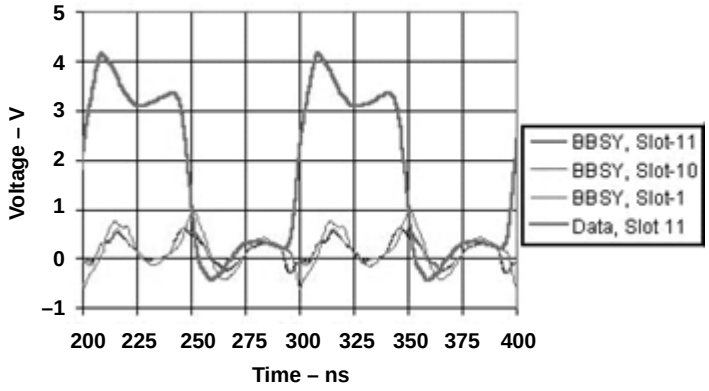


Figure 21. Interference at BBSY Line for Case 1, 20 Mbps

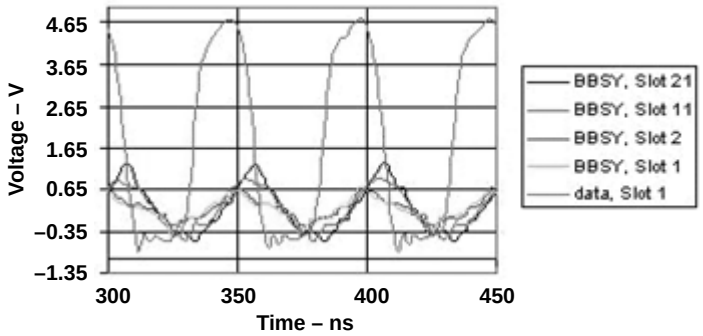


Figure 22. Interference at BBSY Line for Case 2, 40 Mbps

For case 1 of 20-Mbps data rate, the worst-case noise at BBSY reaches 1 V. At case 2 of 40-Mbps data rate, the noise peak exceeded 1 V, due to more transition at a given time. Because V_{CC} is 3.3 V, the noise peak is below the input threshold (1.65 V) in both cases.

Crosstalk at D04

Due to the absence of sufficient ground shield pins in the connectors, crosstalk is a major concern for the VMEbus when multiple data lines are switching at higher frequencies. To observe the effects of crosstalk at one data line due to the signal switching at other data lines, the D04 data bit in the P1 connector was driven with inverted phase data, relative to all other data bits. Please refer to Appendix A to see the physical location of the D04 data bit in the P1 connector. Case 2 in Table 1 generated the worst crosstalk noise. Figures 23 and 24 show the signal integrity at D04 and D00 data bits at different slots at 20 Mbps and 40 Mbps, respectively.

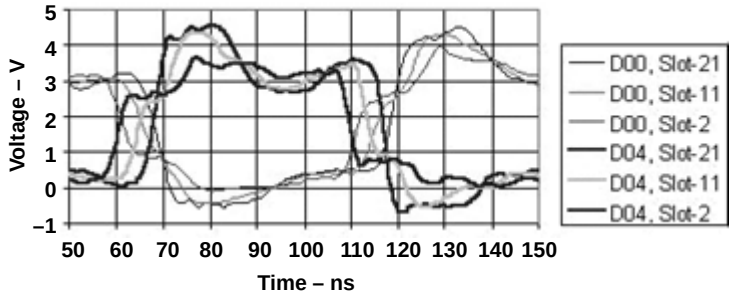


Figure 23. Crosstalk for Case 2, 20-Mbps Data Rate

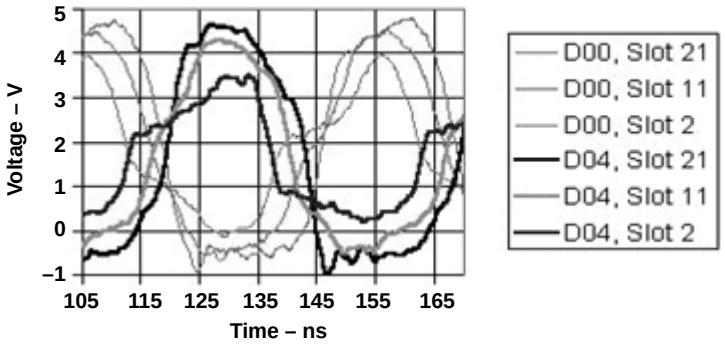


Figure 24. Crosstalk for Case 2, 40-Mbps Data Rate

From Figures 23 and 24, it can be seen that the signal at slot 2 is most affected by the crosstalk noise. This is because the driver is at slot 1 under full load conditions. In all the slots, the worst-case nonmonotonic behavior is outside the 1-V to 2-V region.

Some Suggestions to Improve Signal Integrity

The stub length from the VMEH22501 to the connector should be as short as possible. To reduce system skew, stub lengths should be matched for all the data and control bits. Populating both sides of the daughter card may help optimize the stub lengths.

The 5-row connector and the 3-row connector specifications correspond completely. All the data and control lines have the same pin positions in these two connectors. This allows easy migration from a 3-row connector to a 5-row connector. If a 5-row connector is used instead of a 3-row connector, some bypass capacitors between the supply pins and GND of the external rows (at the back of the connector) will help in reducing some ground-bounce noise.

Using multiple bypass capacitors to stabilize the supply line also is recommended. To reduce high-frequency noise, a small capacitor (0.1 μF, or less) for every two V_{CC} pins on the VME side of the VMEH22501 is recommended. The capacitors should be as close as possible to the V_{CC} pins. An additional large capacitor close to the chip helps maintain the dc level of the power-supply line.

If live insertion is required, a specific power-up sequence is recommended to utilize the full live-insertion capability of the VMEH22501. The power-up sequence should be GND, BIAS V_{CC}, OE pin, I/O ports, then V_{CC}.

Conclusion

The VMEH22501 will enhance the performance of the VMEbus, regardless of the version of the protocol. Because careful consideration was given during the design phase and because it was designed into the distributed VME backplane, the VMEH22501 performs satisfactorily at the highest speed targeted by the 2eSST protocol. The VITA committee acknowledges that this chip should meet the much-awaited need of the support silicon for the 2eSST protocol. This transceiver has been specifically cited for meeting the 2eSST transceiver requirement in chapter 3, rule 3.1 of the 2eSST draft.

References

1. VMEbus Frequently Asked Questions (FAQ) at http://www.vita.com
2. *Logic in Live Insertion Applications With a Focus on GTLP* Application Report, literature number SCEA026
3. *Power-Up 3-State Circuits in TI Standard Logic Devices* Application Report, literature number SZZA033
4. *From BLT to 2eSST—A Look at the Evolution of VMEbus Protocols,* by John Rynearson

Glossary

6U	A physical dimension of a printed circuit board (PCB). The 6U board dimension is 6.3×9.16 inches.
ABT	Advanced BiCMOS technology logic family
ac drive	Transient drive current through a driver output pin when the driver output is transitioning from one logic state to another
Daughter card	A PCB board used to communicate through different slots of a backplane
dc drive	Steady-state drive current through a driver output pin when the driver output logic state is at a fixed high or low logic state
Flight time	Time needed for the signal to traverse from one end of the backplane to the other end
LVT	Low-voltage technology
LVTTL	Low-voltage transistor-transistor logic
OEC™	Output edge-rate control, a trademark of TI
PCB	Printed circuit board
TTL	Transistor-transistor logic
VITA	VMEbus International Trade Association—an incorporated, nonprofit organization of vendors and users having a common market interest
VME	VERSAmodule Europe
VMEbus™	The VMEbus™ logo is a trademark of VITA. This trademark was developed to highlight the use of VMEbus in embedded systems.

Appendix A. VMEbus Connector-Pin Assignment

Table 2. P1/J1 Connector-Pin Assignment and Signal Descriptions Under VME64x

Pin Assignment for the VMEbus P1/J1 Connector					
Pin	**Row z**	**Row a**	**Row b**	**Row c**	**Row d**
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR*	D09	GND
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	–V1
7	MMD	D06	BG1OUT*	D14	–V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus	GND	AM3	A19	RsvBus
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus	IACKIN*	SERA	A17	RsvBus
22	GND	IACKOUT*	SERB	A16	+3.3V
23	RsvBus	AM4	GND	A15	RsvBus
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus	A06	IRQ5*	A13	RsvBus
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus	–12 VDC	+5VSTBY	+12 VDC	GND
32	GND	+5 VDC	+5 VDC	+5 VDC	VPC

Table 3. P2/J2 Connector-Pin Assignment and Signal Descriptions Under VME64x

Pin Assignment for the VMEbus P2/J2 Connector					
Pin	**Row z**	**Row a**	**Row b**	**Row c**	**Row d**
1	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
2	GND	UsrDef	GND	UsrDef	UsrDef
3	UsrDef	UsrDef	RETRY*	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND
32	GND	UsrDef	+5 VDC	UsrDef	VPC

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265