

# Functional Safety FIT Rate, Failure Mode Distribution SN74LVC1G08-Q1

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Single 2-input positive-AND gate

## Functional Block Diagram



Figure 5. Positive Logic

FIT IEC TR 62380 / ISO 26262-11 (1)	Per 10 <sup>9</sup> Hours (FIT)		
	SON	SOT-23	SOT-70
Package			
Total FIT Rate	3	4	4
Die FIT Rate	2	2	2
Package FIT Rate	1	2	2

FIT Siemens Norm SN29500 (2)			
Table	Category	Ref FIT $\lambda_{ref}$	Ref Virtual Tj $\theta_{vj,1}$
3	CMOS Logic	5 FIT	45 C

Failure Modes	Failure Mode Distribution (%)
Driver output stuck-at fault	25%
Output open (HIZ)	20%
Output functional – out of specification timing or voltage	45%
Short circuit any two pins	10%

## **(1) Failure Rate, Mission Profile and Failure Modes Distribution**

The failure rate and mission profile information come from reliability modeling for Integrated circuits in Reliability data handbook IEC TR 62380 and ISO 26262 Part 11

Mission Profile: Motor Control from Table 11

Power dissipation: 1 mW

Climate type: World-wide Table 8

Package factor lambda 3 Table 17b

Substrate Material: FR4

EOS FIT rate assumed = 0

## **(2) Reference failure rate, Virtual (equivalent) junction temperature**

The reference failure rate and virtual junction temperature come from Siemens Norm SN29500-2 tables 1-5.

Failure rate for user mission profile is calculated using the reference failure rate and virtual junction temperature and following the calculation information in SN29500-2 section 4.

The failure mode distribution estimation comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment. The failure rates listed reflect random failure events and do not include failures due to misuse or over stress.

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