Application Report
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System Considerations For Using Bus-hold Circuits To Avoid Floating Inputs

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ABSTRACT

When designing systems that include Complementary Metal-Oxide-Semiconductors (CMOS) devices, designers must pay special attention to the operating condition in which all of the bus drivers are in an inactive, high-impedance condition (tri-state). Unless special measures are taken, this condition can lead to undefined levels and, thus, to a significant increase in the device's power dissipation. In extreme cases, this leads to oscillation of the affected components, which has a negative effect on both the reliability — in terms of both lifetime and the functionality — and the electromagnetic compatibility of the entire system. This application report addresses various circuit design features that minimize these problems. The main purpose of this application report is to present a novel bus-hold circuit that TI has integrated into a wide range of modern bus-interface devices. This bus-hold circuit is the ideal way to meet the demands that are mentioned in this application report to ensure the functional reliability of a system.

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1 Introduction

In recent years, CMOS technology has become the technology of choice for development and subsequent production of highly integrated (VLSI) circuits because of the high complexity and low power consumption that can be achieved with these types of circuits. Also, the technology has proved itself with less complex devices, such as the AHC and AC logic families, as well as with the LVC , ALVC , AVC and most recently in the AXC logic families developed for use with lower supply voltages. Furthermore, it is possible for important parameters, such as the propagation delay time and the drive capability, to achieve properties similar to those found in the bipolar circuits that previously dominated this field. In this respect, the particularly powerful SN74ABT and SN74LVT Bipolar & CMOS (BiCMOS) devices, which combines the strengths of CMOS circuits (low power consumption) with those of bipolar circuits (lower propagation delay time and greater drive capability), deserve a mention.

When using these integrated CMOS and BiCMOS devices, the designer must also consider certain properties of these devices that the specification sheets deal with only briefly, if at all. For example, this includes the behavior of the input stages of these components when no defined logic level is established.

2 Device Overview

2.1 Behavior of CMOS Input Stages

The input stage of a CMOS circuit consists of an inverter (see Figure 1) that decouples the following internal circuit from the external signal source. Due to the high degree of voltage amplification, this stage regenerates the voltage swing and the rise time of the incoming signal.

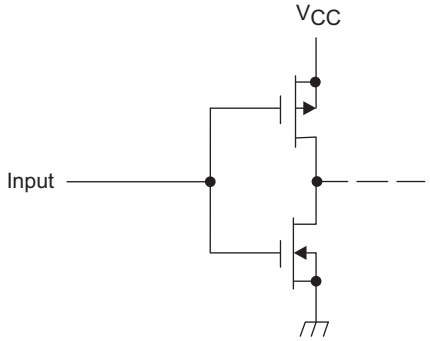

Figure 1. Input Stage of a CMOS Circuit

If there is a valid logic level at the input (the gates of the MOS transistors) of such a circuit, the P-channel transistor conducts if the input is a low level, and the N-channel transistor conducts if the input is a high level. In either case, the complementary transistor is turned off, so that, in both cases, no current flows through the transistors. This results in low power consumption when the CMOS circuits are at rest.

On the other hand, if an input voltage between these defined logic levels ($V_T < V_I < V_{CC} - V_T$; with V_T = threshold voltage of the transistors) is applied to this input, both transistors are partially conducting, leading to an increase in the device's supply current. Figure 2 shows the supply current in relation to the input voltage for AHC and AC devices. In AHC devices, the supply current reaches a peak value of I_{CC} = 2 mA.; while in the faster AC devices, currents of about 5 mA can be expected. Accordingly, the device's power consumption also increases, so that, with undefined logic levels, the advantages of CMOS circuit technology are not realized.

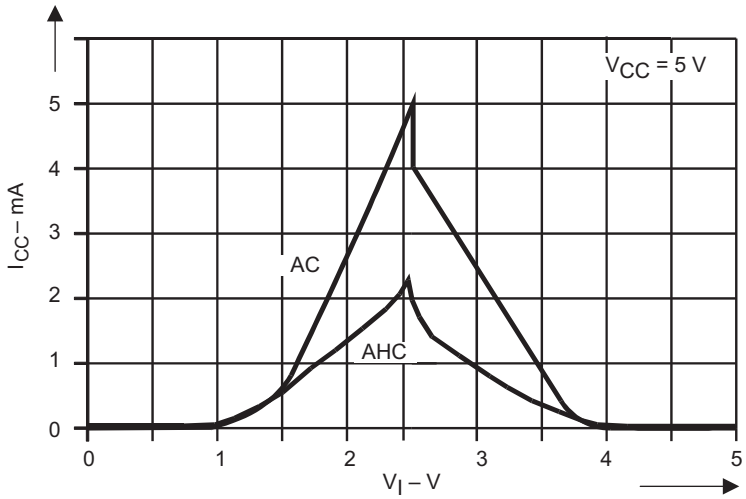

Figure 2. Power Consumption of CMOS Input Stages vs Input Voltage

The effects shown in Figure 2 are typical of all CMOS circuits. This phenomenon also must be taken into account when dealing with Very-Large-Scale Integration (VLSI) circuits, such as microprocessors or memory devices.

Furthermore, CMOS device data sheets recommend the slowest possible rise time for the input signal to ensure optimum functioning of components. However, slowly rising edges cause fast integrated circuits to malfunction and can, in extreme cases, lead to destruction of the circuit. Figure 3 shows an inverting buffer stage with the parasitic inductances of the package leads (L_P) and the capacitive load (C_L) at the output.

For example, consider the input voltage rises from a low to a high level and crosses the threshold voltage V_T. The output switches abruptly from high to low due to the high voltage gain, and discharges C_L. The discharge current causes a voltage drop at the package inductance of the ground terminal, which raises the internal ground potential of the integrated circuit. This means the voltage difference between the input and the internal ground potential decreases, giving the appearance of a decrease of the input voltage.

In the mean time, if the input slew rate is slow and the input voltage has not risen sufficiently, the output stage then switches to the opposite state, and the same process repeats. This process repeats periodically, with the periodicity of the oscillation determined by the device's propagation delay time. In fast logic circuits, the oscillation is over 50 MHz. For more information, refer to the *Solving CMOS Transition Rate Issue Using Schmitt triggers* white paper.

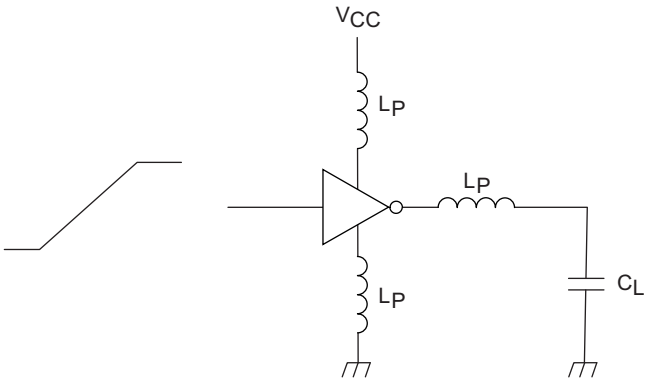

Figure 3. Parasitic Components Causing Circuit Oscillation

Figure 4 shows the oscillation at the output of a CMOS circuit whose input is triggered by a signal with a rise time of t_r = 200 ms. The rise and fall times of this order must be taken into account if, for the operating conditions discussed below, special circuit design techniques are not incorporated to ensure defined signal levels and slew rates.

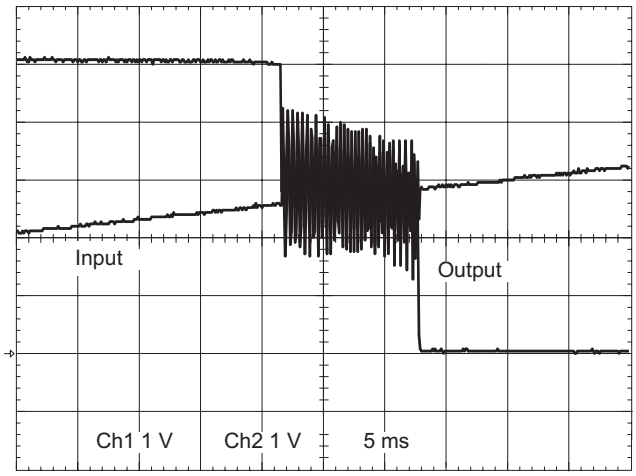

Figure 4. Oscillation at the CMOS Output Whose Input Signal has a Rise Time t_r = 200 ms

In addition to a significant increase in system noise, which compromises the system's electromagnetic compatibility, the circuit's power dissipation rises unacceptably. In MOS circuits, the fact that the transistor's resistance increases as the temperature rises becomes an advantage because this often prevents the circuit from overloading. In contrast with bipolar devices, the transistor's current gain increases as the temperature rises. This also applies to BiCMOS devices, such as the SN74ABT and SN74LVT series. Since there are no factors that can reduce power dissipation, these circuits are often overloaded when they oscillate. Experience shows that permanent degradation of devices can be expected if the oscillation lasts for several seconds.

3 Device Description

3.1 Problems Posed by Bus Systems

If unidirectional transmission lines are involved only, the previously mentioned phenomenon of increased power dissipation and oscillation can be ignored. With unidirectional transmission lines, there is a driver circuit that is always active at one end of the line, and ensures defined logic levels (see Figure 5).

Figure 5. Unidirectional Transmission Line

Bus systems (see Figure 6), in which transmission is bidirectional between individual stations, special attention must be given to the operating condition in which all of the tri-state output bus drivers are in an inactive, high-impedance state in a tri-state device.

Since there isn't a driver to impose a defined logic level on the lines, an undefined voltage level develops which is determined by the leakage currents of the connected components. In the literature, this state is called floating inputs. In the case of WidebusE circuits with 16 channels and AC technology, with a supply voltage of V_{CC} = 5 V, the supply current rises to I_{CC} = 16 × 5 mA = 80 mA (see Figure 2). Under this condition, the power consumption of this component increases to 400 mW, which is no longer considered as low power consumption.

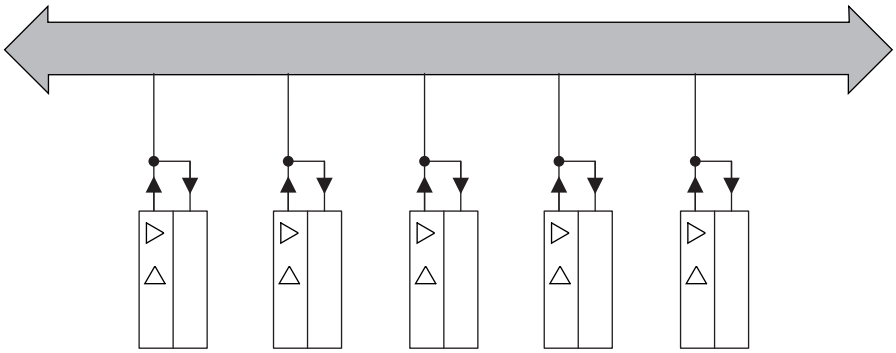

Figure 6. Bidirectional Transmission Line of a Bus System

4 Avoidance of Undefined Levels in Bus Systems

4.1 Avoidance of Undefined Levels Via Appropriate Bus Control

A simple way to prevent an undefined logic level in bus systems is to ensure, via appropriate control of the bus, that the duration of the inactive state (tri-state) is short so that harmful voltages cannot build up. The advantage is that this method does not involve any additional costs from using special components.

If we first consider a single device and assume that the maximum leakage current, I_{OZ}, of a tri-state output in the high-impedance state is 10 µA (see Table 2), and that the input and output capacitance, C_S, of the integrated circuit plus the parasitic capacitance of the connection lines (which are related to this particular component) amount to about 20 pF, the voltage on an inactive line drifts away from the defined logic level at a rate that can be calculated using Equation 1.

$$\frac{dV}{dt} = \frac{I_{OZ}}{C_S} = \frac{10\ \mu A}{20\ pF} = 0.5\ V / \mu s \quad (1)$$

If a drift away from the logic level of a maximum of 1 V is permitted, so that the supply current of the affected input stage has not yet risen too sharply (see Figure 2), the bus may remain in an inactive state (3-state) for a maximum of 2 µs. Usually, more than one device is connected to a bus. When several components are connected to a bus, both their leakage currents and their capacitances are added, and the time constant calculated in equation 1 does not change.

In the data sheets, semiconductor manufacturers give conservative values for the leakage current, I_{OZ}. When determining these values, the leakage current is measured at an ambient temperature of T_A = 25°C, and the maximum values that are to be expected at the operating limits are then calculated. However, according to semiconductor physics, the leakage current doubles with every 10°C rise of T_A.

Thus, if T_A rises from 25°C to 125°C, the leakage current rises by a factor of 210 = 1024. However, this fundamentally correct assumption leads to considerably higher values than the values that are measured in practice. Accordingly, one can assume that typical output leakage currents are smaller than the specification sheet limits by an order of magnitude or more.

Another method to avoid undefined logic levels in inactive buses involves the last active bus-interface device remaining active (monitored by suitable control logic) until another bus driver takes over control of the line. The PCI bus uses this method, whereby inactive bus phases of any length can be bridged without the extra cost of adding components.

4.2 Pullup Resistors

Another way to ensure a defined level during a bus's inactive phase is to tie the lines to the supply voltage or to the ground potential via resistors R_P (see Figure 7). This connection pulls inactive lines to a defined high or low logic level.

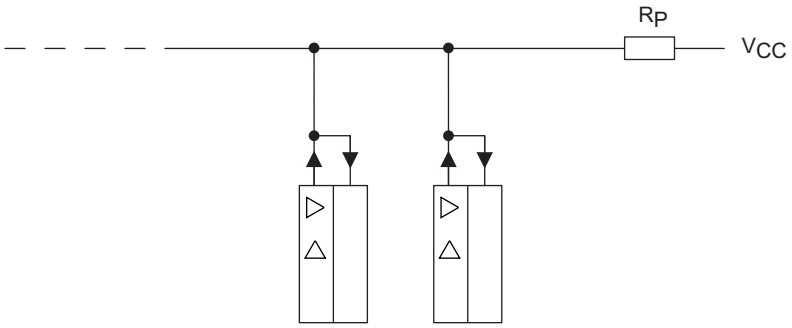

Figure 7. Creating a Defined Level Using Pullup Resistors

Getting the correct impedance for the resistors is not always easy. The resistors should not significantly increase the system's power dissipation; therefore, high-impedance resistors are required (R_p = 10 kΩ to 50 kΩ). The low leakage current of CMOS circuits would permit that.

On the other hand, fast logic circuits need short rise times, t_r, at the inputs to avoid unwanted oscillations. As mentioned previously, this can lead to system malfunction and, possibly, degradation of components. The desired pull-up or pull-down resistance, R_P, can be calculated using:

$$R_p = \frac{t_r}{2.2 \times C_S \times n} \quad (2)$$

where

- n = number of devices connected to the line

Modern logic circuits and corresponding VLSI circuits demand input signals, whose slew rate is $\Delta t/\Delta V$ is less than 10 ns/V. In the case of a supply voltage of V_{CC} = 5 V, corresponding to a signal rise or fall time ($t_{r/f}$) of 5 ns, resistance R_p can be calculated using Equation 3.

$$R_p = \frac{50\ \text{ns}}{2.2 \times 20\ \text{pF} \times 10} \approx 110\ \Omega \quad (3)$$

This outcome is unacceptable if using modern bus-interface circuits — whose primary advantage is a low quiescent current consumption. These resistors consume more current than the logic circuit itself. After all, many logic circuits are not capable of providing the output current needed for such a low-impedance load.

4.3 Bus-Hold Circuit

A better solution is to ensure a defined level for inactive bus lines via bus-hold circuits (see Figure 8). These circuits feed back the output signal of a non-inverting buffer circuit to the input via the resistor R_F. This creates a bistable circuit (latch).

To understand how the circuit works, assume that an active bus driver has switched the line to high level. This means a high level also exists at the output of the bus-hold circuit buffer. Thus, no current flows via the feedback resistor R_F. The leakage currents of the circuit, which are in the micro-ampere region, determine power consumption of the bus-hold circuit. If the output of the bus driver in question changes to the inactive state, the bus-hold circuit holds the high level via the feedback resistor R_F, so that now, apart from leakage currents, no current flows through. Only during the transition time of the line from high to low, or vice versa, unavoidable current spikes occur in the CMOS bus-hold circuits. However, the dynamic power dissipation is several orders of magnitude less than when using pull-up resistors as described previously.

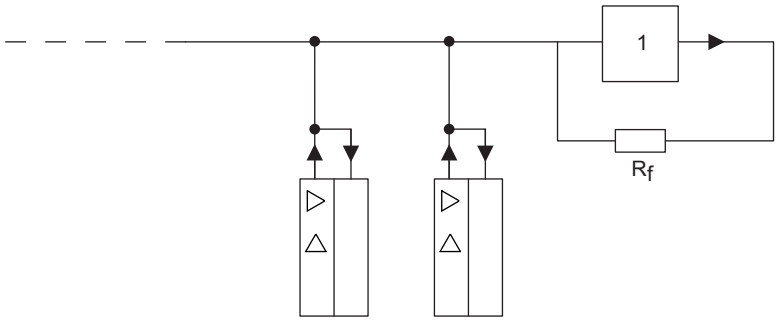

Figure 8. Bus With Bus-Hold Circuit

This kind of circuit can be built simply by using a non-inverting buffer circuit, such as the SN74AHCT541, if, as noted previously, the outputs are fed back to the inputs via resistors R_F. The propagation delay time of these components is, in this case, of secondary importance. Whether the CMOS-compatible version (SN74AHC541) or the TTL-compatible version (SN74AHCT541) is used depends on the switching thresholds of the bus-interface device. The impedance of the feedback resistor R_F is decided, taking into account the fact that the voltage drop V_R at the resistor still ensures a sufficient logic level, even at the maximum leakage current I_{OZ} to be expected from the connected devices. Here the number of bus drivers (n) connected to the bus obviously plays a part. In making the calculation it is assumed that, due to its low load, the output voltage of the buffer circuit used in the bus-hold circuit corresponds to the potential of the supply lines (V_{CC} or GND). Thus,

$$R_f \leq \frac{V_r}{I_{OZ} \times n} \tag{4}$$

If we assume that ten bus drivers are connected to the bus line and the output leakage current of the bus drivers is I_{OZ} = 10 µA, and, a voltage drop of Vr = 1 V at the feedback resistor R_F is allowed, the resistance R_F is:

$$R_f \leq \frac{1\,V}{10\,\mu A \times 10} = 10\,k\Omega \tag{5}$$

With this circuit technique, no charging of line capacitance is required. Instead, only the most recent logic level is held and problems relating to signal rise times are no longer expected. Accordingly, the circuit can be designed with a considerably higher impedance and a lower power consumption, than with the technology previously described in Section 4.2.

5 Integrated Bus-Hold Circuit

Due to all the reasons discussed from the previous section, a defined logic level must be ensured on bus lines in the high-impedance state. Thus, it makes sense to integrate bus-hold circuits in the inputs of bus-interface devices. Doing so means designers no longer have to concern themselves with the problem, and additional components are not needed to ensure defined logic levels under all operating conditions. Overall, this improves the reliability of the whole system.

All newly developed bus-interface device inputs have a bus-hold circuit. The additional letter H in the type designation indicates this feature. An AXC device has no bus-hold circuit, while an AXCH device has an additional bus-hold function. The same concept applies to the ALVT, LVT, LVC, AVC, ABT circuits versus ALVTH, LVTH, LVCH, ALVCH, AVCH and the ABTH circuits.

The additional cost of the bus-hold function in bus-interface devices is not excessive. Figure 9 shows the simplified input circuit found in the modern CMOS and BiCMOS families. The input signal is amplified in the Q1 and Q2 inverter. Simultaneously, this stage decouples the following internal circuit from the exterior of the device. The actual bus-hold circuit consists of transistors Q3 and Q4. The signal, after again being inverted, going through a total of 360 degrees, then returns to the circuit's input.

From the resulting feedback, the two inverters create a latch that continuously attempts to reach one of the two stable (high or low) states. If there is a high level at the circuit input, the output of the second inverter is also high. Therefore, P-channel transistor Q3 conducts. If the input voltage of the integrated circuit drops for any reason, a current is supplied via this transistor, which counteracts any further drop of the line voltage. If, conversely, there is a low level at the circuit input, the N-channel transistor Q4 conducts and compensates for the leakage current of the interface devices connected to the bus.

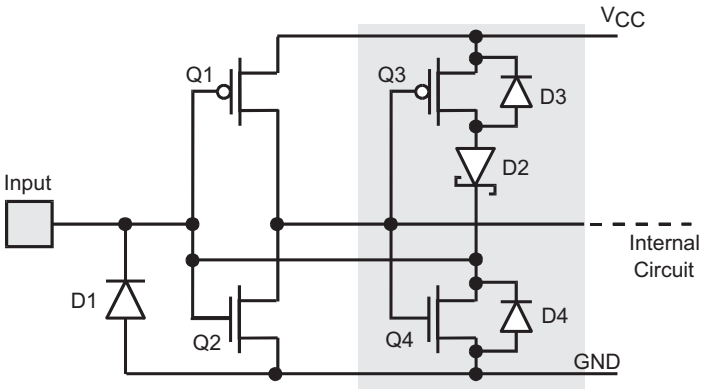

Figure 9. Simplified Circuit Diagram of Bus-Hold Circuits

Transistors Q3 and Q4 in the bus-hold circuit compensate for both their own leakage currents and for those of the connected circuits. Otherwise, the circuit should be loaded as little as possible. As a result of this, these transistors have a comparatively high forward resistance when in the on state. (Rdson = 5 kΩ). Figure 10 shows the input characteristics of typical bus-interface devices with the bus-hold function.

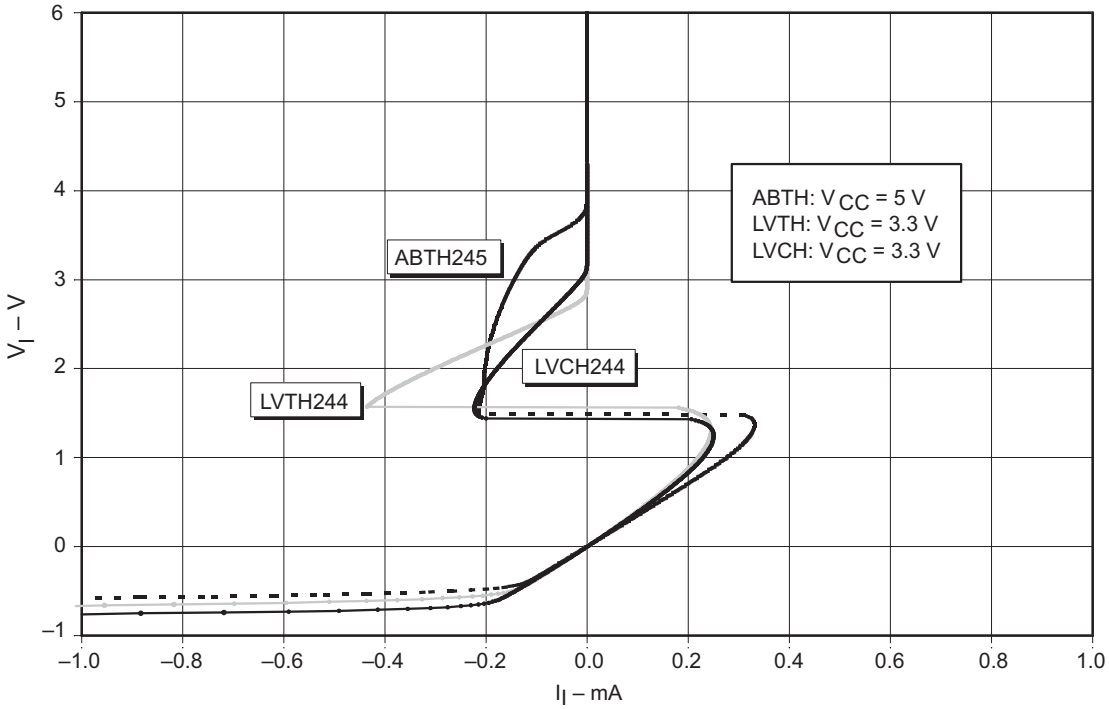

Figure 10. Characteristic Input Curve of Bus-Interface Devices With the Bus-Hold Function

The switching threshold of bus-hold circuits is about 1.5 V in the devices depicted in Figure 10, matching the switching threshold of the appropriate logic circuits. If the input voltage is below this level, the N-channel transistor Q4 conducts (Rdsontyp = 5 kΩ). This transistor also remains conducting, even when the input voltage falls below 0V. If the input voltage drops below –0.7 V, clamping diode D1 conducts, which protects the circuit against destruction due to electrostatic discharge (ESD) and limits negative undershoot stemming from line reflection. Above the cited threshold voltage, P-channel transistor Q3 conducts, pulling the line level to the high potential. Diode D2 in Figure 9 prevents the parasitic diode D3 parallel to transistor Q3 from conducting if the input voltage has a higher positive value than the supply voltage.

For example, this last case might occur when signals with a voltage swing of 5V control the bus-hold circuit, which is operated by a supply voltage of V_{CC} = 3.3 V. This also ensures that the bus-hold circuit remains at the high-impedance state when the supply voltage is off. Figure 10 shows the influence of this diode in that the bus-hold circuit already becomes high impedance at markedly less than 3.3 V. In the case of ABTH devices, whose typical high level also is about 3 V despite a supply voltage of 5-V, it would not make sense for the bus-hold circuit to pull the potential significantly above this level. Accordingly, as Figure 10 shows, additional circuit features limit the rise in voltage.

6 Application Information

6.1 Additional Load Caused by Bus-Hold Circuits

The influence of, and the additional load caused by, the bus-hold circuits can be investigated using the example in Figure 11. In this example, a digital signal processor (TMS320C6xx), eight bus-interface devices (SN74LVCH245A) with the bus-hold function, and one bus-interface device (SN74AHC245) without the bus-hold function are connected to a system bus.

Semiconductor manufacturers still supply devices with tri-state outputs, but without the bus-hold function under discussion. These include, among others, microprocessors, such as digital signal processor TMS320C6xx, or integrated circuit SN74AHC245 used in this example. In some applications this leads to a combination of different types of logic circuits. Figure 11 exemplifies bus systems where circuits with and without the bus-hold function are combined with each other.

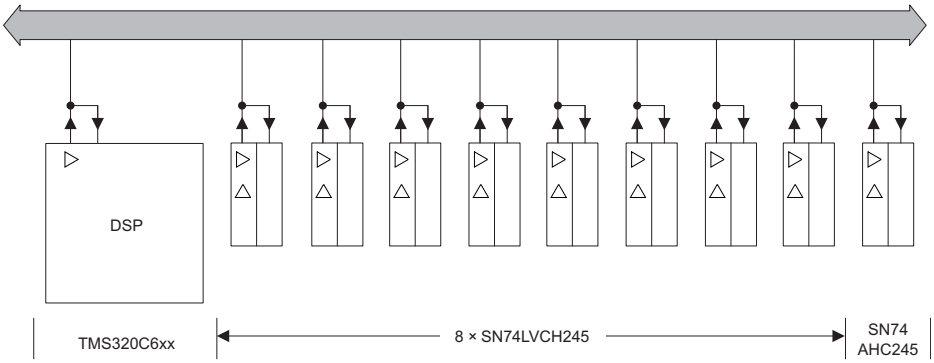

Figure 11. A Simple Bus System

Refer to Table 1 for input and output details about the SN74AXCH8T245 device.

Table 1. Specifications of the Tri-State Outputs With Bus Hold: SN74AXCH8T245

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	Output high voltage	I_{OH} = 12 mA	3 V	2.3		V
V_{OL}	Output low voltage	I_{OL} = 12 mA	3 V		0.7	V
$I_{BH(Hold)}$	Bus-hold sustaining current (hold)	V_I = 0.8 V	3 V	135		μA
		V_I = 2 V	3 V	–135		μA
$I_{BO(Hold)}$	Bus-hold overdrive current (hold)	V_I = 0 to 3.6 V	3.6 V		480	μA

Refer to Table 2 for input and output details about the SN74LVCH245A device.

Table 2. Specifications of the Tri-State Outputs With Bus Hold: SN74LVCH245A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	Output high voltage	I_{OH} = 12 mA	3 V	2.4		V
V_{OL}	Output low voltage	I_{OL} = 12 mA	3 V		0.4	V
$I_{I(Hold)}$	Input leakage current (hold)	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V	3 V	–75		μA
		V_I = 0 to 3.6 V	3.6 V		500	μA

Refer to Table 3 for input and output details about the SN74AHC245 device.

Table 3. Specifications of the Tri-State Outputs: SN74AHC245

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	Output high voltage	I_{OH} = 4 mA	3 V	2.48		V
V_{OL}	Output low voltage	I_{OL} = 4 mA	3 V		0.44	V
I_{OZ}	High-impedance state output current	$V_O = V_{CC}$ or GND	5.5 V		2.5	μA

Refer to Table 4 for input and output details about the TMS320C6201 digital signal processor.

Table 4. Specifications of the Tri-State Outputs: TMS320C6201

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	Output high voltage	I_{OH} = 12 mA	3.14 V	2.48		V
V_{OL}	Output low voltage	I_{OL} = 12 mA	3.14 V		0.4	V
I_{OZ}	High-impedance state output current	$V_O = 0$ or D_{VDD}	3.46 V		10	μA

Due to the appropriate logic levels (V_{IL} < 0.8 V, V_{IH} > 2.0 V), the bus-hold circuit in the SN74LVCH245 device supplies a current of $I_{I(hold)}$ > |75 µA|. Assuming a maximum leakage current of I_{OZmax} = 10 µA for tri-state outputs, a single bus-hold device is capable, on its own, to compensate for the leakage currents of the other nine devices connected to the bus and ensures defined levels on the bus lines.

As noted above, in practice, none of the integrated circuits show the maximum output leakage currents I_{OZ} given in the data sheets. Due to the large variation of the transistor parameters caused by production variations and changes in supply voltage and temperature, the maximum current $I_{I(hold)}$ might rise to 500 µA (see Figure 10).

In the example shown here, a single active output also must be able to charge and discharge the device's capacitance and to switch eight inputs with the bus hold. The outputs of the LVCH and AHC devices, and the processor, can supply a current of 8 × $I_{I(hold)max}$ = 4 mA (see Table 2 , Table 3, and Table 4).

6.2 Influence on the Circuit's Power Loss

When using bus-hold circuits, a current, $I_{I(hold)}$, flows during a signal state transition from low to high and from high to low for the duration of the signal slope. This current has an influence on the system's power consumption. The resultant power dissipation can be calculated as shown below.

According to Table 2, the maximum current in bus-interface device SN74LVCH245 is $I_{I(hold)max}$ = 500 µA at V_{CCmax} = 3.6 V. Because the current during a signal transition follows a triangular shape, we can derive the power consumption, P_{hold}, caused during signal transitions by the bus-hold circuits:

$$P_{hold} = \frac{1}{2} \times V_{CC} \times I_{I(hold)max} \times t_r \times 2 \times f \times n$$

where

- t_r = signal rise or fall time
- f = frequency of signal exchange
- n = number of inputs with a bus-hold circuit
- $I_{I(hold)max}$ = maximum bus-hold circuit input current (6)

For the SN74LVCH245 device, n = 8. If we assume that the mean frequency (f) of signal transitions at the inputs = 10 MHz, the rise time, t_r = 2 ns, yielding:

$$P_{hold} = \frac{1}{2} \times 3.6\ V \times 500\ \mu A \times 2\ ns \times 2 \times 10\ MHz \times 8 = 0.288\ mW$$

(7)

Equation 7 predicts that the parameter P_{hold} increases with longer rise times. In contrast, taking the power dissipation capacitance C_{PD} = 31 pF given in the device's data sheet, the dynamic power dissipation (P_{dyn}) of the circuit can be calculated as:

$$P_{dyn} = C_{pd} \times V_{CC}^2 \times f \times n = 31\,pF \times 3.6^2 \times 10\ MHz \times 8 = 320\ mW$$

(8)

As P_{dyn} is several orders of magnitude greater than the P_{hold}, the power consumption caused by the bus-hold circuit P_{hold} can be disregarded.

6.3 Presetting Logic Levels

Some applications require specific logic levels on certain bus lines during the initialization phase, after the supply voltage is switched on. The microprocessor queries this level and makes certain system settings (start vector, et cetera) on the basis of the information it reads. In conventional bus-interface devices, the desired level is generated on the bus lines via pull-up or pull-down resistors. Since the input resistance of CMOS circuits are very high, high-impedance resistors (10 kΩ to 100 kΩ) are sufficient enough to achieve the voltage level.

However, when using interface devices with the bus-hold function, this circuit detail needs to be paid attention to. Hold circuits have an inherent tendency to generate at a low level when the supply voltage is switched on. As previously noted, this circuit behaves like a latch. A comparatively large capacitance – the interconnect lines and other circuit components – is connected to its set input (the input of the integrated circuit). This capacitance is discharged when the supply voltage is switched on. This is the reason that a low level is generated there when the voltage is switched on. The bus-hold circuit still has a very high impedance during the first moment of the power-on phase (V_{CC} 3 V_T). Using a high-impedance pull-up resistor (10 kΩ to 100 kΩ), at this point in time, is able to force the latch into the opposite logic state and generate a high level at the input of the bus-hold circuit.

Additionally, this observation does not take into account that other devices connected to this bus might couple a charge into the previously mentioned capacitance during voltage startup, which then forces a different level than the expected level. In this scenario, the outputs of the interface devices that are connected to the bus are more effective compared to the bus-hold circuit and an associated preset circuit. If the outputs during the power-on phase briefly enter an undesired active state, they force the bus-hold circuit to the output's state. Then, a high-impedance pull-up or pull-down resistor is no longer able to change this state.

Consequently, the only way to force the device to a certain state is to place suitable low-impedance pull-up or pull-down resistors. The maximum input current to a bus-hold circuit, $I_{I(hold)max}$ = 500 μA. This current flows when a hold-circuit threshold voltage of V_T = 1.5 V is reached (see Figure 10).

Using this figure, the value for pull-up resistance, R_P, can be calculated as:

$$R_p = \frac{V_{CCmin} - V_t}{I_{I(hold)max}} \tag{9}$$

If an LVCH circuit is connected to the bus, the resistance is calculated as:

$$R_p = \frac{3.0\ V - 1.5\ V}{500\ \mu A} = 3\ k\Omega \tag{10}$$

If several devices with the bus-hold function are connected to the bus, the resistance value must be reduced accordingly.

6.4 Applications

The RMII interface standard is designed to reduce the amount of signals required to connect the PHY and the MAC. With this process, a single clock is used instead of two separate clocks. The clock frequency is set at 50 MHz or 100 Mbps, while the data interface is shortened to be two bits instead of four bits. Table 5 below lists the RMII interface signals.

NOTE: The Management Data Input and Output (MDIO) is a bidirectional open-drain interface which is not shown, but the MDIO is a subset of the RMII interface.

Table 5. RMII Interface

SIGNAL	DESCRIPTION	DIRECTION
REF_CLK	Reference clock (50 MHz or 100 Mbps)	From the MAC to the PHY or to the external input
TXD0	Transmit data bit 0	From the MAC to the PHY
TXD1	Transmit data bit 1	From the MAC to the PHY
TX_EN	When set at high, the clock data on the TXD0 and the TXD1 is sent to the transmitter	From the MAC to the PHY
RXD0	Receive data bit 0	From the MAC to the PHY
RXD1	Receive data bit 1	From the MAC to the PHY
CRS_DV	Carrier Sense (CRS) and RX_Data Valid (RX_DV) multiplexed. In a mode of 10 Mbps, (use another word instead of it) alternates every 10 clock cycles	From the MAC to the PHY
RX_ER	Receive error	From the MAC to the PHY

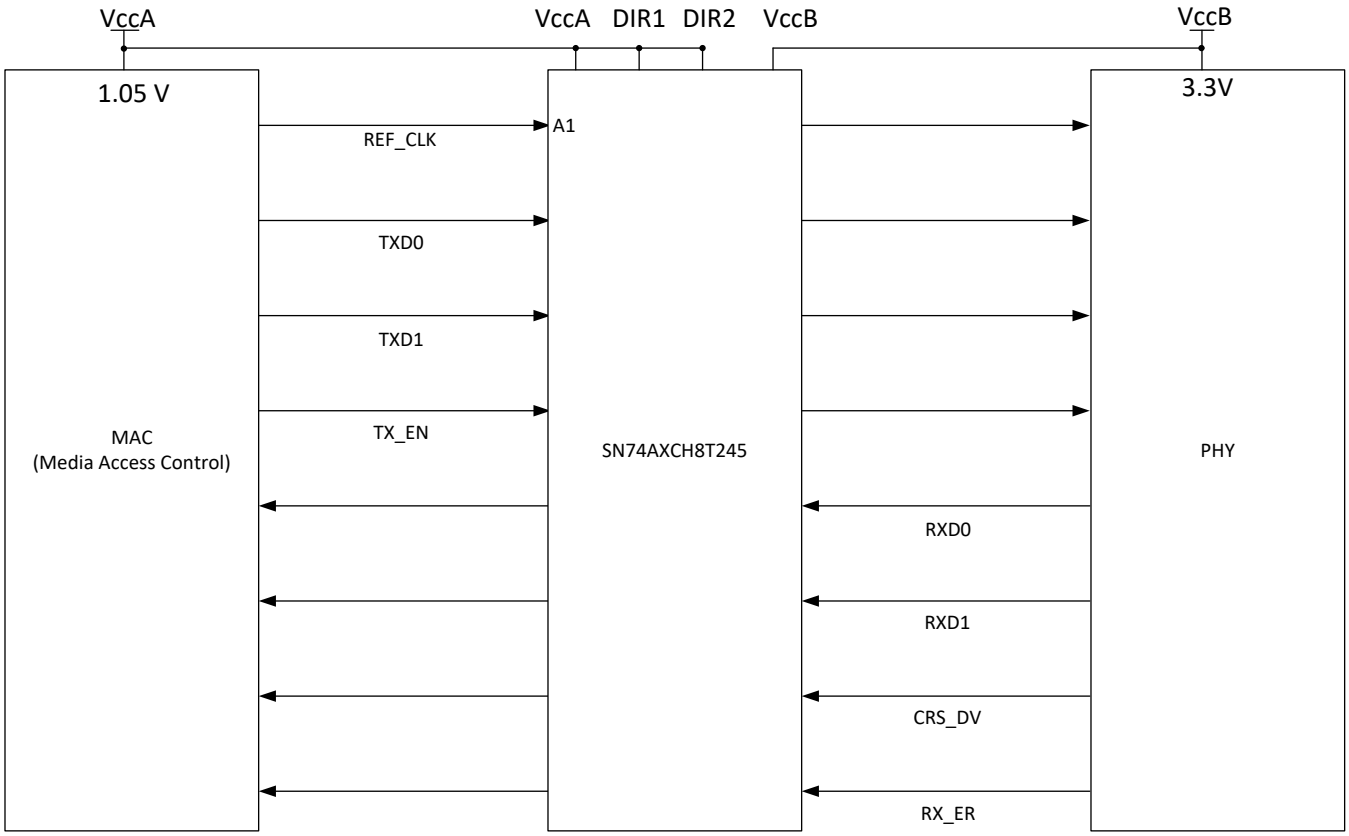

Figure 12. RMII Interface using SN74AXCH8T245

In Figure 13, the data center switches block diagram is shown. The Field programmable gate array (FPGA) and Central Processing Unit (CPU) have lower operating voltages to reduce power consumption. Hence, voltage level translation devices, such as the SN74AXCH8T245, with integrated bus-hold circuits are required for communication between the FPGA and the PHY. This requirement also applies between the FPGA and the CPU.

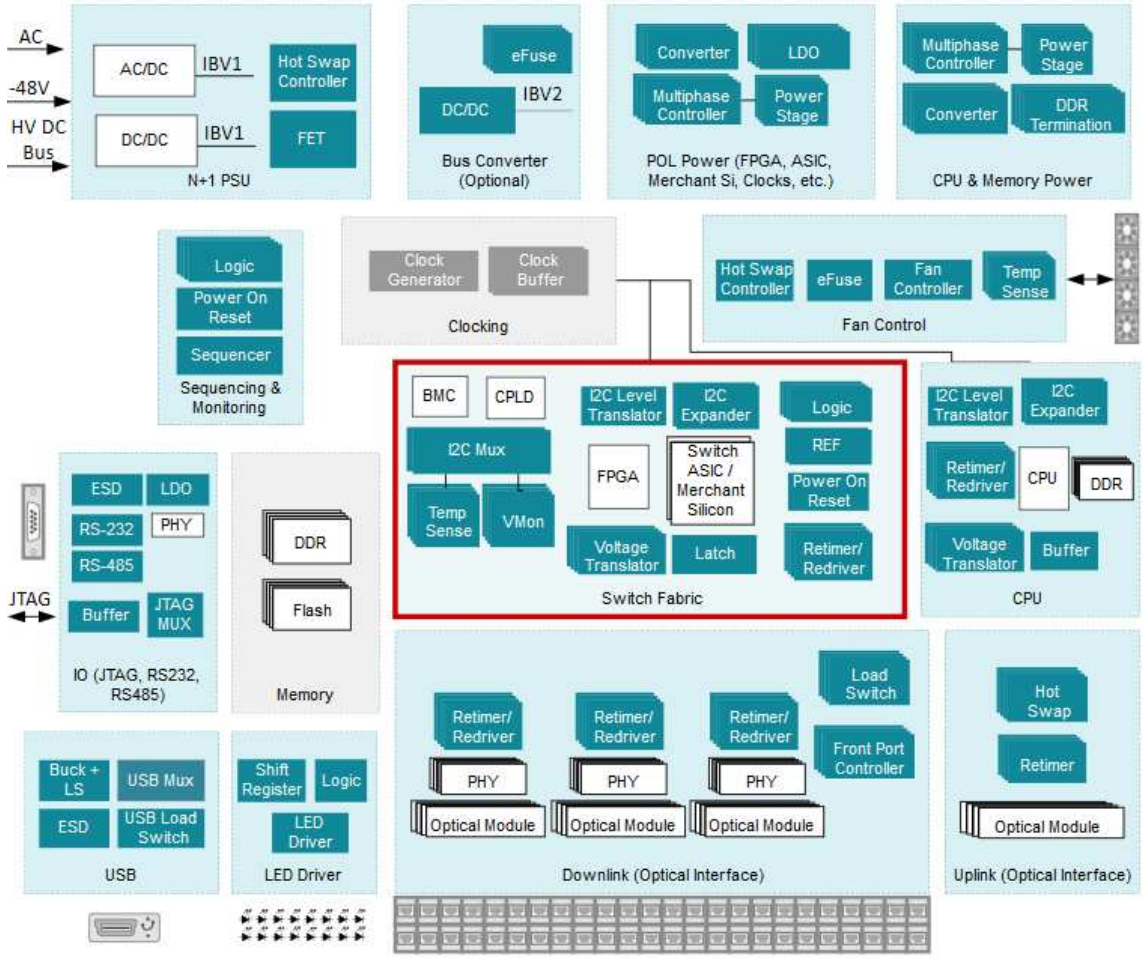

Figure 13. Data Center Switches

7 Summary

This application report addresses the question of how to ensure defined levels on bus lines when all bus drivers are in the inactive high-impedance state (tri-state). This is important, when smaller CMOS-based systems, where the lines cannot be terminated by a resistor network, match to the line impedance. This application report explains different circuit options, with a particular reference to a novel bus-hold circuit that TI integrates into modern bus-interface devices. The additional bus-hold circuit provides an ideal combination of all the functions needed for a bus system to run properly. These functions are as follows:

- To ensure a defined logic level when the bus is in the inactive state (tri-state).
- To avoid an excessive supply current that is caused by logic levels lying outside of the limits range stipulated in the data sheets. A bus-hold circuit is often required for battery-operated systems.
- To prevent oscillations of the bus-interface devices due to undefined logic levels. With the addition of power consumption, this measure promotes the reliability and the electromagnetic compatibility of the system.

8 References

- Texas Instruments, *CMOS Power Consumption and CPD Calculation* application report
- Texas Instruments, *Solving CMOS Transition Rate Issues with Schmitt Triggers* application report
- *RMII Interface* Wikipedia

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