Functional Safety Information

TPS272C45

Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS272C45 (QFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

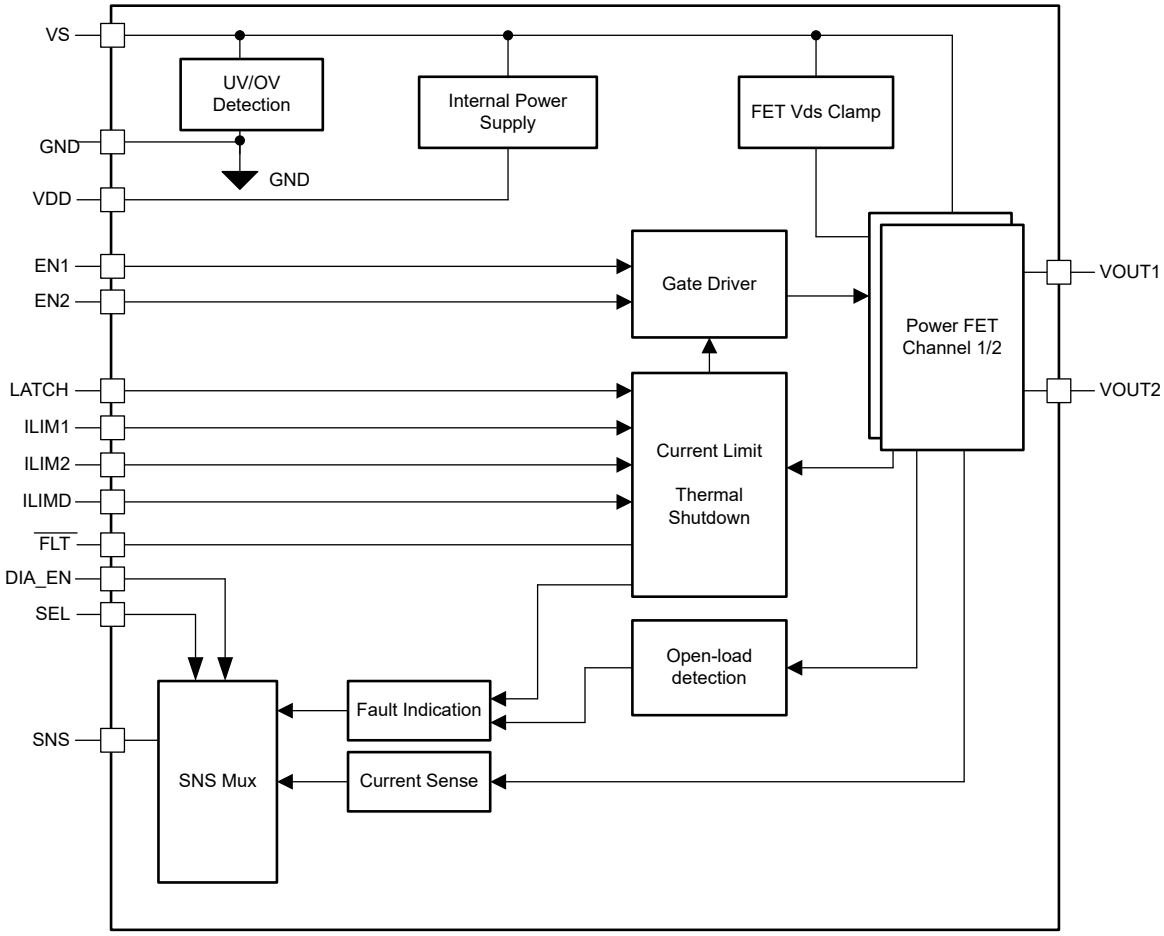

Figure 1-1. Functional Block Diagram

TPS272C45 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS272C45 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	5
Package FIT Rate	12

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 660 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS272C45 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT1, 2 open (HiZ)	20%
OUT1, 2 stuck ON to VS	10%
OUT1, 2 not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protection function fails to trip	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS272C45. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS272C45 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS272C45 data sheet.

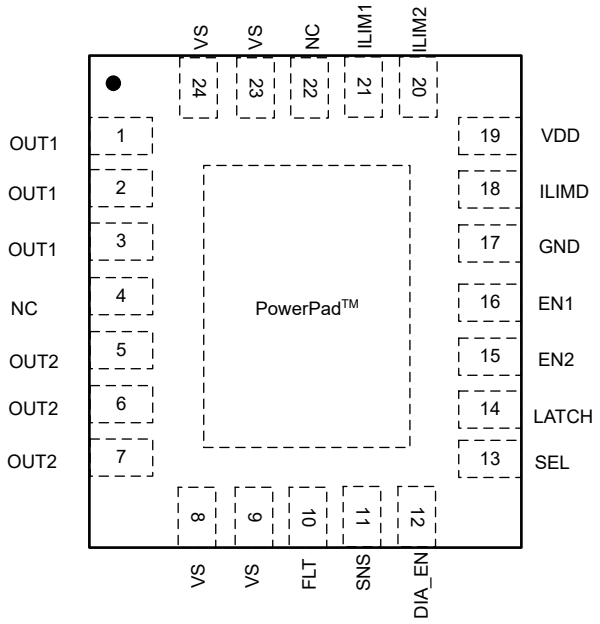

Figure 4-1. Pin Diagram Versions A or C

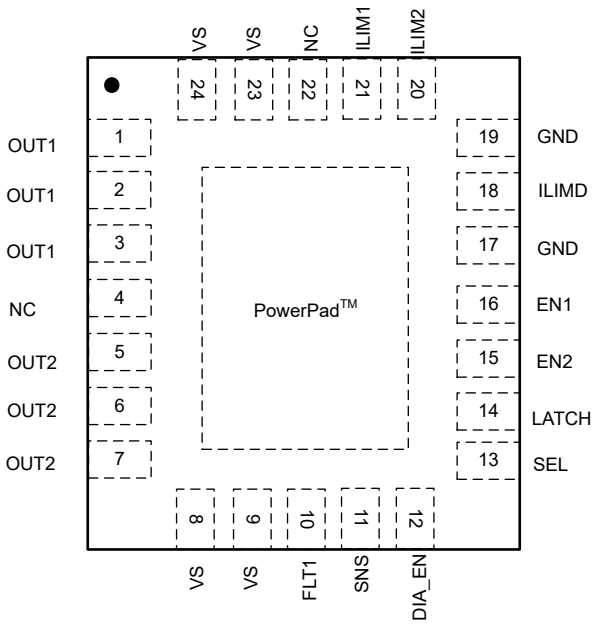

Figure 4-2. Pin Diagram Version B

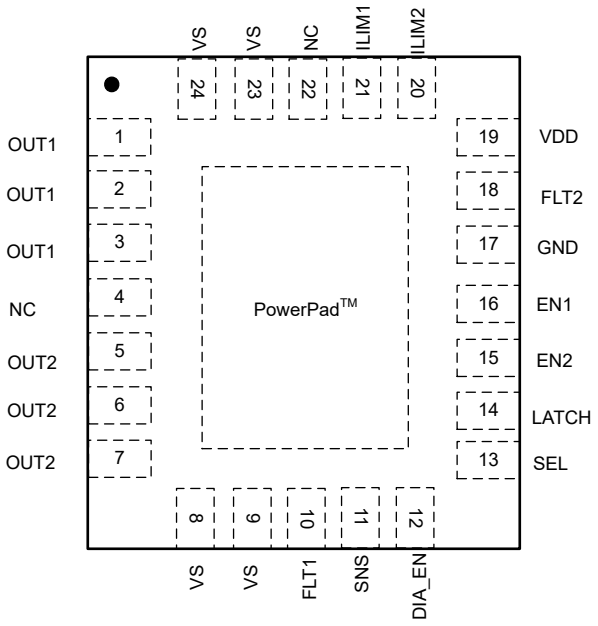

Figure 4-3. Pin Diagram Version D

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the data sheet, including pull-up and pull-down resistors as needed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1, 2, 3	Current limit of the device engages and thermal protection turns off the Channel 1 (OUT1) FET	B
NC	4, 22	No effect	D
OUT2	5, 6, 7	Current limit of the device engages and thermal protection turns off the Channel 1 (OUT1) FET	B
VS	8, 9, 23, 24	The output stages are not powered and the FET does not turn ON	B
FLT (version A, B, C)	10	Fault status reported can be erroneous	B
FLT1 (version D)	10	Fault status reported can be erroneous	B
SNS	11	SNS current or fault status reported on the SNS pin is erroneous	B
DIA_EN	12	Diagnostics including current sense and fault reporting does not function	B
SEL	13	If DIA_EN high then channel 1's sense current output always on SNS	B
LATCH	14	Device will default to auto-retry mode when encountering thermal fault	B
EN1	15	Channel 1 FET is turned off	B
EN2	16	Channel 2 FET is turned off	B
GND	17	Any GND network connected for protection is bypassed	B
ILIMD (version A, B, C)	18	The threshold for current limit is set by ILIMx pin for the entire duration after the channel is enabled. The higher or lower current limit setting for a period after enable and the delay duration does not function	B
FLT2 (version D)	18	Fault status reported can be erroneous	B
VDD (Version A, C, D)	19	Version A, C, D: If an external supply is connected (that is, not grounded) , the device switches to powering all blocks from VS supply – loss of output state for a period and an increase in current draw from VS supply	B
GND (Version B)	19	Version B: no effect	D
ILIMx	20, 21	The current limit protection switches to a level set internally at a higher level	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1, 2, 3	If any one pin is open, an increase in switch resistance. If all pins are open, OUT1 is high impedance	B
NC	4, 22	No effect	D
OUT2	5, 6, 7	If any one pin is open, an increase in switch resistance. If all pins are open, OUT1 will be high impedance	B
VS	8, 9, 23, 24	If any one pin is open, an increase in switch resistance. If all pins are open, output stage power supply input is lost and output switches do not function.	B
FLT (version A, B, C)	10	Fault condition cannot be reported	B
FLT1 (version D)	10	Fault condition on channel 1 cannot be reported	B
SNS	11	No current out of the SNS pin, no current sense functionality	B
DIA_EN	12	Pin pulled low internally, diagnostics including current sense and fault reporting does not function	B
SEL	13	Pin pulled low internally, diagnostics including current sense and fault reporting is for Channel 1 only	B
LATCH	14	Pin pulled low internally, device will default to auto-retry mode when encountering thermal fault	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN1	15	Pin pulled low internally, Channel 1 FET is turned off	B
EN2	16	Pin pulled low internally, Channel 2 FET is turned off	B
GND	17	The output FETs are off and the device supply and functionality is lost	B
ILIMD (version A, B, C)	18	The current limit configuration and delay during the initial phase after enable defaults to > 40 kohm	B
FLT2 (version D)	18	Fault condition on Channel 2 cannot be reported	B
VDD (Version A, C, D)	19	Version A, C, D: If an external supply is connected (i.e. Not grounded) , the device will switch to powering all blocks from VS supply - loss of output state for a period and an increase in current draw from VS supply	B
GND (Version D)	19	Version B: no effect	D
ILIMx	20, 21	The current limit protection switches to a level set internally at a higher level	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1, 2, 3	NC	No effect	D
NC	4	OUT2	No effect	D
OUT2	5, 6, 7	N/A	Not plausible (corner pin)	D
VS	8, 9	FLT (versions A, B, C)	Fault condition cannot be reported	B
VS	8, 9	FLT1 (version D)	Fault condition on Channel 1 cannot be reported	B
FLT1 or FLT	10	SNS	SNS current output is affected, fault condition not reported correctly	B
SNS	11	DIA_EN	SNS current output affected, diagnostic functionality affected.	B
DIA_EN	12	N/A	Not plausible (corner pin)	B
SEL	13	LATCH	Diagnostic functionality affected, as well as auto-retry and latch on thermal fault behavior	B
LATCH	14	EN1	The output state on Channel 1 can be affected	B
EN1	15	EN2	The output state on Channel 1 or Channel 2 can be affected	B
EN2	16	GND	The output on Channel 2 cannot be turned ON	B
GND	17	ILIMD (Versions A, B, C)	The threshold for current limit is set by ILIMx pin for the entire duration after the channel is enabled. The higher or lower current limit setting for a period after enable and the delay duration does not function	B
GND	17	FLT2 (Version D)	Fault status reported on Channel 2 can be erroneous	B
ILIMD (Versions A, C)	18	VDD (Version A, C)	The current limit behavior on enable is affected, additional current draw from VDD supply, if connected.	B
ILIMD (Version B)	18	GND (Version B)	The threshold for current limit is set by ILIMx pin for the entire duration after the channel is enabled. The higher or lower current limit setting for a period after enable and the delay duration does not function	B
FLT2 (Version D)	18	VDD (Version D)	Fault status reported on Channel 2 can be erroneous	B
VDD (Version A, C, D)	19	N/A	Not plausible (corner pin)	B
VDD (Version B)	19	N/A	Not plausible (corner pin)	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1, 2, 3	The channel 1 output cannot be turned off, OUT1 connected to VS	B
NC	4, 22	No effect	D
OUT2	5, 6, 7	The channel 2 output cannot be turned off, OUT2 connected to VS	B
VS	8, 9, 23, 24	No effect	D
FLT (versions A, B, C)	10	Fault status reported can be erroneous	B
FLT1 (version D)	10	Fault status reported can be erroneous	B
SNS	11	SNS pin current or fault status reported can be erroneous	B
DIA_EN	12	Diagnostics will be constantly enabled	B
SEL	13	If DIA_EN high then channel 2's sense current output always on SNS	B
LATCH	14	Device will default to latch mode when encountering thermal fault	B
EN1	15	Channel 1 FET is turned ON, output cannot be turned OFF	B
EN2	16	Channel 2 FET is turned ON, output cannot be turned OFF	B
GND	17	The output stages are not powered and the FET does not turn ON	B
ILIMD (Version A, B, C)	18	The current limit behavior on enable is erroneous, potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
FLT2 (Version D)	18	Fault status reported may be erroneous, potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
VDD (Version A, C, D)	19	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell and loss of full device functionality	A
GND (Version B)	19	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell and loss of full device functionality	A
ILIMx	20, 21	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell and loss of all functionality	A

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265