Functional Safety Information

TPD3S713-Q1
Functional Safety FIT Rate and FMD

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Trademarks

1 Overview

This document contains information for TPD3S713-Q1 (RVC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

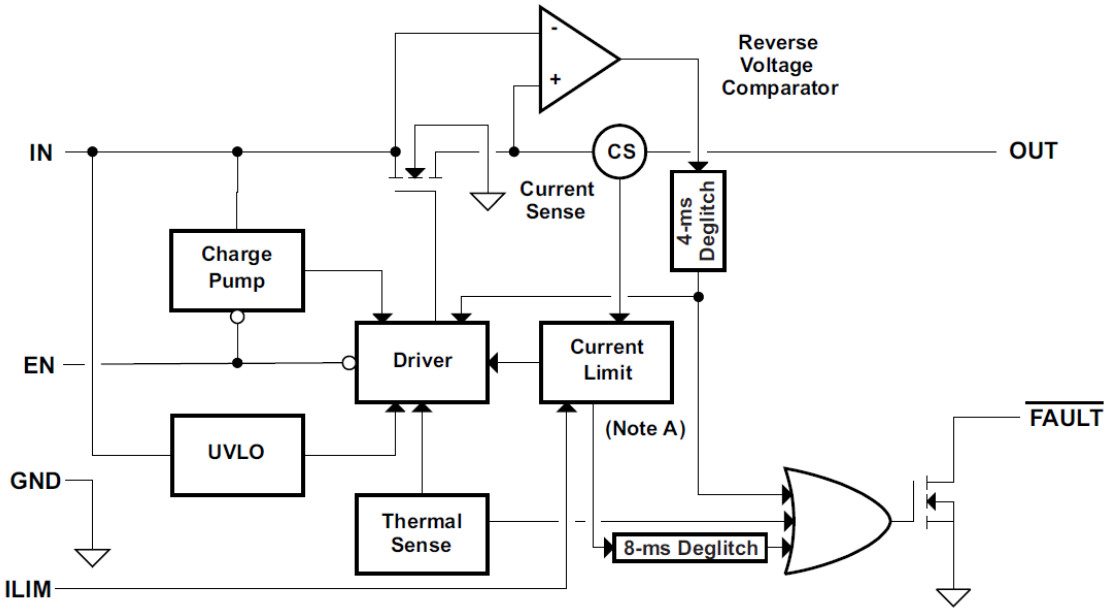

Figure 1-1. Functional Block Diagram

TPD3S713-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPD3S713-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	2
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPD3S713-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
BUS no output	35%
BUS output not in specification-voltage or timing	30%
OUT power FET stuck on	15%
DP_IN, DM_IN, DP_OUT, DM_OUT – not in specification – voltage or timing	15%
FAULT false trip or fails to trip	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPD3S713-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPD3S713-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPD3S713-Q1 data sheet.

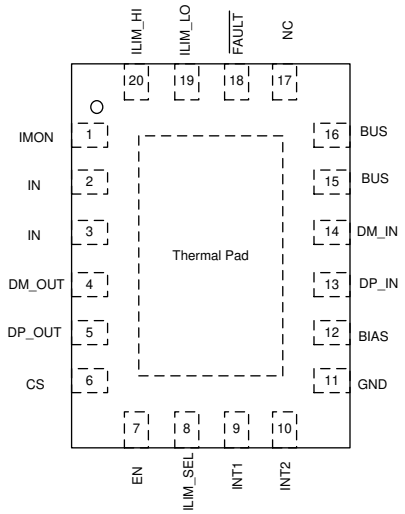

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the 'Recommended Operating Conditions' and the 'Absolute Maximum Ratings' found in the appropriate device data sheet.
- Configuration as shown in the 'Example Application Circuit' found in the appropriate device data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IMON	1	Loss of current monitor functionality, device can't sense the current.	C
IN	2	Device will not operate. No BUS output voltage.	B
IN	3	Device will not operate. No BUS output voltage.	B
DM_OUT	4	Device can't communicate with host and attached device.	B
DP_OUT	5	Device can't communicate with host and attached device.	B
CS	6	Loss of 'Linear cable compensation current' functionality.	C
EN	7	Loss of ENABLE functionality. Device will remain in shut-down mode.	B
ILIM_SEL	8	ILIM_LO resistor is valid, not any function will be impacted.	C
INT1	9	Device can‘t enter into the normal mode.	B
INT2	10	No effect.	D
GND	11	No effect.	D
BIAS	12	Device can't communicate with host and attached device.	B
DP_IN	13	Device can't communicate with host and attached device.	B
DM_IN	14	Device can't communicate with host and attached device.	B
BUS	15	Device hiccups and under current limitted status.	B
BUS	16	Device hiccups and under current limitted status.	B
NC	17	No effect.	D
/FAULT	18	Loss of /FAULT functionality, device always appears to be in the fault condition.	C
ILIM_LO	19	Device will have the max current limit value at 1.15A TYP.	C
ILIM_HI	20	Device will have the max current limit value at 1.15A TYP.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IMON	1	Loss of current monitor functionality, device can't sense the current.	C
IN	2	Long-term reliability may impact due to lower bonding-wire count.	C
IN	3	Long-term reliability may impact due to lower bonding-wire count.	C
DM_OUT	4	Device can't communicate with host and attached device.	B
DP_OUT	5	Device can't communicate with host and attached device.	B
CS	6	Loss of 'Linear cable compensation current' functionality.	C
EN	7	Device enable status is uncertain and can't be controlled.	B
ILIM_SEL	8	ILIM_HI/LO selection is uncertain and can't be controlled.	C
INT1	9	Device operating mode is uncertain and can't be controlled.	C
INT2	10	BUS OVP threshold is uncertain between 6V and 6.95V.	C
GND	11	Device remains unpowered.	B
BIAS	12	Affect the IEC ESD performance.	C
DP_IN	13	Device can't communicate with host and attached device.	B
DM_IN	14	Device can't communicate with host and attached device.	B
BUS	15	Long-term reliability may impact due to lower bonding-wire count.	C
BUS	16	Long-term reliability may impact due to lower bonding-wire count.	C
NC	17	No effect.	D
/FAULT	18	Loss of /FAULT functionality.	C
ILIM_LO	19	No effect if ILIM_SEL is high, otherwise current limit value is close to 0, and device is in current limit status.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ILIM_HI	20	No effect if ILIM_SEL is low, otherwise current limit value is close to 0, and device is in current limit status.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IMON	1	IN	Loss of current monitor functionality, device can't sense the current.	C
IN	2	IN	No effect.	D
IN	3	DM_OUT	Device can't communicate with host and attached device.	B
DM_OUT	4	DP_OUT	Device can't communicate with host and attached device.	B
DP_OUT	5	CS	Device can't communicate with host and attached device, and loss of 'Linear cable compensation current' functionality.	B
CS	6	EN	Loss of 'Linear cable compensation current' functionality, and device enable status is uncertain and can't be controlled.	B
EN	7	ILIM_SEL	ILIM_SEL high/low and device off/on depend on how EN and ILIM_SEL circuits interact.	B
ILIM_SEL	8	INT1	ILIM_SEL high/low and device operating mode depend on how ILIM_SEL and INT1 circuits interact.	B
INT1	9	INT2	Device operating mode and BUS OVP threshold depend on how INT1 and INT2 circuits interact.	B
INT2	10	GND	No effect.	D
GND	11	BIAS	Device can't communicate with host and attached device.	B
BIAS	12	DP_IN	Device can't communicate with host and attached device.	B
DP_IN	13	DM_IN	Device can't communicate with host and attached device.	B
DM_IN	14	BUS	Device enter into DM_IN OVP, and can't communicate with host and attached device.	B
BUS	15	BUS	No effect.	D
BUS	16	NC	NC pin is open-drain structure, if NC pin is trigged, BUS will be shortted to ground.	B
NC	17	/FAULT	NC pin is open-drain structure, if NC pin is trigged, /FAULT will be shortted to ground.	C
/FAULT	18	ILIM_LO	Loss of /FAULT functionality, current limit value is impacted.	B
ILIM_LO	19	ILIM_HI	Current limit value is impacted.	C
ILIM_HI	20	IMON	Loss of current monitor functionality, current limit value is impacted.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IMON	1	Loss of current monitor functionality, device can't sense the current.	C
IN	2	No effect.	D
IN	3	No effect.	D
DM_OUT	4	Device can't communicate with host and attached device.	B
DP_OUT	5	Device can't communicate with host and attached device.	B
CS	6	Loss of 'Linear cable compensation current' functionality.	C
EN	7	Device is always enabled.	C
ILIM_SEL	8	ILIM_HI is always selected.	C
INT1	9	Device is always in normal mode.	C
INT2	10	BUS OVP threshold is 6.95V.	C
GND	11	Former power supply may be pulled down, device is unpowered.	B
BIAS	12	Affect the IEC ESD performance.	C
DP_IN	13	Device enter into DP_IN OVP, it can't communicate with host and attached device.	B
DM_IN	14	Device enter into DM_IN OVP, it can't communicate with host and attached device.	B
BUS	15	Power switch will be bypassed.	B
BUS	16	Power switch will be bypassed.	B
NC	17	No effect.	D
/FAULT	18	Loss of /FAULT functionality, can't check whether the device is in the fault condition.	C
ILIM_LO	19	No effect if ILIM_SEL is high, otherwise current limit value is close to 0, and device is in current limit status.	B
ILIM_HI	20	No effect if ILIM_SEL is low, otherwise current limit value is close to 0, and device is in current limit status.	B

5 Revision History

Changes from Revision * (June 2021) to Revision A (October 2023)	Page
• Added Pin FMA information	5

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