Functional Safety Information

LM73606-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the LM73606-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

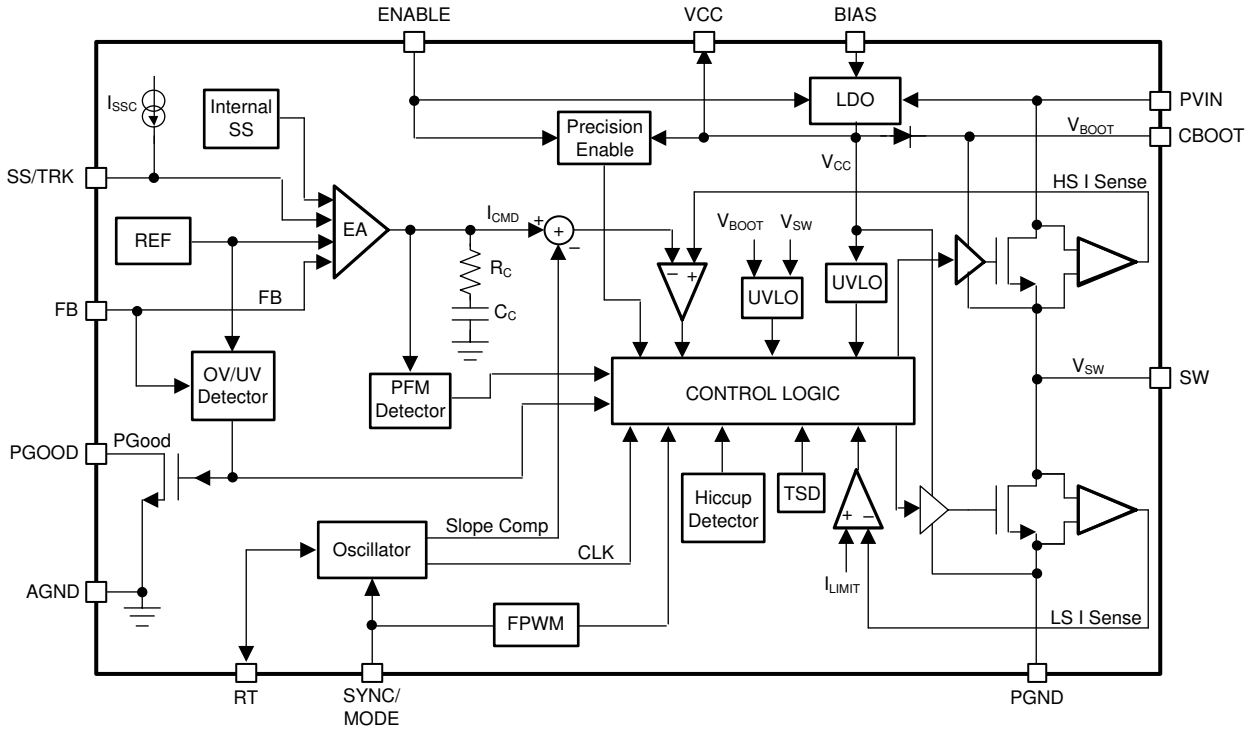

Figure 1-1. Functional Block Diagram

The LM73606-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM73606-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	6
Package FIT rate	14

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 800 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =< 50 V supply	25 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM73606-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW not switching, output stuck on	10
SW not switching, no output	20
SW switching, out of specification voltage or timing	60
Power Good – False Trip or Failure to Trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM73606-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)

Table 4-2 through Table 4-4 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM73606-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM73606-Q1 data sheet.

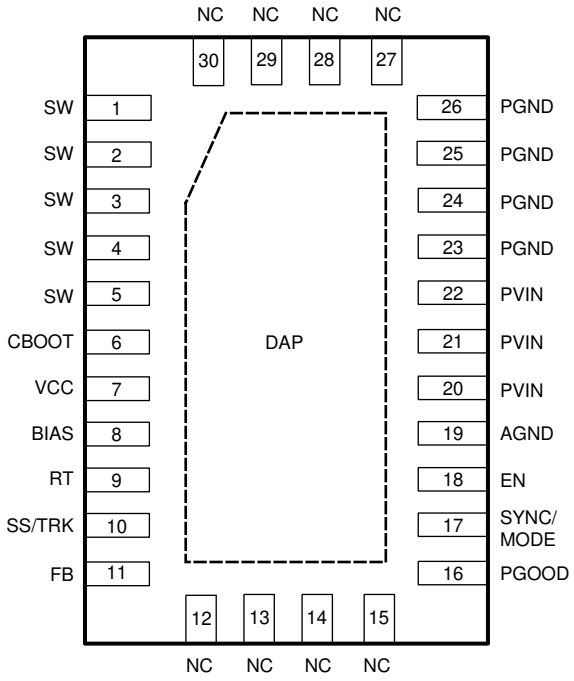

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application Circuit as per the LM73606-Q1 data sheet is used
  - PG is pulled up to VOUT

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	Shorting the SW pin to ground results in large currents through the device and subsequent damage. No output voltage is produced.	A
CBOOT	6	Driver supply to the high-side MOSFET is lost. Output voltage is not regulated. Possible damage to internal regulator and CBOOT charging circuit	B
VCC	7	Internal circuits are disabled. No output voltage is generated. Possible increase in input current and possible damage to internal LDO	C
BIAS	8	A valid connection for the BIAS input. The internal LDO is powered from the input voltage.	D
RT	9	The device is incapable of switching, and no output voltage is produced.	C
SS/TRK	10	The device does not start up. No signal on switch and no output voltage is produced.	C
FB	11	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage level. Possible damage to customer load, output stage components, or both, can occur.	B
NC	12, 13, 14, 15	No risk	D
PGOOD	16	A valid connection for the PG output. PG functionality is lost. Damage to customer components connected to PG input can occur.	C
SYNC/MODE	17	A valid connection for the SYNC/MODE input. Enable auto mode operation.	D
EN	18	A valid connection for the EN input. Enable functionality is lost; the device remains off with no output voltage generated. Damage to customer components connected to EN input can occur.	D
AGND	19	No risk. Ground pin	D
VIN	20, 21, 22	No output voltage is generated. Possible damage to customer input supply, PCB, or both, can occur unless customer provides protection. Reverse current from SW pin to VIN pin due to discharge of output capacitors can damage the regulator.	B
PGND	23, 24, 25, 26	No risk. Ground pin	D
NC	27, 28, 29, 30	No risk	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	Loss of output voltage	B
CBOOT	6	Driver supply to high-side MOSFET is lost. Output voltage is not regulated. Low or no output voltage; erratic switching behavior	B
VCC	7	Internal LDO can oscillate. VCC voltage is not stable. Internal circuits do not function correctly. Output voltage may not be regulated. Damage to internal LDO is possible.	A
BIAS	8	The internal LDO is be powered from the input voltage.	D
RT	9	A valid condition for the RT pin. The device uses the default switching frequency of 500 kHz.	C
SS/TRK	10	A valid condition for the SS/TRK pin. The device uses the internal soft-start ramp.	D
FB	11	The device does not regulate. Output voltage can rise or fall. Damage to customer load, output stage components, or both, is possible.	B
NC	12, 13, 14, 15	No risk	D
PGOOD	16	A valid connection for the PG output. PG functionality is lost.	C
SYNC/MODE	17	Floating this pin can cause unexpected operation mode.	B
EN	18	Loss of enable functionality. Erratic operation; probable loss of regulation	B
AGND	19	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B
VIN	20, 21, 22	Loss of output voltage	B
PGND	23, 24, 25, 26	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	27, 28, 29, 30	No risk	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	CBOOT	Boot capacitor does not charge. Erratic operation with loss of regulation	B
CBOOT	6	VCC	Damage to VCC regulator, other internal circuits, or both. Output voltage can be affected.	A
VCC	7	BIAS	FETs are undersupplied. No regulation on output. Unloaded device is able to regulate.	A
BIAS	8	RT	Internal circuits are disabled. No output voltage is generated. Possible increase in input current and possible damage to internal LDO	A
RT	9	SS/TRK	Internal circuits are disabled. No output voltage is generated.	B
SS/TRK	10	FB	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage level. Possible damage to customer load, output stage components, or both, can occur.	B
FB	11	NC	When NC is not connected, there is no issue.	D
			When connecting NC to ground, the regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage level. Possible damage to customer load, output stage components, or both, can occur.	B
NC	12, 13, 14, 15	PG	When NC is not connected, there is no issue.	D
			When connecting NC to ground, the PGOOD pin is shorted to ground. Consequently, the PGOOD output is not functional.	C
PG	16	SYNC/MODE	When SYNC/MODE is tied low: the PGOOD pin is shorted to ground. Consequently, the PGOOD output is not functional. If PGOOD is tied to VOUT, then the output voltage is shorted and the device enters hiccup operation.	C
			When SYNC/MODE is tied high: if PGOOD is shorted to VOUT < 5.5 V, possible damage to customer load, output stage components, or both, can occur.	B
			When SYNC/MODE is tied high: if PGOOD is > 5.5 V, this exceeds to the absolute maximum of SYNC/MODE. The device is at risk to be damaged.	A
SYNC/MODE	17	EN	When SYNC/MODE is tied low: a valid connection for the EN input. Enable functionality is lost; the device remains off with no output voltage generated.	B
			When SYNC/MODE is tied high to external supply: a valid connection for the EN input. Enable functionality is lost; the device remains on.	C
			When SYNC/MODE is tied high to VCC: if short occurs before start-up, the device does not start up. If short occurs during regulation, enable functionality is lost and the device remains on.	B
EN	18	AGND	A valid connection for the EN input. Enable functionality is lost; the device remains off with no output voltage generated.	B
AGND	19	PVIN	No output voltage is generated. Possible damage to customer input supply, PCB, or both, can occur unless customer provides protection. Reverse current from SW pin to the VIN pin due to discharge of output capacitors can damage regulator.	B
PVIN	20, 21, 22	PGND	No output voltage is generated. Possible damage to customer input supply, PCB, or both, can occur unless customer provides protection. Reverse current from SW pin to the VIN pin due to discharge of output capacitors can damage regulator.	B
PGND	23, 24, 25, 26	NC	No issue. PGND is a valid connection for NC.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	27, 28, 29, 30	SW	When NC is floating, there is no issue.	D
			When NC is connected to GND: this is high risk. Shorting the SW pin to ground results in large currents through the device and subsequent damage. No output voltage is produced.	A

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