Functional Safety Information

TMP127-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

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1 Overview

This document contains information for the TMP127-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

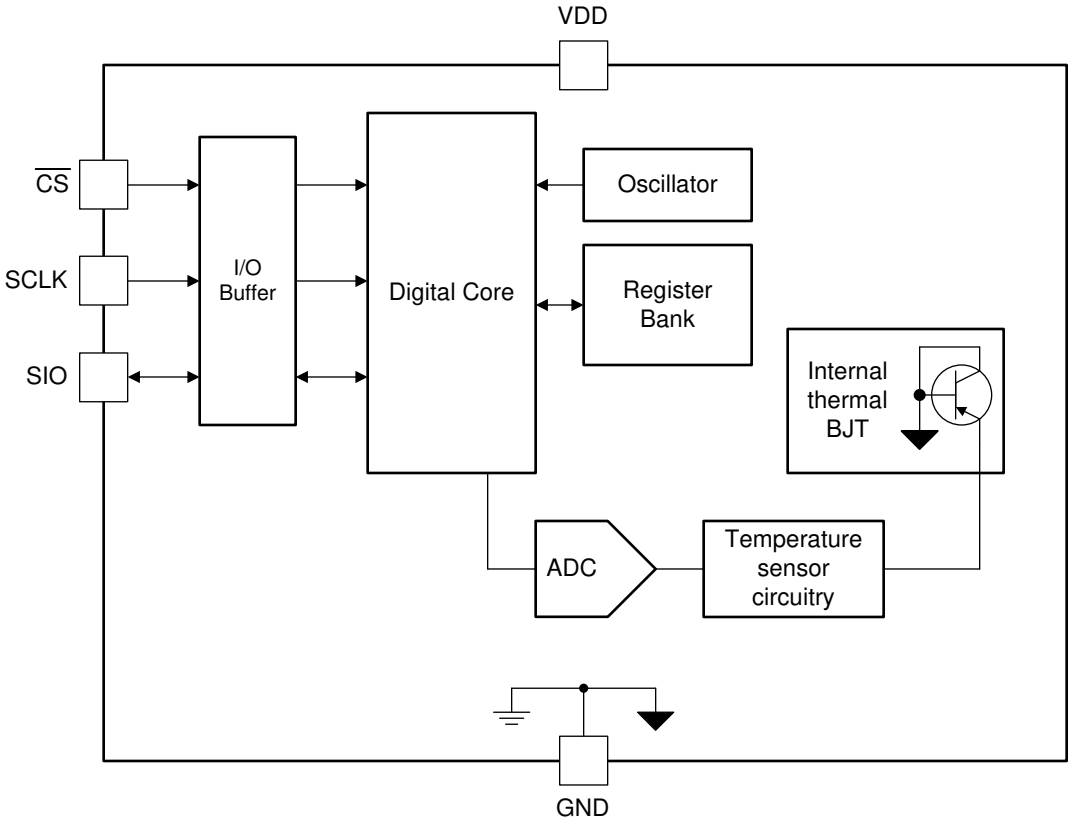

Figure 1-1. Functional Block Diagram

The TMP127-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 package of the TMP127-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1.0 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMP127-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Serial Communication Error	15%
ADC offset out of specification	20%
ADC gain out of specification	25%
ADC conversion output code bit error	15%
ADC incorrect input channel selected	5%
Register bank data bit error	15%
Alert false trip, fails to trip	5%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP127-Q1 (SOT-23 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2.)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- The device is the only slave on the SPI bus.

4.1 SOT-23 Package

Figure 4-1 shows the TMP127-Q1 pin diagram for the SOT-23 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP127-Q1 data sheet.

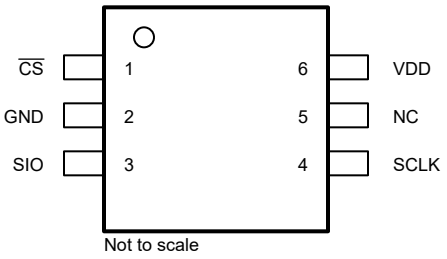

Figure 4-1. Pin Diagram (SOT-23) Package

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	4	SCLK stuck low. No SPI communication with device possible.	B
$\overline{CS}$	1	$\overline{CS}$ stuck low. Normal operation. SPI communication still functional. However, SPI of device cannot be actively reset anymore by taking $\overline{CS}$ high and low again.	C
GND	2	No effect. Normal operation.	D
VDD	5	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
SIO	3	SIO stuck low. No SPI communication back to SPI master possible. Increase in supply current when SIO tries to drive high. Device damage plausible if SIO drives high for extended period of time.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	4	State of SCLK input undetermined. No SPI communication with device possible.	B
$\overline{CS}$	1	State of $\overline{CS}$ input undetermined. SPI communication corrupted.	B
GND	2	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
VDD	5	Device functionality undetermined. Device unpowered if all external analog and digital pins are held low. Device may power up through internal ESD diodes to VDD if voltages above the device's power-on reset threshold are present on any of the analog or digital pins.	B
SIO	3	State of SIO output undetermined. No SPI communication back to SPI master possible.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	4	VDD	SCLK stuck high. No SPI communication with device possible.	B
$\overline{CS}$	1	GND	$\overline{CS}$ stuck low. Normal operation. SPI communication still functional. However SPI of device cannot be actively reset anymore by taking $\overline{CS}$ high and low again.	C
GND	2	$\overline{CS}$	If $\overline{CS}$ is low then normal operation. If $\overline{CS}$ is high then device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
VDD	5	SCLK	If SCLK is high then normal operation. If SCLK is low then device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
SIO	3	GND	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when SIO tries to drive high. Device damage plausible if this condition exists for extended period of time.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	4	SCLK stuck high. No SPI communication with device possible.	B
$\overline{CS}$	1	$\overline{CS}$ stuck high. No SPI communication with device possible	B
GND	2	Device functionality undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
VDD	5	No effect. Normal operation.	B
SIO	3	SIO stuck high. No SPI communication back to SPI master possible. Increase in supply current when SIO tries to drive low. Device damage plausible if SIO drives low for extended period of time.	B

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