Functional Safety Information

TCAN1463-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

List of Figures

List of Tables

Trademarks

1 Overview

This document contains information for TCAN1463-Q1, a controller area network (CAN) transceiver with Signal Improvement Capability (SIC), to aid in a functional safety system design. The TCAN1463-Q1comes in the SOIC (D) , VSON (DMT) and SOT (DYY) packages. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

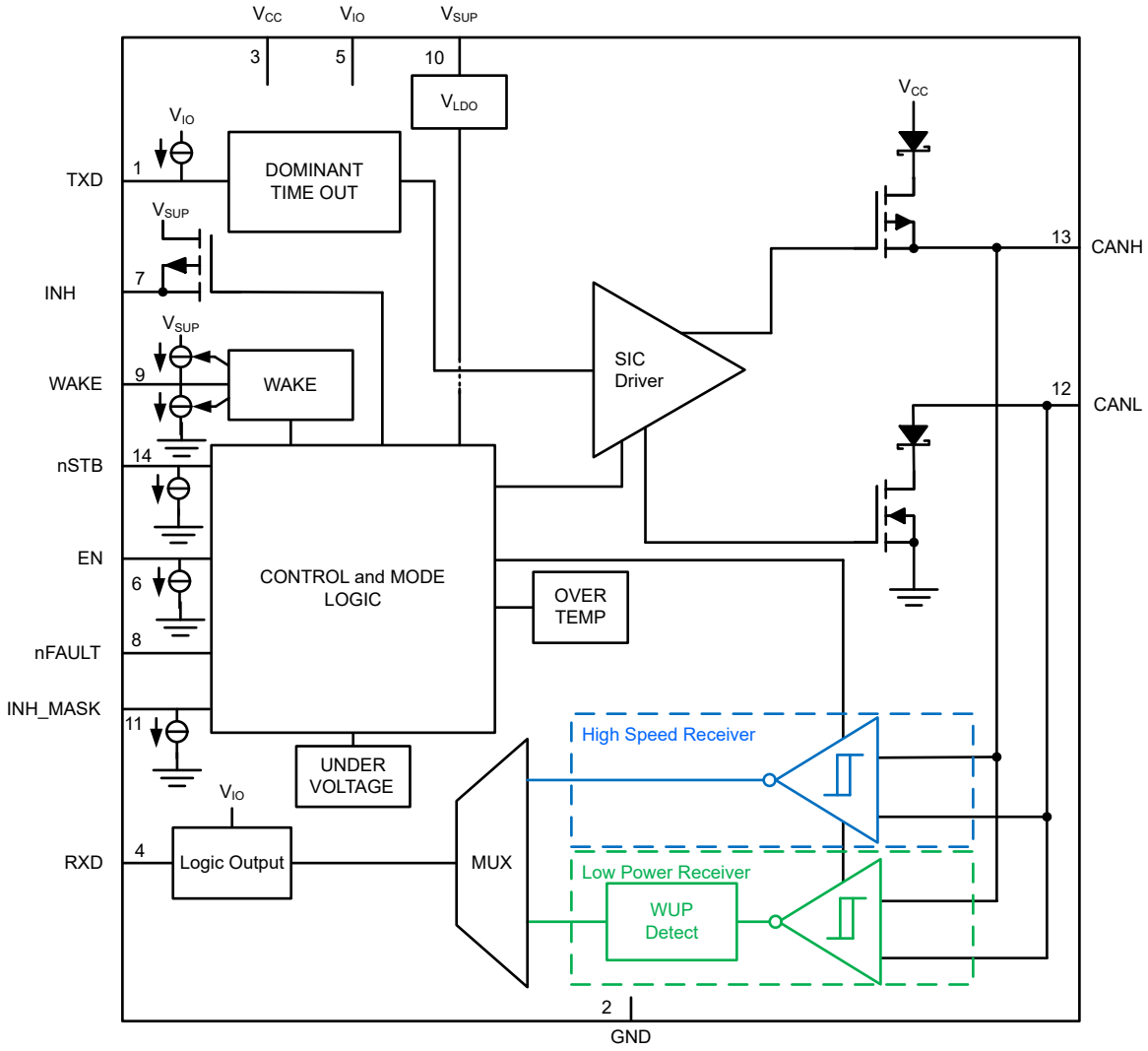

Figure 1-1. Functional Block Diagram

TCAN1463-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCAN1463-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 14-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 14-pin VSON (DMT)	FIT (Failures Per 10^9 Hours) 14-pin SOT (DYY)
Total Component FIT Rate	22	10	11
Die FIT Rate	6	4	7
Package FIT Rate	16	6	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 353 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed ≤ 50 V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1463-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	35%
Transmitter fail	35%
System stuck in sleep mode	15%
Control and Mode logic failure	10%
CANL or CANH driver stuck dominant	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCAN1463-Q1 . The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{SUP} (see Table 4-5)
- Pin short-circuited to V_{CC} (see Table 4-6)
- Pin short-circuited to V_{IO} (see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TCAN1463-Q1 pin diagram for the SOIC and SOT packages. Figure 4-2 shows the TCAN1463-Q1 VSON pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN1463-Q1 data sheet.

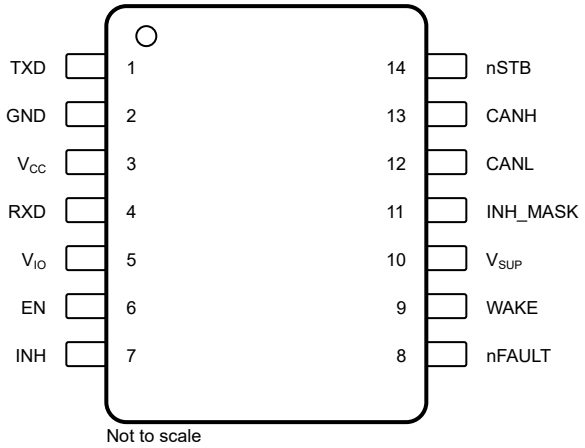

Figure 4-1. TCAN1463-Q1 SOIC/SOT Pin Diagram

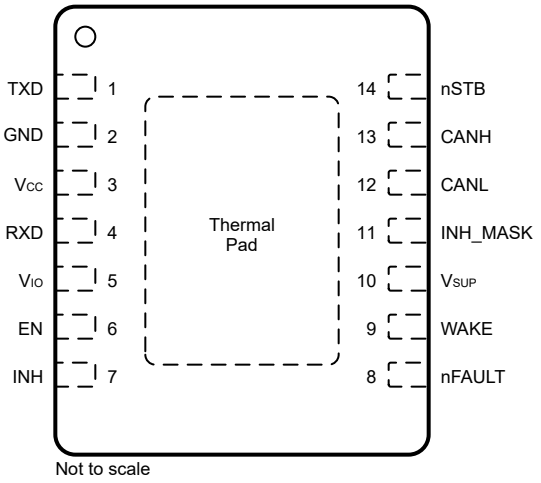

Figure 4-2. TCAN1463-Q1 VSON Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{CC} = 4.5 V to 5.5 V
- V_{SUP} = 4.5 V to 40 V
- V_{IO} = 1.7 V to 5.5 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be biased dominant indefinitely and device will enter dominant time out mode. Unable to transmit data.	B
GND	2	None	D
V_{CC}	3	Device will be in protected mode, high current draw from external regulator supplying V_{CC}.	B
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
V_{IO}	5	Device will be in protected mode. Transceiver passive on bus, and high current draw from external regulator supplying V_{IO}.	B
EN	6	EN pin biased low, device will not be able to enter normal mode. Unable to communicate.	B
INH	7	High I_{SUP} current, INH pin may be damaged and indication from sleep mode transition not available.	A
nFAULT	8	nFAULT pin biased low indefinitely which indicates a fault indefinitely.	B
WAKE	9	WAKE pin biased low indefinitely, will not be able to utilize local wake-up function.	B
V_{SUP}	10	Device unpowered, high I_{SUP} current.	B
INH_MASK	11	Inhibit mask functionality cannot be used as intended	B
CANL	12	$V_{O(REC)}$ spec violated. Degraded EMC performance.	C
CANH	13	Device cannot drive dominant to the bus, no communication possible.	B
nSTB	14	nSTB biased low indefinitely, transceiver unable to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD pin defaults to a recessive bias, device is always recessive and unable to transmit data.	B
GND	2	Device unpowered.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC}	3	Device in protected mode.	B
RXD	4	No RXD output, unable to receive data.	B
V_{IO}	5	Device in protected mode.	B
EN	6	EN pin defaults to a logic-low bias, device will not be able to enter normal mode. Unable to communicate.	B
INH	7	None	D
nFAULT	8	No effect on performance, unable to monitor system faults.	B
WAKE	9	No effect on device performance, will not be able to utilize local wake-up function.	B
V_{SUP}	10	Device unpowered.	B
INH_MASK	11	Inhibit masking functionality cannot be used as intended.	B
CANL	12	Device cannot drive dominant on bus, unable to communicate.	B
CANH	13	Device cannot drive dominant on bus, unable to communicate.	B
nSTB	14	nSTB defaults to a logic-low bias, device will not be able to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	TXD will be biased dominant indefinitely and device will enter dominant time out mode. Unable to transmit data.	B
GND	2	V_{CC}	Device will be in protected mode, high I_{CC} current.	B
V_{CC}	3	RXD	RXD output biased recessive indefinitely, controller unable to receive data from CAN bus.	B
RXD	4	VIO	RXD output biased recessive indefinitely, controller unable to receive data from CAN bus.	B
V_{IO}	5	EN	EN pin biased high indefinitely, device will be unable to enter standby and silent mode.	B
EN	6	INH	Absolute maximum violation on EN pin except in sleep mode. Transceiver may be damaged.	A
nFAULT	8	WAKE	Potential absolute maximum violation on nFAULT pin if WAKE is biased high. Transceiver may be damaged.	A
WAKE	9	V_{SUP}	WAKE biased high indefinitely, unable to utilize local wake-up function.	B
V_{SUP}	10	INH_MASK	Absolute maximum violation on INH_MASK pin, transceiver may be damaged.	A
INH_MASK	11	CANL	If INH_MASK is at V_{IO} level, I_{OS} current may be reached, RXD always recessive. If INH_MASK is at logic low, $V_{O(REC)}$ spec violated. Degraded EMC performance.	B
CANL	12	CANH	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANH/CANL.	B
CANH	13	nSTB	Driver and receiver turn off when the CAN bus is recessive. May not enter normal mode.	B

Note

The VSON package includes a thermal pad. All devices pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{SUP}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, transceiver may be damaged.	A
GND	2	Device unpowered, high I_{SUP} current.	B
V_{CC}	3	Absolute maximum violation, transceiver may be damaged.	A
RXD	4	Absolute maximum violation, transceiver may be damaged.	A
V_{IO}	5	Absolute maximum violation, transceiver may be damaged.	A
EN	6	Absolute maximum violation, transceiver may be damaged.	A
INH	7	Minimal current driven into the INH pin.	D
nFAULT	8	Absolute maximum violation, transceiver may be damaged.	A
WAKE	9	WAKE biased high, unable to utilize local wake-up function.	B
V_{SUP}	10	None	D
INH_MASK	11	Absolute maximum violation, transceiver may be damaged.	A
CANL	12	I_{OS} current may be reached. RXD always recessive.	B
CANH	13	$V_{O(REC)}$ spec violated, degraded EMC performance and communcation errors may result as well.	C
nSTB	14	Absolute maximum violation, transceiver may be damaged.	A

Note

The VSON package includes a thermal pad.

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device unpowered, high current draw from external regulator supplying VCC.	B
V_{CC}	3	None	D
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
V_{IO}	5	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if V_{CC} > VIO.	C
EN	6	EN biased high indefinitely, device will be unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on V_{CC} pin, INH will be biased at V_{CC} voltage, system may not wake up.	A
nFAULT	8	nFAULT biased high indefinitely, transceiver unable to report faults.	B
WAKE	9	None	D
V_{SUP}	10	Absolute maximum violation on V_{CC}.	A
INH_MASK	11	Inhibit masking functionality will be activated when the device enters Silent mode. Microcontroller may get damaged if V_{CC} > V_{IO}	B
CANL	12	I_{OS} current may be reached, RXD always recessive.	B
CANH	13	$V_{O(REC)}$ spec violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely, transceiver unable to enter standby and sleep mode.	B

Note

The VSON package includes a thermal pad.

Table 4-7. Pin FMA for Device Pins Short-Circuited to V_{IO}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device unpowered, high current draw from external regulator supplying VIO.	B
V_{CC}	3	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if V_{CC} > VIO.	C
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
V_{IO}	5	None	D
EN	6	EN biased high indefinitelyf, device will be unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on V_{IO} pin, INH will be biased at V_{IO} voltage, system may not wake up.	B
nFAULT	8	nFAULT biased high indefinitely, transceiver unable to report faults.	B
WAKE	9	None	D
V_{SUP}	10	Absolute maximum violation on V_{IO}.	A
INH_MASK	11	Inhibit masking functionality will be activated when the device enters Silent mode.	D
CANL	12	I_{OS} current may be reached, RXD always recessive.	B
CANH	13	$V_{O(REC)}$ spec violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely, transceiver unable to enter standby and sleep mode.	B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265