Functional Safety Information

LM36x5C-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for the LM36x5C-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

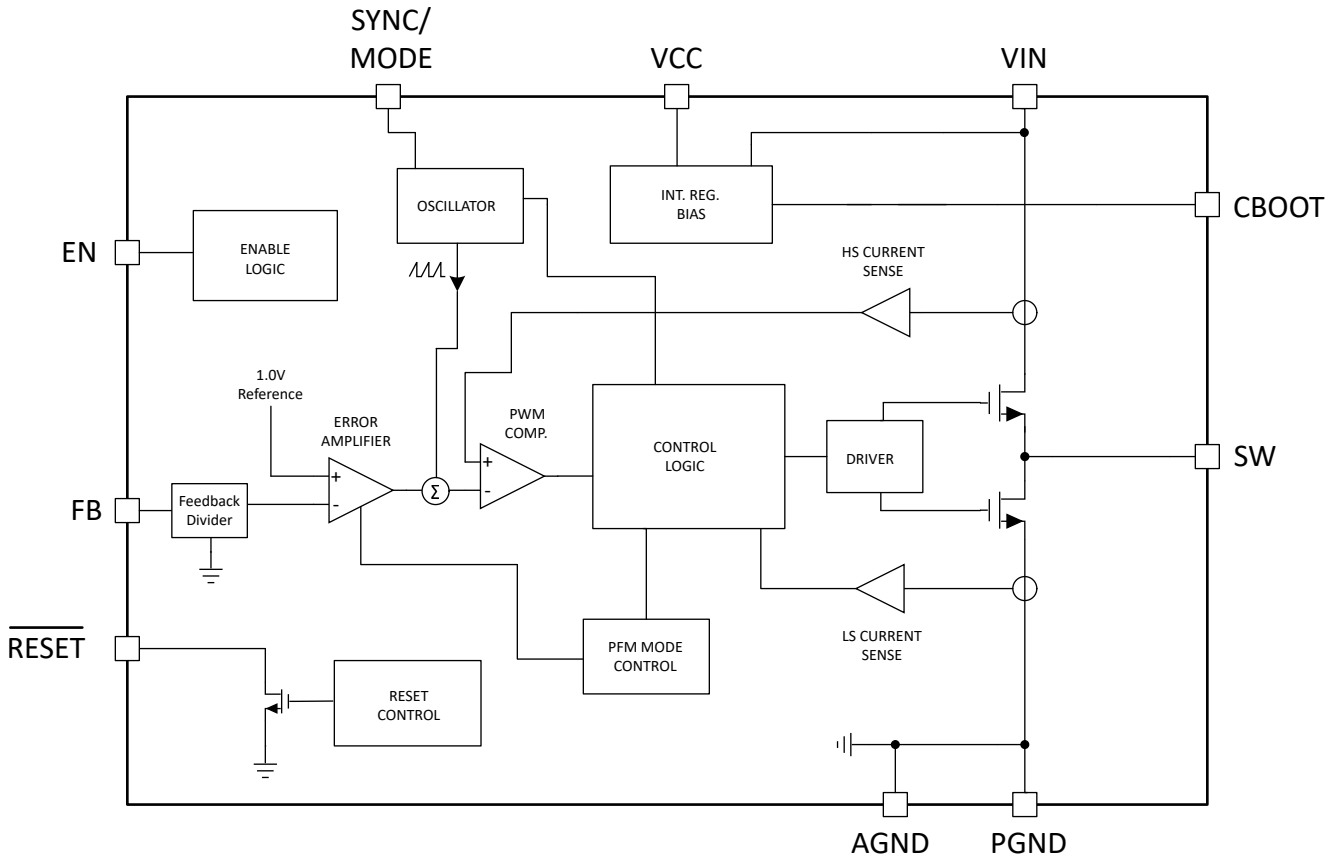

Figure 1-1. Functional Block Diagram

The LM36x5C-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the WSON package of the LM36x5C-Q1 based on the followingtwo different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	7
Package FIT Rate	5

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 600 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM36x5C-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	35%
Output not in specification -- voltage or timing	45%
SW driver FET stuck on	10%
$\overline{\text{RESET}}$ false trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM36x5C-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (Table 4-3)
- Pin short-circuited to an adjacent pin (Table 4-4)
- Pin short-circuited to VIN (Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in both LM636x5-Q1 data sheet.
- Configuration as shown in the *Example Application Circuit* found in the LM636x5-Q1 data sheet.

Figure 4-1 shows the LM36x5C-Q1 pin diagram for the WSON package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM636x5-Q1 data sheet.

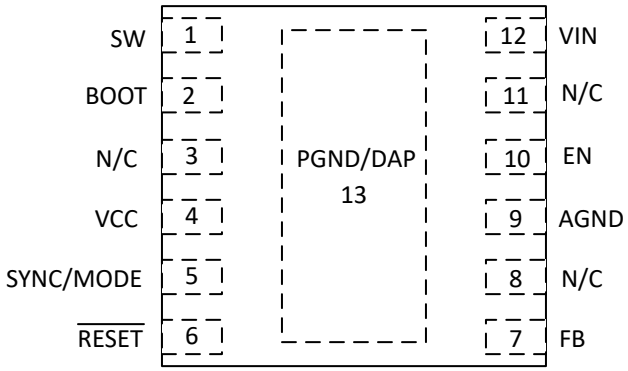

Figure 4-1. Pin Diagram for DRR0012E (WSON-12)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
N/C	3	No effect	D
VCC	4	Fault mode shuts the device off.	B
SYNC/MODE	5	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, no effect is produced. If a 0Ω jumper is used to connect the SYNC/MODE input to VCC, then the VCC output is pulled to ground; *see short to ground on pin 4*.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ functionality is lost.	B
FB	7	The regulator operates at the maximum duty cycle. The output voltage rises to nearly the input voltage (V_{IN}) level. Possible damage to customer load, output stage components, or both, can occur. No effect on the device.	B
N/C	8	No effect	D
AGND	9	No effect	D
EN	10	Loss of ENABLE functionality The device remains in shutdown mode.	B
N/C	11	No effect	D
VIN	12	The device does not operate. No output voltage is generated. Output capacitors discharge through input short. Large reverse current can damage device.	A
PGND	13	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Loss of output voltage	B
BOOT	2	Loss of output voltage regulation; low or no output voltage. Damage to the internal device.	A
N/C	3	No effect	D
VCC	4	VCC LDO is unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
SYNC/MODE	5	Internal pulldown places the device in auto mode.	B
$\overline{\text{RESET}}$	6	Loss of $\overline{\text{RESET}}$ functionality	B
FB	7	Loss of output voltage regulation. Output voltage can rise or fall outside of intended regulation window. Possible damage to the customer load.	B
N/C	8	No effect	D
AGND	9	Loss of output voltage regulation. Possible damage to the internal circuits.	A
EN	10	Loss of ENABLE functionality. Erratic operation; probable loss of regulation	B
N/C	11	No effect	D
VIN	12	Loss of output voltage	B
PGND	13	Possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	BOOT	Loss of output regulation, possible damage to internal circuits	A
BOOT	2	N/C	No effect	D
N/C	3	VCC	No effect	D
VCC	4	SYNC/MODE	Depends on exact application configuration. For application circuit as shown in the *Example Application Circuit* in the device data sheet, VCC is shorted to ground; see "short to ground on pin 4." For all other configurations, the effect is FPWM mode; loss of auto mode function.	B
SYNC/MODE	5	$\overline{\text{RESET}}$	Depends on exact application configuration. For the application circuit as shown in the *Example Application Circuit* in the device data sheet, $\overline{\text{RESET}}$ is shorted to ground; *see short to ground on pin 6*. For all other configurations, the effect is either no change or erratic operation, loss of $\overline{\text{RESET}}$, SYNC/MODE functionality, or both with possible damage to device internal circuits	A
FB	7	N/C	No effect	D
N/C	8	AGND	No effect	D
AGND	9	EN	Loss of enable function. The devices shut down.	B
EN	10	N/C	No effect	D
N/C	11	VIN	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET or FETs, other internal circuits, or both	A
BOOT	2	Damage to internal circuits	A
N/C	3	No effect	D
VCC	4	Damage to internal circuits for V_{IN} > 5.5V	A
SYNC/MODE	5	Depends on exact application configuration. For application circuit as shown in the *Example Application Circuit* in the device data sheet, no damage occurs. For all other configurations, damage to internal circuits occurs for V_{IN} > 5.5V.	A
$\overline{\text{RESET}}$	6	Damage to internal circuits	A
FB	7	Damage to internal circuits	A
N/C	8	No effect	D
AGND	9	Possible damage to internal circuits or package	A
EN	10	No damage to device. Loss of ENABLE functionality	B
N/C	11	No effect	D
VIN	12	No effect	D
PGND	13	Possible damage to internal circuits or package	A

5 Revision History

Changes from Revision * (June 2022) to Revision A (March 2024)	Page
• Updated document title	2
• Changed *SW output* to *No output voltage* in Failure Mode Distribution (FMD) section	4
• Changed *SW output not in specification* to *Output not in specification*in Failure Mode Distribution (FMD) section	4
• Corrected typo in Failure Mode Distribution (FMD) section	4

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