Functional Safety Information

TPS3435, TPS3436, TPS35, and TPS36 Functional Safety FIT Rate, FMD and Pin FMA for Pinout C

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1 Overview

This document contains information for TPS3435, TPS3436, TPS35, and TPS36, (DDF package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

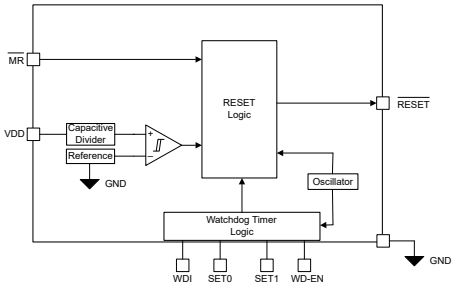

Figure 1-1. TPS35 and TPS36 Pinout Option C

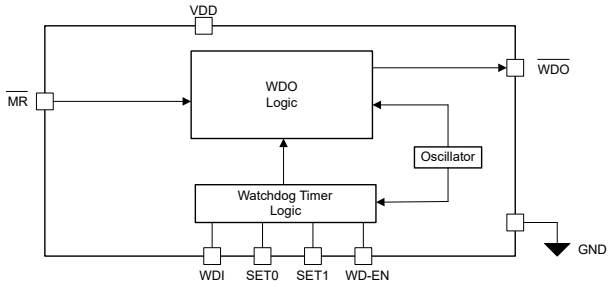

Figure 1-2. TSP3435 and TPS3436 Pinout Option C

TPS3435, TPS3436, TPS35, and TPS36 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS3435, TPS3436, TPS35, and TPS36 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 364 µW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3435, TPS3436, TPS35, and TPS36 in Table 3-1 and Table 3-2 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution TPS35 and TPS36

Die Failure Modes	Failure Mode Distribution (%)
False Assert on Reset or WDO	1%
RESET or WDO remain asserted	3%
Incorrect Timing Operation (Early or late WDO faults, Reset/WDO de-assertion delays)	66%
Reset Trip outside of specification.	24%
Supply Current is out of spec	6%

Table 3-2. Die Failure Modes and Distribution TPS3435 and TPS3436

Die Failure Modes	Failure Mode Distribution (%)
False Assert on Reset or WDO	1%
RESET or WDO remain asserted	4%
Incorrect Timing Operation (Early or late WDO faults, Reset/WDO de-assertion delays)	87%
Supply Current is out of spec	8%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3435, TPS3436, TPS35, and TPS36. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-3)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 and Figure 4-2 show the TPS3435, TPS3436, TPS35, and TPS36 pin diagrams. For a detailed description of the device pins please refer to *TPS3435,TPS3436,TPS35, or TPS36* in the *Pin Configuration and Functions* section of the data sheet.

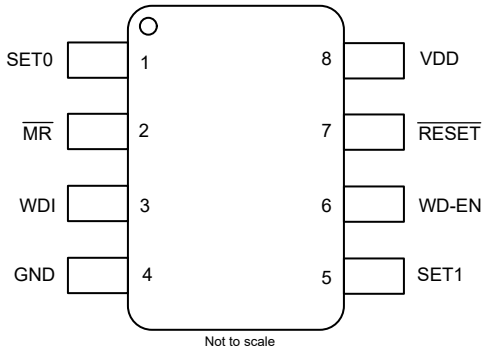

Figure 4-1. Pin Configuration Option C DDF Package, 8-Pin SOT-23, TPS35 and TPS36 Top View

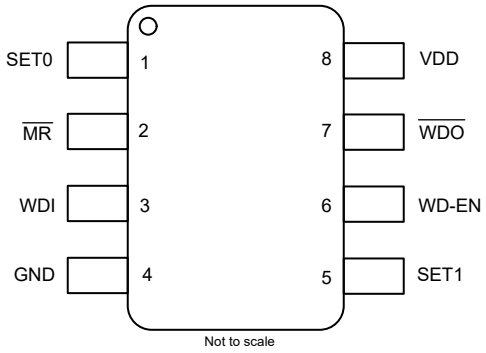

Figure 4-2. Pin Configuration Option C DDF Package, 8-Pin SOT-23, TPS3435 and TPS3436 Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset pullup voltage (V_{PULLUP} = 5.5 V, output reset load (C_{LOAD}) = 10 pF.
- Tables valid over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted.
- Typical values are at T_A = 25°C, VDD = 6.0 V unless stated otherwise.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
SET0	1	Unexpected behavior if application needs SET0 = 1.	B
$\overline{MR}$	2	$\overline{RESET}$/$\overline{WDO}$ is asserted.	B
WDI	3	Constant WD timeout faults.	B
GND	4	Expected operating condition.	D
SET1	5	Unexpected behavior if application needs SET1 = 1.	B
WD-EN	6	Leads to large indeterminate voltage levels. This causes large currents that can damage the device. The output behavior is not deterministic.	A
$\overline{WDO}$ / $\overline{RESET}$(Open Drain)	7	$\overline{WDO}$ / $\overline{RESET}$ constantly asserted; some additional current can flow through pullup resistor.	B
$\overline{WDO}$ / $\overline{RESET}$(Push Pull)	7	Functionality lost and can cause permanent damage.	A
VDD	8	Device non-operational.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
SET0	1	Leads to large indeterminate voltage levels. This causes large currents that can damage the device. The output behavior is not deterministic.	A
$\overline{MR}$	2	Device can not pass $\overline{MR}$ to $\overline{RESET}$.	B
WDI	3	Nothing happens until error condition, then reset delay is 2 mS.	C
GND	4	Device is non-operational.	B
SET1	5	Leads to large indeterminate voltage levels. This causes large currents that can damage the device. The output behavior is not deterministic.	A
WD-EN	6	Nothing happens until error condition or power cycle, then WD is disabled.	B
$\overline{WDO}$ / $\overline{RESET}$(Open Drain)	7	Constant high, no $\overline{WDO}$/$\overline{RESET}$ functionality.	B
$\overline{WDO}$ / $\overline{RESET}$(Push Pull)	7	High impedance output, no $\overline{WDO}$/$\overline{RESET}$ functionality.	B
VDD	8	Device is non-operational.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
SET0	1	$\overline{MR}$	High current at a system level can flow to the device driving $\overline{MR}$ or SET0.	B
$\overline{MR}$	2	WDI	High current at a system level can flow to the device driving $\overline{MR}$ or WDI.	B
WDI	3	GND	Constant WD timeout faults.	B
GND	4	SET1	Unexpected behavior if application needs SET1 = 1.	B
SET1	5	WD-EN	SET1 toggles with WD-EN.	B
WD-EN	6	$\overline{WDO}$ / $\overline{RESET}$(Open Drain)	High current can flow from WD-EN or $\overline{WDO}$ / $\overline{RESET}$ based on the pullup resistor value.	B
WD-EN	6	$\overline{WDO}$ / $\overline{RESET}$(Push Pull)	Can cause permanent damage.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
$\overline{\text{WDO}}$ / $\overline{\text{RESET}}$(Open Drain)	7	VDD	Large current can flow into WDO/RESET when in error condition. This can cause permanant damage.	A
$\overline{\text{WDO}}$ / $\overline{\text{RESET}}$(Push Pull)	7	VDD	Can cause permanent damage.	A
VDD	8	SET0	Unexpected behavior if application needs SET0 = 0.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
SET0	1	Unexpected behavior if application needs SET0 = 0.	B
$\overline{\text{MR}}$	2	High current can flow into the device driving $\overline{\text{MR}}$.	B
WDI	3	Constant WD timeout faults.	B
GND	4	Device is non-operational.	B
SET1	5	Unexpected behavior if application needs SET1 = 0.	B
WD-EN	6	Watchdog is always enabled, loss of WD-disable functionality.	B
$\overline{\text{WDO}}$ / $\overline{\text{RESET}}$(Open Drain)	7	Large current can flow into WDO/RESET when in error condition. This can cause permanant damage.	A
$\overline{\text{WDO}}$ / $\overline{\text{RESET}}$(Push Pull)	7	Can cause permanent damage.	A
VDD	8	Normal operation.	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265