Functional Safety Information

TMCS1126-Q1
Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TMCS1126-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

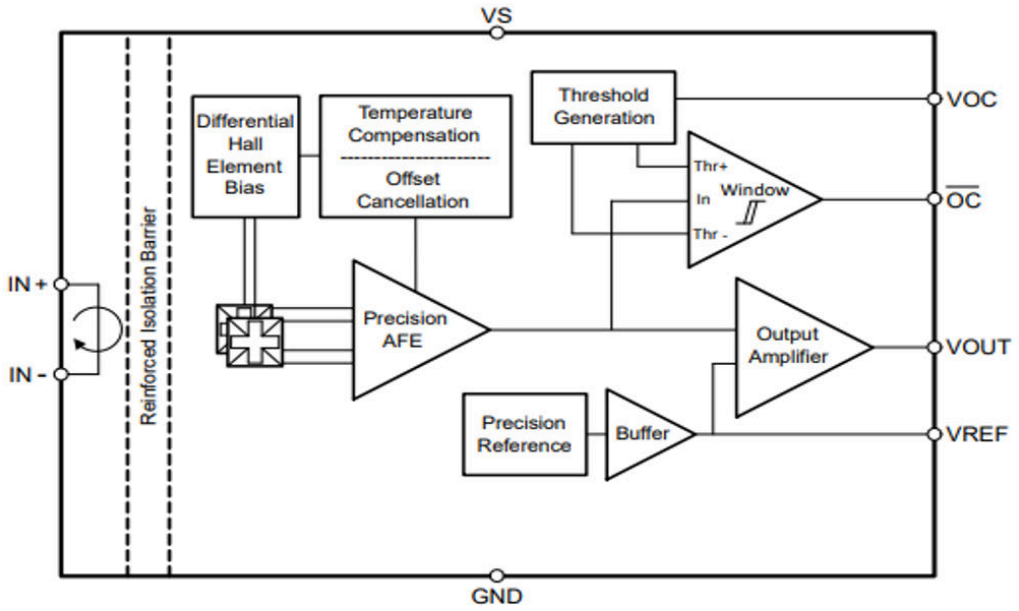

Figure 1-1. TMCS1126-Q1 Functional Block Diagram

The TMCS1126-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TMCS1126-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	62
Die FIT Rate	26
Package FIT Rate	36

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 4500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed = < 50V supply	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TMCS1126-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (High-Z)	10
VOUT Stuck (high or low)	20
VOUT functional, not in specification	20
VREF open (High-Z)	10
VREF Stuck (high or low)	10
VREF functional, not in specification	10
$\overline{OC}$ false trip, failure to trip	20

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TMCS1126-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TMCS1126-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS1126-Q1 data sheet.

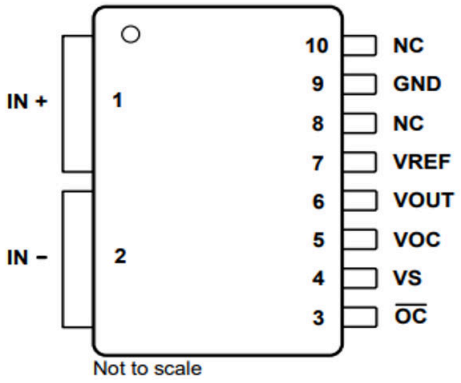

Figure 4-1. TMCS1126-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A= -40°C to +125°C
- V_S= 3V to 5.5V
- V_{CM}= -1.3kV to 1.3kV
- VREF = 0V to V_S

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	For forward current, hall-sensor bypassed, providing no signal to be sensed and amplified. If IN+ is at a large potential above GND, this will result in a lot of current being sunk. Depending upon layout and configuration, this could damage the input current system supply, the load device, or the IC itself.	A
IN-	2	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If IN- is at a large potential above GND, this will result in a lot of current being sunk. Depending upon layout and configuration, this could damage the input current system supply, the load device, or the IC itself.	A
$\overline{OC}$	3	The alert will not be able to trigger since it would be shorted to GND.	B
VS	4	Power supply shorted to ground.	B
VOC	5	Threshold at GND means that all voltages trip the alert. As a result, the alert is stuck in active mode.	B
VOUT	6	Output pulled to GND and output current will be short circuit limited. When left in this configuration while VS connected to a high load capable supply and for certain high load conditions through the IN+ and IN- pins, die temperature could approach or exceed 150°C.	A
VREF	7	VREF shorted to GND and output current will be short circuit limited.	B
NC	8	Normal operation.	D
GND	9	Normal operation.	D
NC	10	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	No current running through inputs.	B
IN-	2	No current running through inputs.	B
$\overline{OC}$	3	Alert open; cannot read alert.	B
VS	4	No power to device. Vout will stay close to GND.	B
VOC	5	No alert threshold set. Alert output will be unpredictable.	B
VOUT	6	Output will be present at the pin; having no loading will not affect the output. However, the user will see unpredictable results further down on the signal chain.	B
VREF	7	VREF will be present at the pin; No loading will not affect the device. However, the user will see unpredictable results further down on the signal chain.	B
NC	8	Normal operation.	D
GND	9	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
NC	10	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	IN-	IN+ shorted to IN-. This creates a current divider which increases sensitivity error inversely proportional to the resistance of the short.	C
IN-	2	$\overline{OC}$	IN- shorted to $\overline{OC}$. If IN->6V, the device will be damaged. If IN- < OC, large current may be pulled from VS.	A
$\overline{OC}$	3	VS	$\overline{OC}$ shorted to VS. Large current may be pulled from VS.	A
VS	4	VOC	VOC shorted to VS; over current threshold will be at the wrong threshold.	B
VOC	5	VOUT	VOC shorted to VOUT. Over current threshold will vary, alert response will be unpredictable.	B
VOUT	6	VREF	Output shorted to VREF. Based on the voltage level of each, the output current may be short circuit limited. When left in this configuration while VS connected to a high load capable supply and for certain high load conditions through the IN+ and IN- pins, die temperature could approach or exceed 150°C.	A
VREF	7	NC	VREF either left open or shorted to VS or GND depending on NC pin connection.	D if NC is open; B otherwise
NC	8	GND	If NC at GND or open then operation is normal. If NC at VS, then VS is shorted to GND.	B if NC is at VS; D otherwise
GND	9	NC	If NC at GND or open then operation is normal. If NC at VS, then VS is shorted to GND.	B if NC is at VS; D otherwise
NC	10	IN+	If IN+> 6V, the device may be damaged. If NC is at VS and IN+ < Vs or if NC is at GND and IN+ is at a large potential above ground, large current may be flowing between VS and the input current system supply.	A if IN+>6V; B otherwise

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	If IN+>6V, the device will be damaged. If IN+ < Vs, a lot of current may be pulled from VS.	A
IN-	2	If IN->6V, the device will be damaged. If IN- < Vs, a lot of current may be pulled from VS.	A
$\overline{OC}$	3	$\overline{OC}$ pin stuck high; may have too high of a current draw when triggered.	B
VS	4	Normal operation.	D
VOC	5	Over current threshold at the wrong threshold.	B
VOUT	6	Output pulled to VS and output current will be short circuit limited. When left in this configuration while VS connected to a high load capable VS and for certain high load conditions through the IN+ and IN- pins, die temperature could approach or exceed 150°C.	A
VREF	7	VREF pulled to VS and output current will be short circuit limited.	B
NC	8	Normal operation.	D
GND	9	VS shorted to GND.	B
NC	10	Normal operation.	D

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