Functional Safety Information TCAN844-Q1 and TCAN844V-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

TEXAS INSTRUMENTS

Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
3 Failure Mode Distribution (FMD)	. 4
4 Pin Failure Mode Analysis (Pin FMA)	5
	••••

List of Figures

Figure 1-1. TCAN844-Q1 and TCAN844V-Q1 Functional Block Diagram	2
Figure 4-1. SOIC (D) Pin Diagram	5
Figure 4-2. VSON (DRB) Pin Diagram	5
Figure 4-3. SOT (DDF) Pin Diagram	6

List of Tables

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11	3
Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2	3
Table 3-1. Die Failure Modes and Distribution	4
Table 4-1. TI Classification of Failure Effects	5
Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground	6
Table 4-3. Pin FMA for Device Pins Open-Circuited	7
Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin	7
Table 4-5. Pin FMA for Device Pins Short-Circuited to V _{CC}	7
Table 4-6. Pin FMA for Device Pins Short-Circuited to V _{BAT}	8
Table 4-7. Pin FMA for Device Pins Short-Circuited to Vin	8

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for TCAN844-Q1 and TCAN844V-Q1. These are controller area network (CAN) transceivers. The TCAN844-Q1 and TCAN844V-Q1 come in the SOIC (D), VSON (DRB), and SOT (DDF) packages to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- · Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA) for the device pins of TCAN844-Q1 and TCAN844V-Q1

Figure 1-1 shows the device functional block diagram for reference. TCAN844-Q1 has the V_{IO} input at pin 5, while TCAN844V-Q1 has a no connect (NC) at pin 5.



Figure 1-1. TCAN844-Q1 and TCAN844V-Q1 Functional Block Diagram

TCAN844-Q1 and TCAN844V-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.



2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TCAN844-Q1 and TCAN844V-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours) 8-pin SOIC (D)	FIT (Failures Per 10 ⁹ Hours) 8- pin VSON (DRB)	FIT (Failures Per 10 ⁹ Hours) 8- pin SOT (DDF)	
Total component FIT rate	10	6	5	
Die FIT rate	3	2	3	
Package FIT rate	7	4	2	

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 119mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS/BICMOS ASICs Analog and Mixed =<50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN844-Q1 and TCAN844V-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	30
Transmitter fail	40
CANL or CANH driver stuck dominant	10
Short circuit any two pins	20

Table 3-1. Die Failure Modes and Distribution



4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TCAN844-Q1 and TCAN844V-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{CC} (see Table 4-5)
- Pin short-circuited to V_{BAT} (see Table 4-6)
- Pin short-circuited to V_{IO} (Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Class	Failure Effects
A	Potential device damage that affects functionality.
В	No device damage, but loss of functionality.
С	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Table 4-1. TI Classification of Failure Effects

Figure 4-1 shows the TCAN844-Q1 and TCAN844V-Q1 (SOIC (D)) pin diagram. Figure 4-2 shows the TCAN844-Q1 and TCAN844V-Q1 (VSON (DRB)) pin diagram. Figure 4-3 shows the TCAN844-Q1 and TCAN844V-Q1 (SOT (DDF)) pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN844-Q1 and TCAN844V-Q1 data sheets.





Figure 4-2. VSON (DRB) Pin Diagram





Figure 4-3. SOT (DDF) Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- V_{CC} = 4.5V to 5.5V
- $V_{BAT} = 6V \text{ to } 24V$
- V_{IO} = 1.7V to 5.5V

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Device enters dominant time out mode. Unable to transmit data.	В
GND	2	None.	D
V _{CC}	3	Device not powered, high I _{CC} current.	В
RXD	4	RXD default is high-side FET ON, with pin short to ground, RXD forms direct path between supply and ground causing high current.	A
NC	5	None.	D
V _{IO}	5	Device is in protected mode. Transceiver is passive on bus.	В
CANL	6	V _{O(REC)} specification violated. Degraded EMC performance.	С
CANH	7	Device cannot drive dominant to the bus, no communication is possible.	В
STB	8	STB stuck low, transceiver unable to enter low-power mode.	В
Thermal Pad	-	None.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Note

The VSON (DRB) package includes a thermal pad.

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD pin defaults high, device always recessive and unable to transmit data.	В
GND	2	Device not powered.	В
V _{CC}	3	Device not powered.	В
RXD	4	No RXD output, unable to receive data.	В
NC	5	None.	D
V _{IO}	5	Device is in protected mode. Transceiver passive on bus.	В
CANL	6	Device cannot drive dominant on the bus, unable to communicate.	В
CANH	7	Device cannot drive dominant on the bus, unable to communicate.	В
STB	8	STB pin defaults high, transceiver stuck in low-power mode.	В
Thermal Pad	-	None.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Note

The VSON (DRB) package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
TXD	1	GND	Device enters dominant time out mode. Unable to transmit data.	В
GND	2	V _{CC}	Device not powered, high I _{CC} current.	В
V _{CC}	3	RXD	RXD output stuck high, unable to receive data.	В
NC	5	CANL	None.	D
V _{IO}	5	CANL	Bus stuck recessive, no communication is possible. I _{OS} current can be reached on CANL.	В
CANL	6	CANH	Bus stuck recessive, no communication is possible. I _{OS} current can be reached on CANH/CANL.	В
CANH	7	STB	Driver and receiver turn off when a dominant is driven. Not being able to enter normal mode is possible.	В

Note

The VSON (DRB) package includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD stuck high, unable to transmit data.	В
GND	GND 2 Device not powered, high I _{CC} current.		В
V _{CC} 3		None.	D
RXD	4	RXD pin stuck high, unable to receive data.	В
NC 5 None.		None.	D
V _{IO}	5	IO pins operate as 5V input and outputs. Microcontroller can be damaged if V_{CC} > V_{IO} .	С
CANL	6	RXD always recessive, no communication is possible. I _{OS} current can be reached.	В
CANH	7	V _{O(REC)} specification violated, degraded EMC performance.	С
STB	8	STB stuck high, transceiver always in standby mode.	В

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{BAT}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	Absolute maximum violation, transceiver can be damaged. Unable to transmit data.	A
GND	2	Device not powered, high I _{BAT} current	В
V _{CC}	3	Absolute maximum violation, transceiver can be damaged. Bus can be unable to communicate.	A
RXD	4	Absolute maximum violation, transceiver can be damaged. Unable to receive data.	A
NC	5	None.	D
V _{IO}	5	Absolute maximum violation, transceiver can be damaged.	A
CANL	6	RXD always recessive, no communication is possible. I _{OS} current can be reached.	В
CANH	7	V _{O(REC)} specification violated, degraded EMC performance.	С
STB	8	Absolute maximum violation, transceiver can be damaged. Transceiver stuck in low-power mode.	A

Table 4-7. Pin FMA for Device Pins Short-Circuited to $\rm V_{IO}$

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
TXD	1	TXD stuck high, unable to transmit data.	В
GND	2	Device not powered, high I _{IO} current.	В
V _{CC}	3	IO pins operate as 5V input and outputs. Microcontroller can be damaged if $V_{CC} > V_{IO}$.	С
RXD	4	RXD pin stuck high, unable to receive data.	В
NC	5	None.	D
V _{IO}	5	None.	D
CANL	6	RXD always recessive, no communication is possible. I_{OS} current can be reached is $V_{IO} \ge 3.3V$.	В
CANH	7	$V_{O(REC)}$ specification violated if $V_{IO} \ge 3.3V$, degraded EMC performance.	С
STB	8	STB stuck high, transceiver always in standby mode.	В

Note

Table 4-7 is only applicable to the TCAN844-Q1 and TCAN844V-Q1 device.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2024, Texas Instruments Incorporated