

# Coherent Sampling Solution for an Electric Power System

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## ABSTRACT

This application note discusses a coherent sampling solution for an electric power system, based on the TLV320AIC3254, SN74CD4046, and ADS131E08, an analog-front end for power monitoring, control and protection. This report offers the error analysis caused by non-coherent sampling in electric power systems and a coherent sampling solution to generate a data converter sampling clock that is locked to a frequency drifting, noisy 50- to 60-Hz power line.

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## 1 Introduction

There are two methods used in data-conversion sampling; coherent sampling and non-coherent sampling. Non-coherent sampling occurs if the sampling frequency is not an integer multiple of the sampled frequency, for this analysis, the AC power-line frequency. The level of power system accuracy is significantly influenced by the coherency of the sampling. In electronic systems, non-coherent sampling error is caused by two sources. The first source of error depends on the crystal stability in varying the modulator frequency. And the second, the voltage and current frequencies of electric systems change with time. In China, the state grid frequency changes between 49.8 Hz to 50.2 Hz. Since the crystal stability is 10 ppm, the non-coherent sampling is mainly caused by power-line frequency drift which decreases the accuracy of the power measurement. So in electric power systems, coherent sampling means that the sampling clock of the data converter needs to be synchronized with the 50- to 60-Hz, drifting, noisy power line.

## 2 Non-Coherent Sampling Error Analysis

There are several fundamental specifications in electric power system measurements; RMS current, RMS voltage, active power, reactive power, apparent power, power factor, power-line frequency, and harmonic analysis. These measurements can be simplified into 3 aspects; RMS measurement, power measurement and harmonic analysis. This section describes the non-coherent sampling error analysis on these 3 measurements.

### 2.1 RMS Error Analysis

Due to the similarity in the calculations of RMS current and RMS voltage, only RMS voltage error by non-coherent sampling is discussed in this section. Assuming there are no harmonics, the power-line voltage is given by [Equation 1](#) where  $U_m/\sqrt{2}$  is the RMS voltage.

$$U(t) = U_m \sin \omega t \quad (1)$$

With a data converter of sampling frequency of  $f_s$ ,  $N$  points are collected each period. For a single period, we define the phase error,  $\Delta\omega$ , as shown in [Equation 2](#).

$$\Delta\omega = \beta - \alpha = 2\pi f_x \left( \frac{1}{f} - \frac{1}{f_x} \right) = 2\pi \left( \frac{f_x}{f} - 1 \right) \quad (2)$$

where:

- $f_x$  is the frequency of the power line,
- $f$  is the ideal frequency (that is, 50 to 60 Hz for power-line frequencies)
- $\alpha$  is the first sample point,
- $> 2\pi + \beta$  is the last sample point

With non-coherent sampling, the sample speed can be described as [Equation 3](#).

$$\omega_s = \frac{2\pi + \beta - \alpha}{N} = \frac{2\pi + \Delta\omega}{N} \quad (3)$$

So in one period, every sample point is given by [Equation 4](#).

$$\omega_s t_n = \omega_s n + \phi, \quad n = 1, 2, \dots, N, \quad \phi = \alpha - \omega_s \quad (4)$$

Using [Equation 1](#) and [Equation 4](#), the power-line voltage in one period can be expressed as shown in [Equation 5](#).

$$u(n) = U_m \sin(\omega_s n + \phi) \quad (5)$$

To calculate RMS voltage for one period, use the equation show in [Equation 6](#).

$$\begin{aligned} U_{rms} &= \sqrt{\frac{1}{N} \sum_1^N u^2(n)} = \sqrt{\frac{U_m^2}{N} \sum_1^N \sin^2(\omega_s n + \phi)} = \frac{U_m}{\sqrt{2}} \sqrt{1 - \frac{1}{N} \sum_1^N \cos(2\omega_s n + 2\phi)} \\ &= \frac{U_m}{\sqrt{2}} \sqrt{1 - \frac{1}{N} \operatorname{Re} \left( \sum_1^N e^{j(2\omega_s n + 2\phi)} \right)} = \frac{U_m}{\sqrt{2}} \sqrt{1 - \frac{1}{N} \frac{\sin(\omega_s N)}{\sin(\omega_s)} \cos(\omega_s + \omega_s N + 2\phi)} \end{aligned} \quad (6)$$

For  $N \gg 1$  and a power-line frequency drift of  $\pm 0.2$  Hz, [Equation 6](#) can be simplified into [Equation 7](#).

$$U_{rms} = \lim_{\Delta\omega \rightarrow 0} \frac{U_m}{\sqrt{2}} \sqrt{1 - \frac{1}{N} \frac{\sin(\omega_s N)}{\sin(\omega_s)} \cos(\omega_s + \omega_s N + 2\phi)} = \frac{U_m}{\sqrt{2}} \left[ 1 - \frac{\Delta\omega}{4\pi + 2\Delta\omega} \cos(2\alpha + \Delta\omega - \omega_s) \right] \quad (7)$$

So the relative error of RMS voltage is defined as shown in [Equation 8](#).

$$r = \frac{\Delta\omega}{4\pi + 2\Delta\omega} \cos(2\alpha + \Delta\omega - \omega) \quad (8)$$

Using [Equation 8](#), we can determine the maximum relative RMS voltage error as shown in [Equation 9](#).

$$r_{rms} = \frac{\Delta\omega}{4\pi + 2\Delta\omega} \quad (9)$$

Using the electronic grid in China as a example,  $f_s = 8000$  Hz,  $f_x = 50.2$  Hz,  $f = 50$  Hz, then the maximum relative RMS voltage error caused by non-coherent sampling is 0.198%.

## 2.2 Power Error Analysis

Since active power, reactive power and apparent power are similar in calculation, only active power error is analyzed in this section. Assuming there are no harmonics, the power-line current is given in Equation 10.

$$i(t) = I_m \sin(\omega t + \varphi) \quad (10)$$

$\varphi$  is the power factor angle. The active power is calculated in Equation 11.

$$\begin{aligned} P_{act} &= \frac{1}{N} \sum_1^N u(n)i(n) = \frac{1}{N} U_m I_m \sum_1^N \sin(\omega_s n + \varphi) \sin(\omega_s n + \varphi + \phi) \\ &= \frac{U_m I_m}{2} \cos(\phi) \left[ 1 - \frac{\Delta\omega}{2\pi + \Delta\omega} \frac{\cos(2\varphi + \Delta\omega - \omega_s - \phi)}{\cos(\phi)} \right] \end{aligned} \quad (11)$$

The maximum relative active power error caused by non-coherent sampling is defined as

$$r_{act} = \frac{\Delta\omega}{2\pi + \Delta\omega} \frac{1}{\cos\phi} \quad (12)$$

If the power factor angle is zero, the active power error is minimum. Using the sample parameters from the RMS example,  $f_s = 8000$  Hz,  $f_x = 50.2$  Hz,  $f = 50$  Hz, we can determine the maximum relative error of active power caused by non-coherent sampling is 0.396%.

## 2.3 Harmonic Analysis

Based on an interpolating windowed FFT algorithm described in [The Algorithm of Interpolating Windowed FFT for Harmonic Analysis of Electric Power System](#), non-coherent sampling error for harmonic analysis is simulated using Matlab.

Using  $f_s = 8000$  Hz,  $f = 50$  Hz,  $N = 2048$ , we collect 160 points every period. This results in  $\Delta\omega = 0$ , which indicates we are sampling coherently. The maximum frequency error is 0.002%, the maximum amplitude error is 0.04%, maximum phase error is 1.2%. The simulated results are showed in Figure 1.

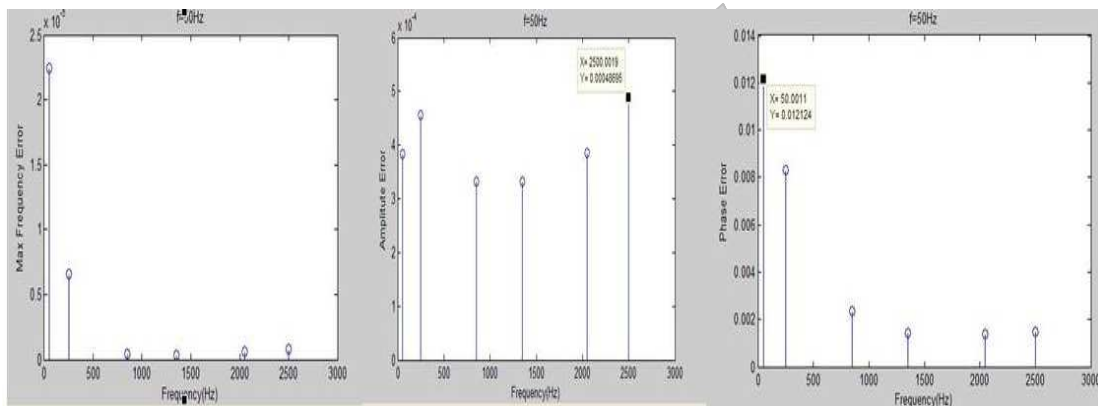
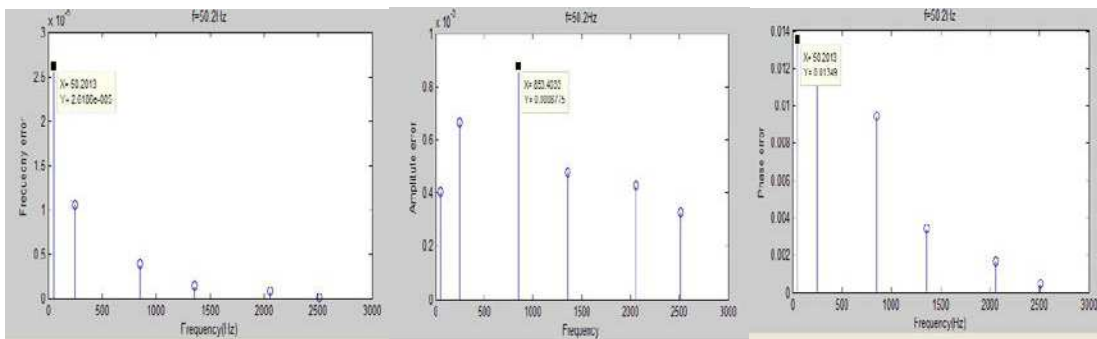


Figure 1. Simulated Results of Sampling Coherently

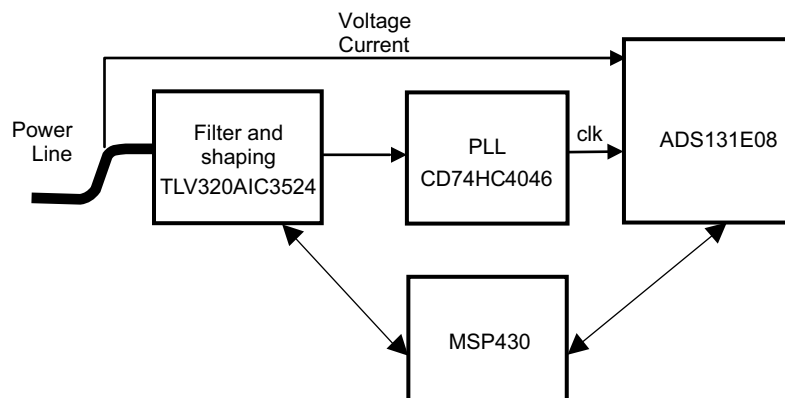
Using  $f_s = 8000$  Hz,  $f = 50.2$  Hz,  $N = 2048$ , we calculate  $\Delta\omega = 0.025$  and therefore determine we are performing non-coherent sampling. The max frequency error is 0.0026%, max amplitude error is 0.088%, maximum phase error is 1.35%. The simulated results are showed in Figure 2.



**Figure 2. Simulated Results of Sampling Non-Coherently**

### 3 Coherent Sampling Solution

For the Class 0.2S standard electricity meter, when the power factor is 1 and current is between 1% and 5% of the maximum, the error limits are  $\pm 0.4\%$ . When current is above 5% of the maximum, the error limit changes to  $\pm 0.2\%$ . From the analysis reviewed in [Section 2](#), we can know that for 0.1S and 0.2S standard meters, a coherent sampling solution is required to achieve this level of performance and accuracy. This means that sampling frequency must follow the line frequency drift. [Figure 3](#) shows a functional block diagram of a coherent sampling solution.



**Figure 3. Functional Block Diagram**

There are 4 parts in the solution:

- TLV320AIC3524 as a band-pass filter (BPF) to decrease the power-line noise and shape the power-line signal into square wave
- CD74HC4046 as a PLL to generate a modulated clock locked with square wave
- ADS131E08 samples the voltage and current signal from the power line, with the PLL-generated clock
- MSP430 performs several different functions. The first function is to configure the codec, TLV320AIC3524, and ADS131E08. The second function calculates the accurate AC line frequency from the codec square-wave output and on-board timer. Finally, the MSP430 performs the e-meter power calculations with converted data from ADS131E08. The ADS131E08 is a sigma-delta ADC, with fixed over sampling ratio. The PLL-generated modulator clock ensures the output data rate will change with the power-line frequency, providing the required coherent sampling. The codec and PLL are described in [Section 3.1](#) and [Section 3.2](#)

### 3.1 Filter and Shaping with TLV320AIC3254

Two functions are included in the front-end of the circuit. The first is to filter the power-line noise, and the second is to shape the power-line signal into square wave as the input to the CD74HC4046. The TLV320AIC3254 is an audio codec with an integrated mini-DSP, ADC and DAC. This device provides a simple and easy method to design a high order band-pass digital filter and shaping circuit in a board-efficient and cost-effective manner. Figure 4 shows the block diagram created using PurePath™ Studio Graphical Development Environment.

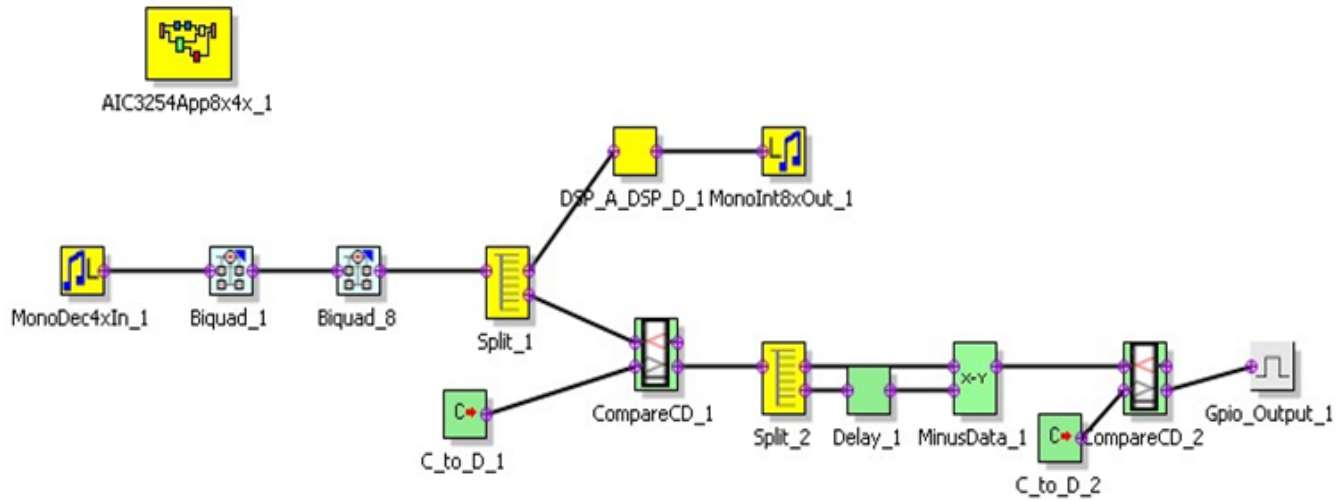


Figure 4. Block Design of the TLV320AIC3254

In the Figure 4, two blocks, Biquad\_1 and Biquad\_8, implement a 10<sup>th</sup>-order Chebyshev low-pass filter and a 10<sup>th</sup>-order Chebyshev high-pass filter, resulting in a 10 order Chebyshev band-pass filter. The filtered signal is split into two paths, one is output from the DAC, using Monolnt8xOut\_1 block in Figure 4. The other path, through the GPIO\_Output\_1 block, shapes the filtered signal into a square wave with 0.01-Hz accuracy and outputs the signal to a GPIO. The center frequency of the band-pass filter is configured as 50 Hz. Figure 5 shows the frequency response curve of the band-pass filter. The DC signal and the first harmonic is attenuated by 80 dB. The results shown were measured with Audio Precision SYS-2722 in AP2700.

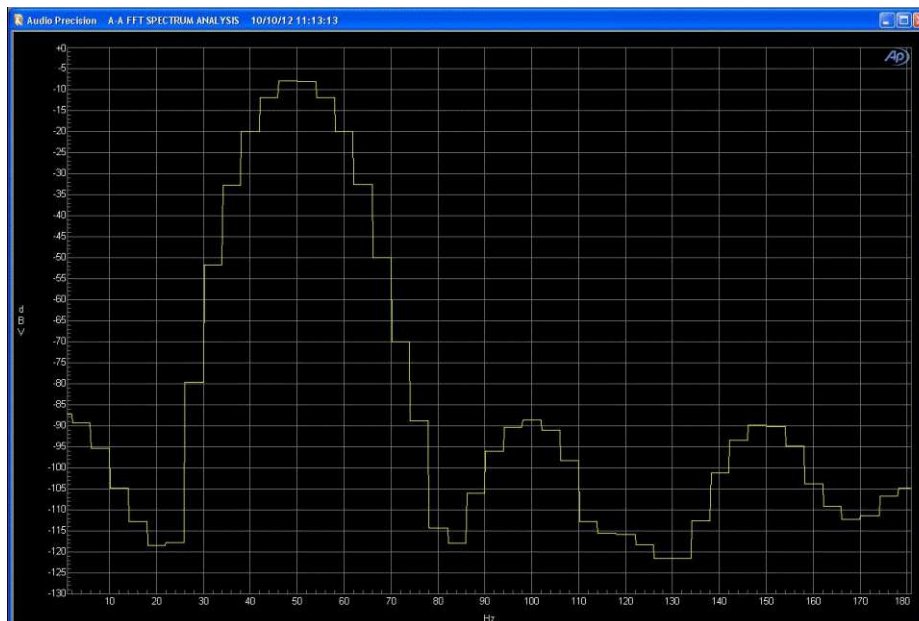


Figure 5. Frequency Response of the Filter

### 3.2 PLL Design

For coherent sampling, the ADS131E08 sample clock of 2.048 MHz follows the power-line frequency, 50 Hz. CD74HC4046 was selected for the PLL, where the input clock is about 50 Hz and the desired output clock is 2.048 MHz. This means the output clock is 40960 times the input clock, which is achieved using the HC4040 and HC390 counters. The accuracy of the power line is 0.01 Hz so the PLL is accurate to 409.6 Hz. Figure 6 shows the PLL circuit.

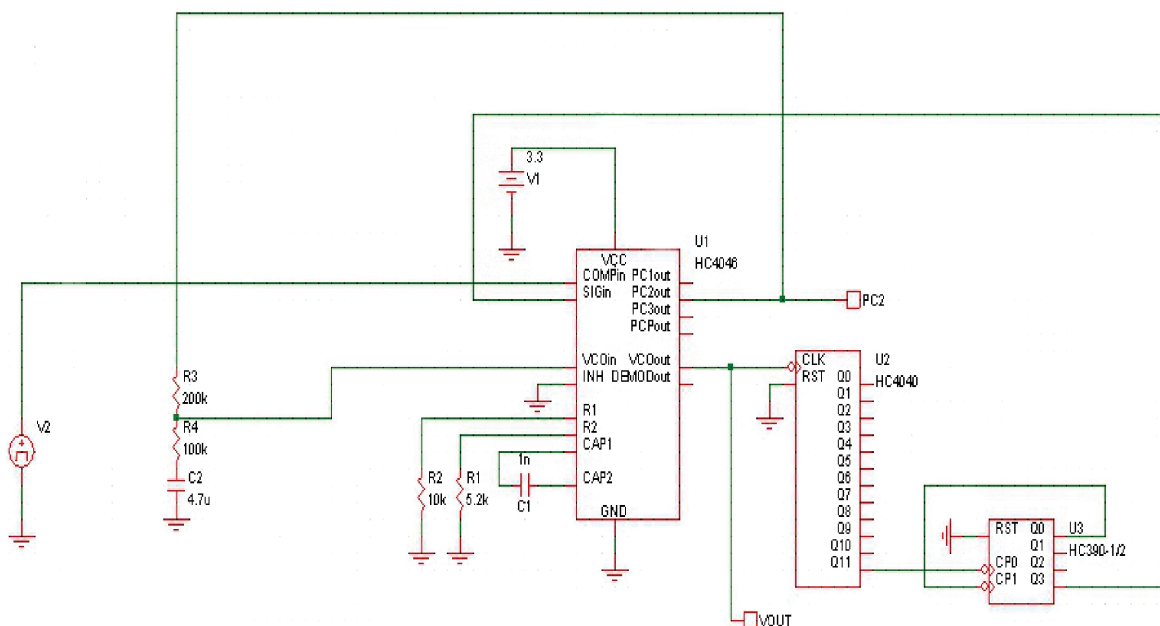
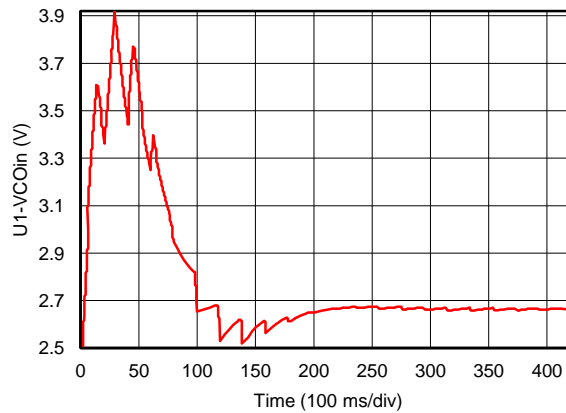


Figure 6. PLL Design Circuit

The setting time is about 250 ms, simulated in Simetrix Intro, is shown in Figure 7.



**Figure 7. Setting Time Simulation**

The power frequency drifts according to time, with 0.01-Hz minimum frequency jump. A good approximation of the time required for the PLL to lock to the input frequency is shown in Equation 13.

$$t_{lock} = \frac{4}{BW} (1 - \log \frac{f_e}{f_j}) \quad (13)$$

where:

- $t_{lock}$  is the lock time,
- BW is the loop bandwidth,
- $f_e$  is the locked frequency error,
- $f_j$  is the frequency jump.

Continuing to use the Chinese electric power system in this example, the power-line maximum frequency jump is 0.4 Hz ( $\pm 0.2$  Hz). The PLL loop bandwidth is 2 Hz and the locked frequency error is 1 Hz. From Equation 13, we calculate the maximum lock time as 1.2 seconds. In electric power systems, frequency drift is actually extremely slow and nearly impossible to change very rapidly. A typical frequency jump of 0.01 Hz occurs over several hours. Using 0.01-Hz frequency jump and a frequency error of 0.1 Hz, Equation 13 calculates the lock time as 0 seconds. Therefore, the lock time of this PLL part should be acceptable for most electric power systems.

For the 60-Hz power-line frequency, change the HC390. Connect the Q3 to the reset pin, RST. And make the Q2 as the output of the HC390. It means that the sampling clock is 32768 times 60 Hz = 1.96608 MHz.

#### 4 Summary

From this analysis, we have demonstrated that non-coherent sampling can cause relative error in e-metering and harmonic analysis in electronic power systems. In order to achieving better performance, a PLL-based coherent sampling solution was presented using the TLV320AIC3254 as a filter and the CD74HC4046 as a PLL, in order to provide a sampling clock for the ADS131E08 that is locked to the noisy power-line frequency.

#### 5 References

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5. ADS131E08 Product data sheet. Literature number [SBAS561](#).
6. CMOS Phase-Locked-Loop Applications Using the CD54/74HC/HCT4046A and CD54/74/HCT7046A, W. M. Austin. Literature number [SCHA003B](#).



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