Application Report
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Implementation of FSK Modulation and Demodulation using CD74HC4046A

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ABSTRACT

In telecommunications and signal processing, frequency modulation (FM) is encoding of information on a carrier wave by varying the instantaneous frequency of the wave. Digital data can be encoded and transmitted via carrier wave by shifting the carrier's frequency among a predefined set of frequencies—a technique known as frequency-shift keying (FSK). FSK is widely used in modems, radio-teletype and fax modems, and can also be used to send Morse code.

Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. This application report discusses logic-level implementation of binary FSK (BFSK) modulator and demodulator using a phase-locked loop PLL device – CD54HC4046A, CD54HCT4046A, CD74HC4046A, and CD74HCT4046A (hereafter in this document referred to as HC/HCT4046A). BFSK is the simplest FSK, using a pair of discrete frequencies to transmit binary information.

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1 Introduction

Many measurement applications (for example, electric and gas meters) require a way to communicate electronically with a central office so that measured data can be reported back to the central office and new tariffs can be set in the remote site. (1) Telephony provides a convenient means of data communication.

This application report discusses logic-level implementation of FSK modulator and demodulator using a PLL device HC/HCT4046A. The HC/HCT4046A, PLL with VCO is a high-speed CMOS IC designed for use in general-purpose PLL applications, including frequency modulation, demodulation, discrimination, synthesis, and multiplication.

Figure 1 illustrates the functional block diagram of a PLL IC, highlighting the following:

- The voltage controlled oscillator (VCO) generates a center frequency locally.
- The center frequency is compared with the incoming signal frequency using a phase comparator (PC)
- The PC generates an error voltage, V_d, which is fed into VCO after a low-pass filter (LPF) shifting the frequency of VCO to lock with the incoming signal.

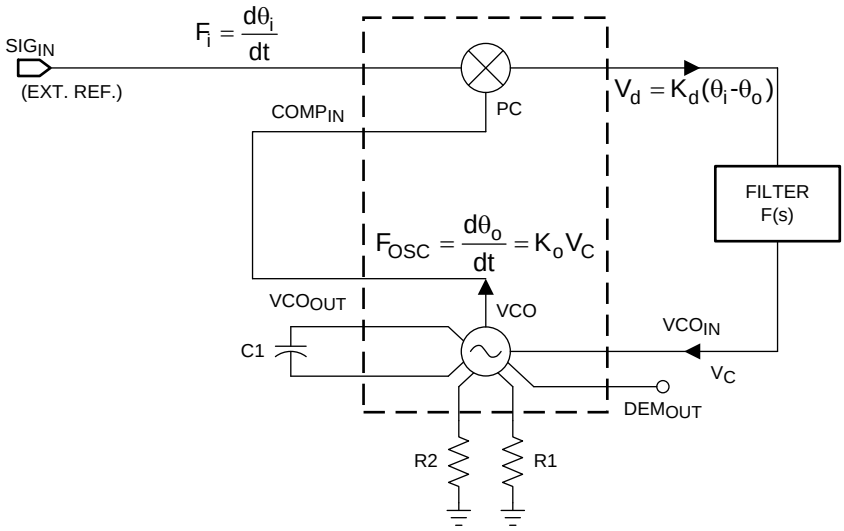


Figure 1. Block Diagram of HC/HCT4046A in a Typical PLL Circuit

(1) Schematics in this report are only for reference. Precise implementation can vary from country to country and based on the application, transmission media, and so forth.

2 Implementation of Modulator

The modulator uses only VCO, as shown in the block diagram illustrated in Figure 2. Values of R1 and C1 determine the frequency range of the VCO and center frequency of operation depends upon VCO input, which is a digital input signal level for a modulator. Hence high (bit1) and low (bit 0) voltage levels of digital input determines actual output frequencies and separation between them.

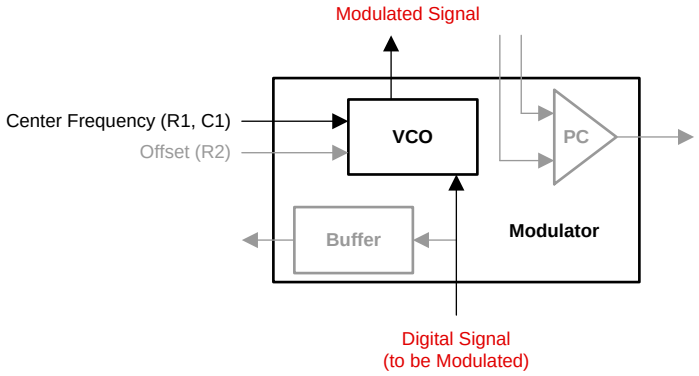
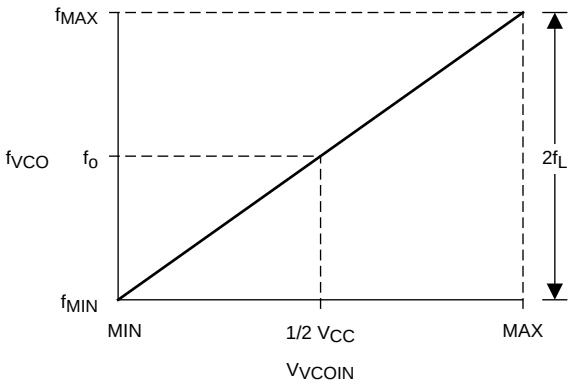


Figure 2. Basic Block Diagram of a PLL as a Modulator

To design a modulator with maximum and minimum frequency of f_{MAX} and f_{MIN} respectively, the following steps are required:

1. Given f_{MAX} and f_{MIN}, center frequency f_O can be estimated as (f_{MAX} – f_{MIN}) / 2, see Figure 3.



$2f_L$ = Frequency Lock Range, f_o= Center Frequency

Figure 3. Frequency Characteristics of VCO Operating without Offset

2. Determine the values of R1 and C1 using figures 11–15 in the device datasheet (SCHS204). Note that the values of these components must satisfy following conditions:

   (a) 3 kΩ < R1 < 300 kΩ

   (b) C1 > 40 pF

   (c) (R1 || R2) > 2.7 kΩ

   Use of R2 to set the offset frequency is optional and can be left open, if not needed.

3. Figure 16–21 of the device datasheet (SCHS204) gives an estimate of separation between frequencies for the given VCO_{IN} voltage.
   1.0 V < VCO_{IN} < 0.9 × V_{CC} is recommended to generate proper oscillation from VCO.

4. An optional LPF (R3-C2, illustrated in Figure 4) is included to minimize noise at the VCO_{IN} pin. The 3-dB cut off frequency of this filter should be 10 times or higher than the maximum bit rate of the modulating signal.

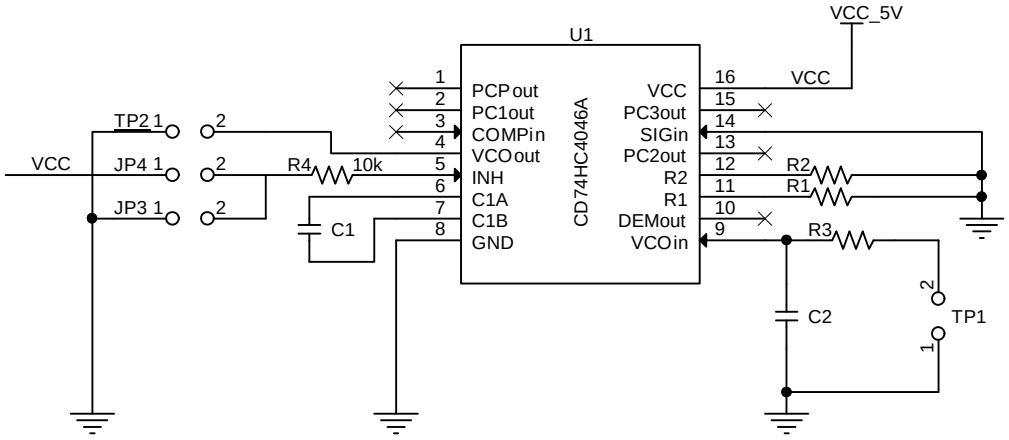


Figure 4. Typical Modulator Schematic

Example:

A test circuit (V_{CC} = 5 V) was implemented to modulate a digital signal with the following component values:

R1 = 3 kΩ, C1 = 47 pF, R2 = open, R3 = 0 Ω, C2 = open

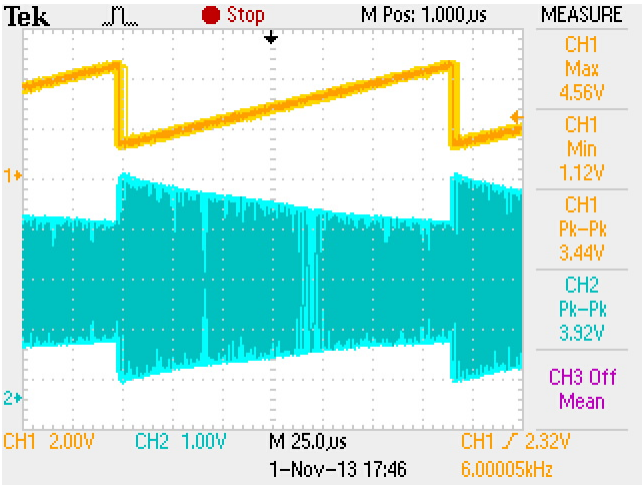
Table 1. Modulator Test Circuit Results

	VCO_{IN} (V)	Frequency of VCO_{OUT} (Hz)	VCO_{OUT} peak to peak (V)
1.	1.0	8.22 M	4.6
2.	2.5	17.24 M	3.1
3.	4.5	27.93 M	2.2

Therefore, by choosing logic 0 as 1 V and logic 1 as 4.5 V, a frequency separation of 19.7 MHz can be obtained.

In a practical circuit, frequency separation depends upon the bandwidth availability of the transmission media. Therefore, by choosing an appropriate offset frequency and voltage level of the VCO_{IN} signal, expected modulation can be achieved.

With an increase in VCO_{IN} (CH1) voltage, the frequency of oscillation increases and VCO_{OUT} peak-to-peak voltage (CH2) decreases as shown in Waveform 1.



Waveform 1. VCO_{IN} (CH1) Voltage and VCO_{OUT} Peak-to-Peak (CH2) Variation

3 Implementation of Demodulator

The demodulator operates in closed-loop mode with the PC and an external LPF, as shown in Figure 5.

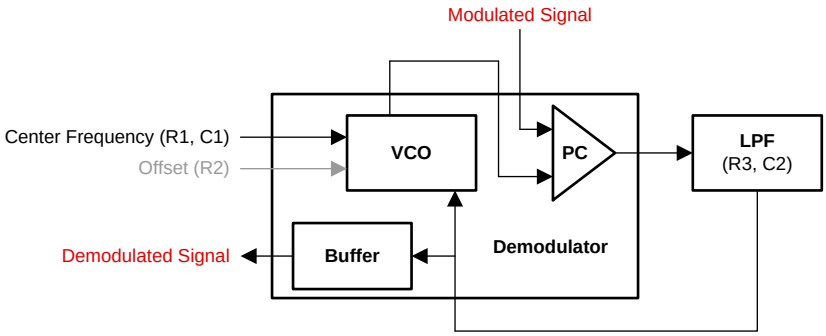


Figure 5. Basic Block Diagram of PLL as Demodulator

To design a demodulator with maximum and minimum frequency of f_{MAX} and f_{MIN}, respectively (which is same as that of modulator), the following steps are required:

1. Use the same value of R1 and C1 as that of modulator.
2. While using PC1, the capture range depends on the LPF (R3-C2) characteristics and can be made as large as the lock range. For PC2, capture range is equal to lock range and is independent of the LPF.
3. Since leakage current can affect the V_{DEMOUT}, a load resistor (R5) from this pin to GND in the range of 50 kΩ to 300 kΩ is recommended.

A typical demodulator schematic is illustrated in Figure 6.

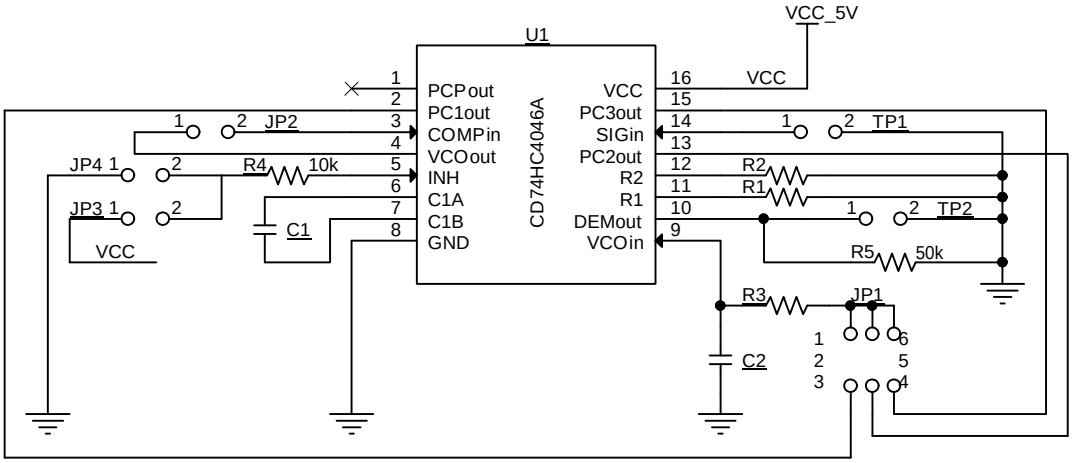


Figure 6. Typical Demodulator Schematic

Example:

A test circuit (V_{CC} = 5 V) was implemented to demodulate a digital signal using PC2 with following component values:

R1 = 3 kΩ, C1 = 47 pF, R2 = open, R3 = 36 kΩ, C2 = 120 pF

Table 2. Demodulator Test Circuit Results

	VCO_{IN} (V) at Modulator	Frequency of SIG_{IN} (Hz) at Demodulator	SIG_{IN} peak to peak (V) at demodulator	DEM_{OUT} (V) at modulator
1.	1.0	8.22M	4.6	1.28
2.	2.5	17.24M	3.1	2.5
3.	4.5	27.93M	2.2	3.76

Therefore, by choosing 3.5 Vp-p VCO_{IN} and frequency separation of 19.7 MHz at modulator, DEM_{OUT} of (3.76 – 1.28) = 2.48 Vp-p can be obtained.

4 Test Circuit Waveforms

The waveforms in Table 3 show variations in the following when VCO_{IN} voltage is changed:

(a) VCO_{OUT} frequency

(b) Peak-to-peak voltage of modulator VCO_{OUT} or SIG_{IN} of demodulator

(c) Corresponding DEM_{OUT} voltage

The waveforms in Table 4 show VCO_{IN} (level-shifted digital modulating signal), VCO_{OUT} (modulated signal) and corresponding DEM_{OUT} (demodulated signal) at different frequencies of digital signal.

Table 3. Variation in VCO_{OUT} Frequency, Peak-to-Peak Voltage and DEM_{OUT}

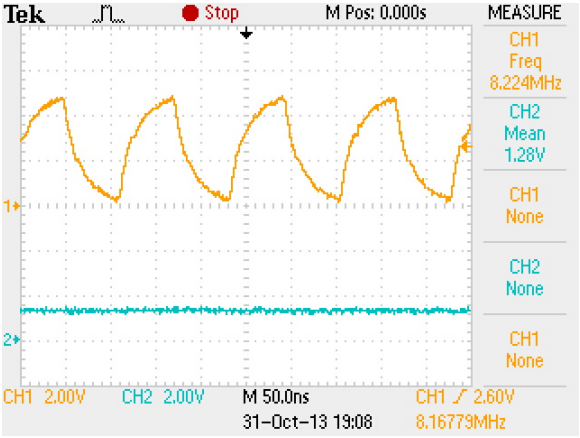
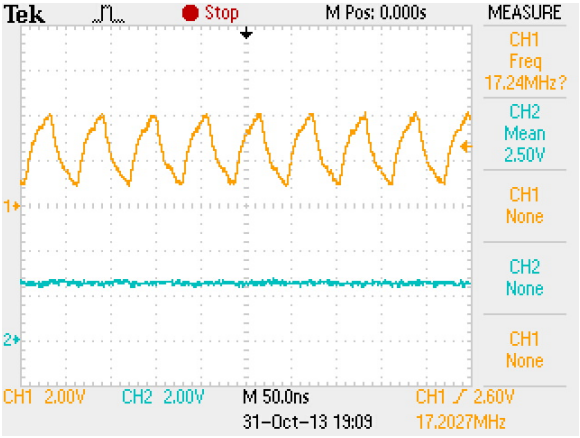
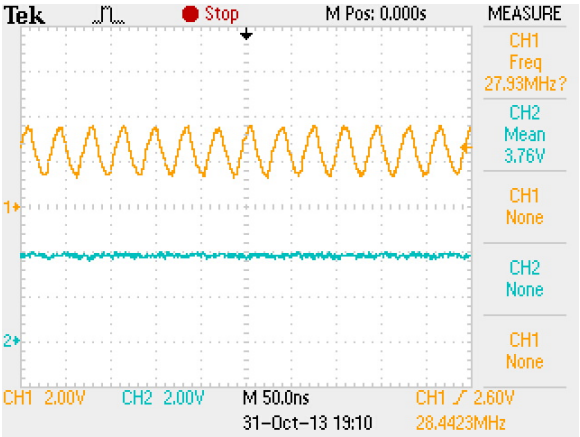
	Condition at Modulator	Demodulator Waveforms: CH1: SIG_{IN} and CH2: DEM_{OUT}
1.	VCO_{IN} = 1 V	 **Waveform 2**
2.	VCO_{IN} = 2.5 V	 **Waveform 3**
3.	VCO_{IN} = 4.5 V	 **Waveform 4**

Table 4. VCO_{IN} (Modulating), VCO_{OUT} (Modulated) and DEM_{OUT} (Demodulated)

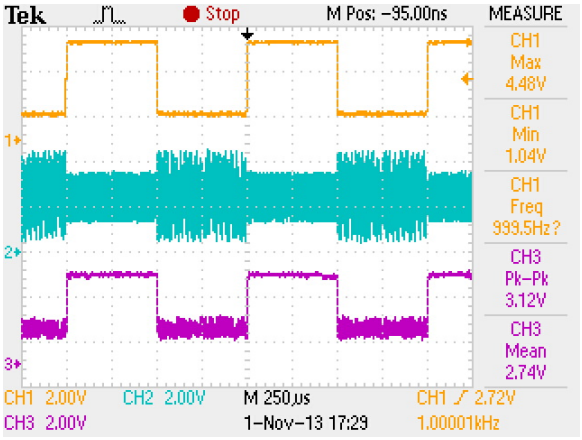
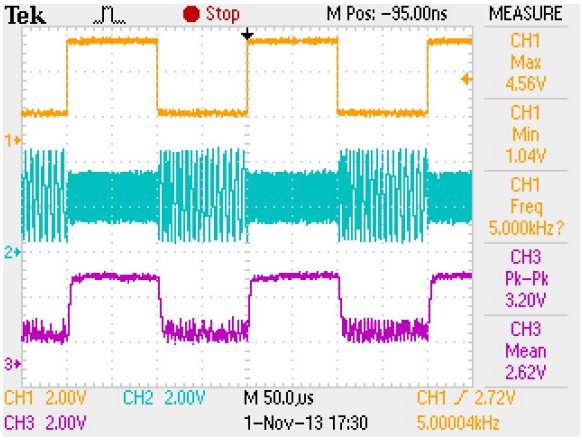
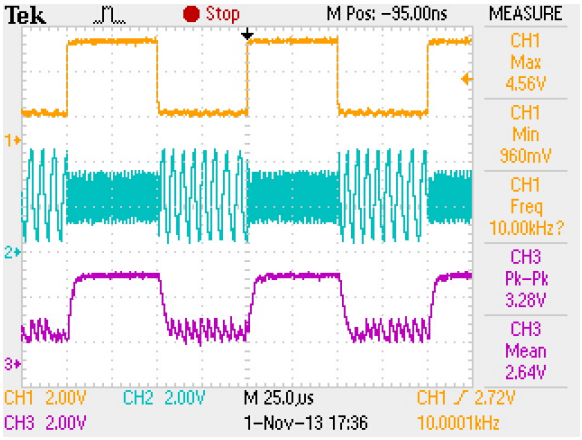
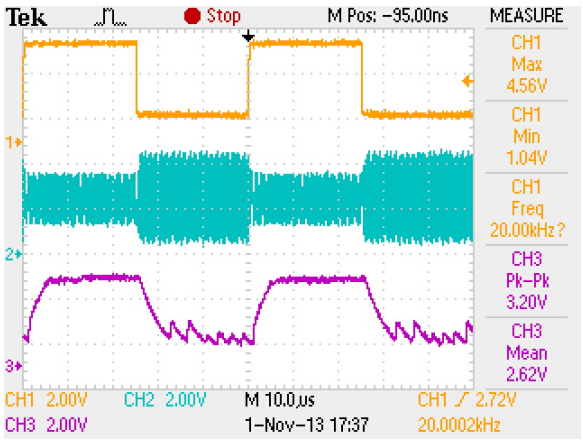
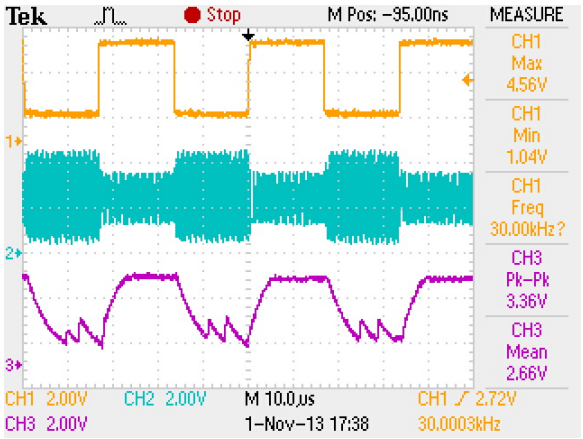
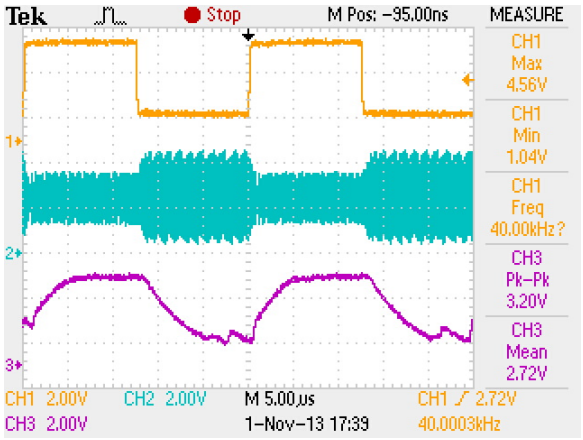
	VCO_{IN}	DEM_{OUT}	Waveforms: CH1: VCO_{IN}, CH2: VCO_{OUT}, CH3: DEM_{OUT}
1.	Peak to peak (V)=3.44 V, Frequency = 1 kHz	Peak to peak (V) = 3.12 V, Mean (V) = 2.74 V	 **Waveform 5**
2.	Peak to peak (V) = 3.52 V, Frequency = 5 kHz	Peak to peak (V) = 3.20 V, Mean (V) = 2.62 V	 **Waveform 6**
3.	Peak to peak (V) = 3.60 V, Frequency = 10 kHz	Peak to peak (V) = 3.28 V, Mean (V) = 2.64 V	 **Waveform 7**

Table 4. (continued)

	VCO_{IN}	DEM_{OUT}	Waveforms: CH1: VCO_{IN}, CH2: VCO_{OUT}, CH3: DEM_{OUT}
4.	Peak to peak (V) = 3.60 V, Frequency = 20 kHz	Peak to peak (V) = 3.12 V, Mean (V) = 2.69 V	 **Waveform 8**
5.	Peak to peak (V) = 3.52 V, Frequency = 30 kHz	Peak to peak (V) = 3.04 V, Mean (V) = 2.72 V	 **Waveform 9**
6.	Peak to peak (V) = 3.52 V, Frequency = 40 kHz	Peak to peak (V) = 2.88 V, Mean (V) = 2.71 V	 **Waveform 10**

It can be concluded from Waveforms 5 through 9, that it is difficult to use the DEM_{OUT} signal as it is, at higher frequency of modulating signal. Hence, a Schmitt trigger can be used with appropriate threshold and hysteresis to get a clean demodulated signal with sharp rising and falling edges.

5 Schemes To Realize Modulator – Demodulator Pair

This section briefly describes various FSK modulation-demodulation schemes. It is important to consider the limitations of each technique before using it for a specific application. In each case, frequency used to represent digital data after FSK modulation should be hundred folds or higher than that of digital data rate to ensure correct bit duration for each bit after demodulation.

5.1 Scheme 1

In this scheme, VCO at the modulator transmits a particular frequency during occurrences of bit 1 in the digital data and remains idle during occurrence of bit 0. At the demodulator end, the presence or absence of the frequency is tracked by the PLL. PC output followed by LPF, represents the demodulated signal, which is the equivalent of the original digital information.

For this scheme, VCO_{IN} < 0.6 V for logic 0 and
VCO_{IN} close to 0.9 × V_{CC} for logic 1 is recommended.

Use of PC2 at the demodulator gives good results over a wide range of frequency.

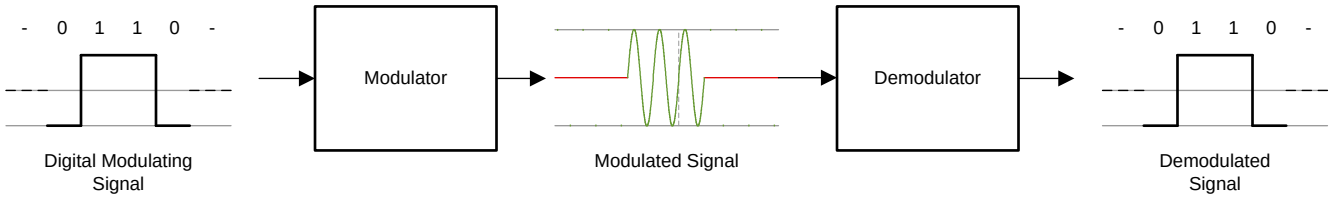


Figure 7. Scheme 1

Advantages:

- Power consumption is less at the modulator.
- A burst of frequency is transmitted only during transmission of a specific data bit (either 1 or 0), hence, there is less noise created in the transmission media.
- Single frequency is used; therefore, the bandwidth requirement is smaller.
- Gives better performance even at higher frequencies (200 kbps or higher) of modulating signal (as compared to scheme 2), because of wide separation possible between logic 0 and logic 1 voltages.

Limitations:

- It is difficult to determine if the remote modulator is defunct (versus continuously sending 0's).
- When VCO_{IN} < 0.6 V (logic 0), modulator output may either be 0 V or V_{CC}; however, this does not affect demodulation.

5.2 Scheme 2

In this scheme, VCO at the modulator transmits one particular frequency during occurrences of bit 1 in the digital data and other frequency during occurrence of bit 0. At the demodulator end, the change in the frequency is tracked by the PLL. PC output followed by LPF represents the demodulated signal, which is the equivalent of the original digital information.

For this scheme, 1.0 V < VCO_{IN} < 0.9 V_{CC} is required.

Use of PC2 at the demodulator gives good results over a wide range of frequency.

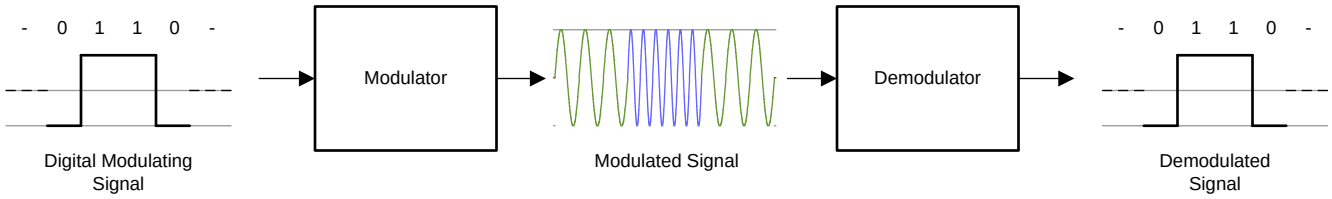


Figure 8. Scheme 2

Level shifting of the input digital signal is required to meet the VCO_{IN} input range which can be achieved using a level-shifter circuit.

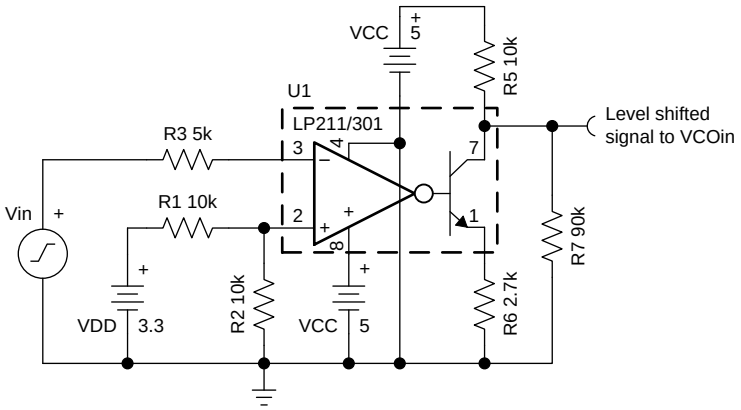


Figure 9. Level-Shifter Circuit using LP211

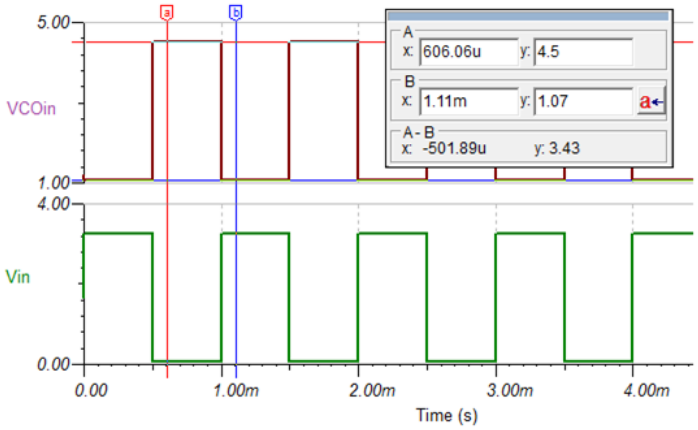


Figure 10. Simulated Waveforms of Level-Shifter Circuit using LP211

As can be seen from the test waveform in Figure 10, a digital signal Vin (0 V–3.3 V) is converted to VCO_{IN} (1.07 V–4.5 V).

Advantages:

- It is easy to determine if the remote modulator is defunct.

Limitations:

- Power consumption is more at the modulator due to continuous oscillations.
- Requires more bandwidth
- As VCO_{IN} logic 0 and logic1 voltage level separation decreases, noise on the demodulated output appears to increase.

6 Conclusion

This application report described logic-level implementation of BFSK modulator and demodulator using HC/HCT4046A devices.

However, while implementing this circuit for a real-time application, the following important factors must be considered for a reliable communication link:

- Output impedance of the modulator
- Characteristic impedance of the transmission media
- Frequency response of transmission media
- Input impedance of the demodulator

Hence, impedance matching and signal conditioning becomes an important aspect in a practical system.

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