Functional Safety Information

LM2904B-Q1

Functional Safety FIT Rate, FMD and Pin FMA

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1 Functional Safety FIT Rate, FMD and Pin FMA

1.1 Overview

This document contains information for LM2904B-Q1 to aid in a functional safety system design. Information provided are:

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- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

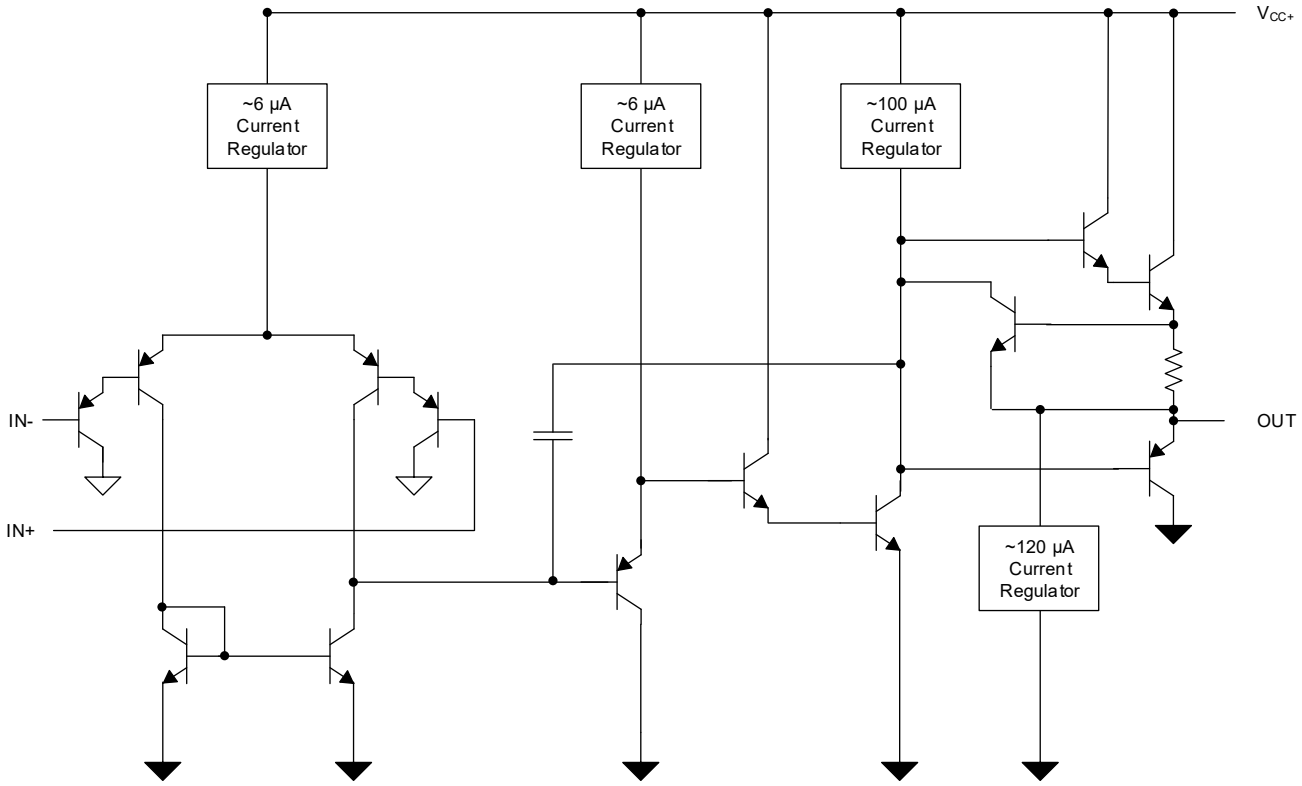

Figure 1-1. Functional Block Diagram

LM2904B-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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1.2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the LM2904B-Q1 based on two different industry-wide used reliability standards:

- Table 1-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 1-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
Package	TSSOP-8	SOIC-8	VSSOP-8
Total Component FIT Rate	9	10	7
Die FIT Rate	3	3	3
Package FIT Rate	6	7	4

The failure rate and mission profile information in Table 1-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 1-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar Operational Amplifier	6FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 1-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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1.3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM2904B-Q1 in Table 1-3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 1-3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification	30%

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1.4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM2904B-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 1-5)
- Pin open-circuited (see Table 1-6)
- Pin short-circuited to an adjacent pin (see Table 1-7)
- Pin short-circuited to supply (see Table 1-8)

Table 1-5 through Table 1-8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 1-4.

Table 1-4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Single-supply operation is used. For example, V+ = 15V and V- = 0V

1.4.1 LM2904B-Q1 Pin FMA

Figure 1-2 shows the pin diagram for the LM2904B-Q1. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the data sheet.

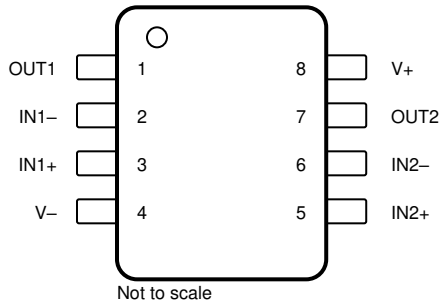

Figure 1-2. Pin Diagram

Table 1-5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat	B
IN1-	2	Channel 1 output high, if other input is greater than zero volts	C
IN1+	3	Channel 1 output low, if other input is greater than zero volts	C
V-	4	Normal operation, unless dual supply voltage was intended	D
IN2+	5	Channel 2 output low, if other input is greater than zero volts	C
IN2-	6	Channel 2 output high, if other input is greater than zero volts	C
OUT2	7	May cause device to overheat	B
V+	8	No power; inputs block positive current flow	C

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Table 1-6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can't be used by application	C
IN1-	2	Channel 1 output low, if other input is within valid common mode voltage range	C
IN1+	3	Channel 1 output high, if other input is within valid common mode voltage range	C
V-	4	Lowest voltage pin will try to power the device's V- pin	B
IN2+	5	Channel 2 output high, if other input is within valid common mode voltage range	C
IN2-	6	Channel 2 output low, if other input is within valid common mode voltage range	C
OUT2	7	Output can't be used by application	C
V+	8	Highest voltage output pin will try to power internal V+ via internal diode(s)	B

Table 1-7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Channel 1 configured in unity gain	C
IN1-	2	IN1+	No input VID, so Channel 1 is undefined	C
IN1+	3	V-	Channel 1 output low, if other input is greater than zero volts	C
V-	4	IN2+	Channel 2 output low, if other input is greater than zero volts. Pins are not adjacent to each other	C
IN2+	5	IN2-	No input VID, so Channel 2 output is undefined	C
IN2-	6	OUT2	Channel 2 configured in unity gain	C
OUT2	7	V+	May cause overheating of immediate damage for V+ > 15V	A
V+	8	OUT1	May cause overheating of immediate damage for V+ > 15V. Pins are not adjacent to each other	A

Table 1-8. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating or immediate damage for V+ > 15V	A
IN1-	2	Channel 1 output low, if other input is within valid common mode voltage range	C
IN1+	3	Channel 1 output high, if other input is within valid common mode voltage range	C
V-	4	No power, power source is shorted	C
IN2+	5	Channel 2 output high, if other input is within valid common mode voltage range	C
IN2-	6	Channel 2 output low, if other input is within valid common mode voltage range	C
OUT2	7	May cause overheating or immediate damage for V+ > 15V	A
V+	8	No effect. Normal operation.	D

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (February 2021)	Page
• Added VSSOP (DGK) information	3

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