APPLICATION NOTE

PRACTICAL CONSIDERATIONS IN HIGH PERFORMANCE MOSFET, IGBT and MCT GATE DRIVE CIRCUITS

BILL ANDREYCAK

INTRODUCTION

The switchmode power supply industry's trend towards higher conversion frequencies is justified by the dramatic improvement in obtaining higher power densities. And as these frequencies are pushed towards and beyond one megahertz, the Mosfet transition periods can become a significant portion of the total switching period. Losses associated with the overlap of switch voltage and current not only degrade the overall power supply efficiency, but warrant consideration from both a thermal and packaging standpoint. A/though brief, each of the Mosfet switching transitions can be further reduced if driven from from a high speed, high current totem-pole driver - one designed exclusively for this application. This paper will highlight three such devices; the UC1708 and UC1710 high current Mosfet driver ICs, and the UC1711 high speed driver. Other Mosfet driver ICs and typical application circuits are featured in UNITRODE Application Note U-118.

EFFECTIVE GATE CAPACITANCE

The Mosfet input capacitance (Ciss) is frequently misused as the load represented by a power mosfet to the gate driver IC. In reality, the effective input capacitance of a Mosfet (Ceff) is much higher, and must be derived from the manufacturers' published total gate charge (Qg) information. Even the specified maximum values of the gate charge parameter do not accurately reflect the driver's instantaneous loads during a given switching transition. Fortunately, FET manufacturers provide a curve for the gate-to-source voltage (Vgs) versus total gate charge in their datasheets. This will be segmented into four time intervals of interest per switching transition. Each of these will be analyzed to determine the effective gate capacitance and driver requirements for optimal performance.

Inadequate gate drive is generally the result of underestimating the effective load of a power mosfet to its driver.

TOTAL GATE CHARGE (Qg)

First, a typical high power Mosfet "Gate Charge versus Gate-to-Source Voltage" curve will be examined. An IRFP460 device has been selected and this curve is applicable to most other Fet devices by adjusting the gate charge numbers accordingly. Both turn-on and turn-off trasnsitions are shown with the respective drain currents and drain-to-source voltages.

TURN-ON WAVEFORMS

Gate voltage vs time

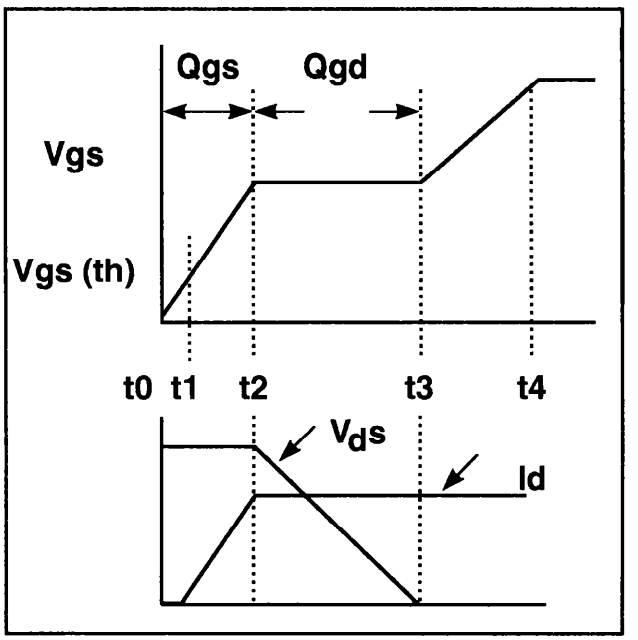


Figure 1.

INTERVAL t0-t1

The time required to bring the gate voltage from zero to its threshold Vgs(th) can be expressed as a delay time. Both the voltage across the switching device and current through it are uneffected during this interval.

INTERVAL t1-t2

This period starts at time t1 when the gate voltage has reached Vgs(th) and drain current begins to flow. Current continues to rise until essentially reaching its final value at time t2. While this occurred, the gate to source voltage had also been increasing. The drain-to-source voltage remains unchanged at Vds(off). Power in the Mosfet is wasted by the simultaneous overlap of voltage and current.

INTERVAL t2-t3

Beginning at time t2 the drain-to-source voltage starts to fall which introduces the "Miller" capacitance effects (Cgd) from the drain to the Mosfet gate. The result is the noticeable plateau in the gate voltage waveform from time t2 until t3 while a charge equal to Qgd is admitted. It is here that most drive circuits are taxed to their limits. The interval concludes at time t3 when the drain voltage approaches its minimum.

INTERVAL t3-t4

During this final interval of interest the gate voltage rises from the plateau of the prior region up to its final drive voltage. This increasing gate voltage decreases Rds(on), the Mosfet drain-to-source resistance. Bringing the gate voltage above 10 to 12 volts, however, has little effect on further reducing Rds(on).

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
to-t1	0-threshold	0	Vds(off)	Slew rate (dv/dt)
t1-t2	thrs-plateau	rising	Vds(off)	Slew rate (dv/dt)
t2-t3	V(plateau)	Ion(dc)	falling	Peak current I(max)
t3-t4	rising	Ion(dc)	Ion*Rds(t)	Peak I & dv/dt

TURN-OFF WAVEFORMS
Gate voltage vs. time

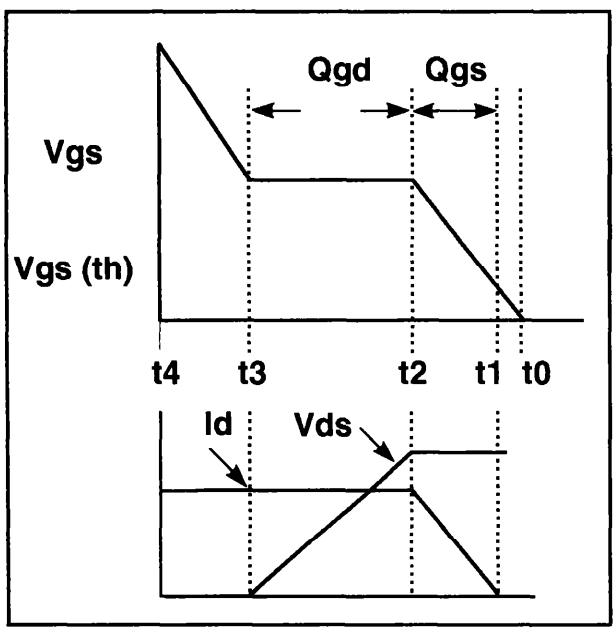


Figure 2

The intervals during turn-off are basically the same as those described for turn-on, however the sequence and corresponding waveforms are reversed.

INTERVAL t4-t3

The beginning of the turn-off cycle can be described as a delay from the final drive voltage (Vgs(on)) the the plateau region. Both the drain voltage and current waveforms remain unchanged while the devices effective resistance (Rds(on)) increases as the gate voltage decreases.

INTERVAL t3-t2

Once the plateau is reached at time t3, the gate voltage remains constant until time t2. Gate charge due to the Miller effect is being removed, an amount equal to Qgd. The drain voltage rises to its off state amplitude, Vds(off), while the drain current continues to flow and equals I(on). This lossy transition ends at time t2.

INTERVAL t2-t1

Once the Miller charge is completely removed, the gate voltage is reduced from the plateau to the threshold voltage causing the drain current to fall from I(on) to zero. Transition power loss ends at time t1 when the gate threshold is crossed.

INTERVAL t1 -t0

This brief period is of little interest in the turn-off sequence since the device is off at time t1.

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t4-t3	falling	Ion(dc)	Ion* Rds(t)	Peak I and dv/dt
t3-t2	V(plateau)	Ion(dc)	falling	Peak Current I (max)
t2-t1	Vplat-thrsh	falling	Vds(off)	Slew rate (dv/dt)
t1-t0	thrsh-0	0	Vds(off)	Slew rate (dv/dt)

FET Transition Power Loss

During each of the FET turn-on and turn-off sequences power is lost due to the switching device's simultaneous overlap of drain - source voltage and drain current. Since both the FET voltage and current are externally controlled by the application, the driver IC can only reduce the power losses by making the transition times as brief as possible. Minimization of these losses simply requires a competent driver IC, one able to provide high peak currents with high voltage slew rates.

A review of the prior transition waveforms indicates that power is lost between the times of t1 and t3. While t2 serves as the pivot point for which waveform is rising or falling, as the equations show its irrelavent in the power loss equation. For the purpose of brevity, the waveform of interest can be approximated as a triangle while the other waveform is constant. The duration between times t1 and t3 can now be defined as the net transition time, t(tran), with a conversion period of t(period)

During the two intervals from t1 to t3:

$$Ploss = \frac{0.5 * I(on) * Vds(off) * t(2\text{-}1)}{t(period)}$$

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(3\text{-}2)}{t(period)}$$

Combining the two equations with t(tran) = t3-1 results in a net loss of:

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(trans)}{t(period)}$$

Since these loses are incurred twice percycle, first at turn-on and then again at turn-off, the net result is a doubling of the power loss.

Ploss = Vds(off)*I(on)*t(trans)/t(period)

This relationship displays the need for fast transitions at any switching frequency, and is of significant concern at one megaHertz. Minimization of the FET transition power loss can be achieved with high current drivers.

GATE CHARGE

Each division of the transition interval has an associated gate charge which can be derived from the FET manufacturers datasheets. Since there are three basic shapes to the Vgs curve, the interval from t0 to t1 can be lumped together with that of the t1 to t2 period. For most large FET geometries, the amount of charge in the t0 to - t1 span is negligible anyway. This simplification allows an easy calculation of the effective gate capacitance for each interval along with quantifying the peak current required to traverse in a given amount of time.

Charge can be represented as the product of capacitance multiplied by voltage, or current multiplied by time. The effective gate capacitance is determined by dividing the required gate charge (Qg) by the gate voltage during a given interval. Likewise, the current necessary to force a transition within a specified time is obtained by dividing the gate charge by the desired time.

Cgs (effective) = delta Qg / delta Vgs

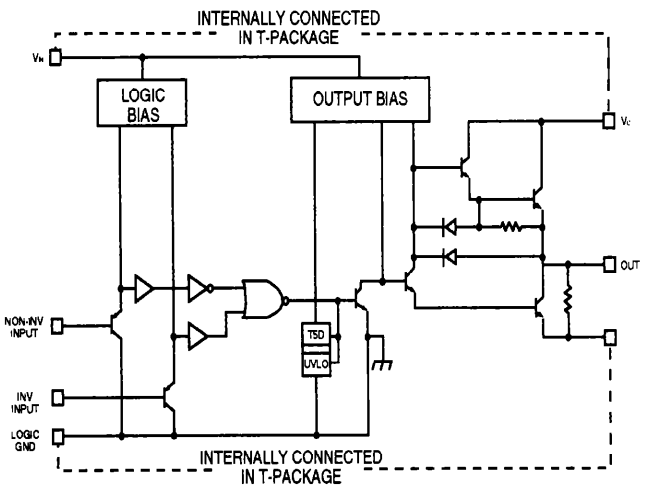
Ig(required) = delta Qg / t(transition)

UC1710
The "MILLER KILLER"

High peak gate drive currents are desirable in paralleled FET applications, typical of a high power switching section or power factor correction stage. Dubbed as "the Miller Killer", the UC1710 boasts a guaranteed 6 amp peak output current. This hefty driver current minimizes the FET parasitic "Miller" effects which would otherwise result in poor transi-

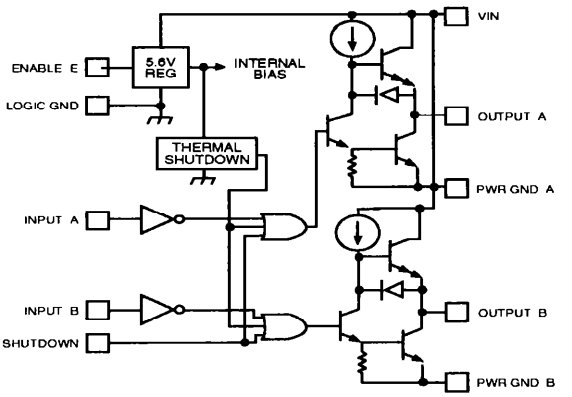
tion performance. Higher currents are possible with this driver, however the limiting factor soon becomes the parasitic series inductance of the FET package (15 nH) and the layout interconnection of 20 nH/inch. An RF type arrangement of the PC board layout is an absolute **MUST** to realize this device's full potential.

UC 1710 BLOCK DIAGRAM



The UC1710 has "no-load" rise and fall times of 20 nanoseconds (or less) which do not change significantly with any loads under 3 nanoFarads. It's also specified into a load capacitance of 30 nanoFarads, roughly equivalent to what is represented by three paralleled "size 6" FET devices. Propagation delays are brief with typical values specified at 35 nanoseconds from either input to a ten percent change in output voltage.

UC 1708 BLOCK DIAGRAM



The UC1708 is a unique blend of the high speed attributes of the UC1711 along with the higher peak current capability of the UC1710. This dual noninverting driver accepts positive TTL/CMOS logic from control circuits and provides 3 amp peak outputs from each totem pole.

Propagation delays are under 25 nanoseconds while rise and fall times typically run 35 nanoseconds into 2.2 nanoFarads. The output stage design is a "no float" version which incorporates a self biasing technique to hold the outputs low during undervoltage lockout, even with Vin removed.

In the 16 pin DIL package, the device features a remote ENABLE and SHUTDOWN function in addition to seperate signal and power grounds. The ENABLE function places the device in a low current standby mode and the SHUTDOWN circuitry is high speed logic directly to the outputs.

UC1708 / 1710 / 1711 PERFORMANCE COMPARISON
TABLE 1.

PARAMETER	LOAD	UC1708	UC1710	UC1711
Propagation Delay	0	25	30	10
t(plh)	1.0 nF	25		15
input to 10% output	2.2 nF	25	30	20
	30 nF		30	
Raise time	0	25	20	12
t(tlh)	1.0 nF	30		25
10% to 90% rise	2.2 nF	40	25	40
	30 nF		85	
Propagation Delay	0	25	30	3
t(phl)	1.0 nF	25		5
input to 90% output	2.2 nF	25	30	
	30 nF		30	
Fall Time	0	25	15	7
t(thl)	1.0 nF	30		25
90% to 10% fall	2.2 nF	40	20	40
	30 nF		85	

TRANSITION PERFORMANCE

Using the table above, the driver output slew rates and average current delivered can be calculated. The figures can be compared to lower power op-amps or comparators to gain a perspective on the relative speed of these high performance drivers.

The UC1708 delivers output slew rates (dv/dt) in the order of 300 to 480 volts per microsecond, at average load currents of under one amp, depending on the load. The high speed UC1711 exhibits similar characteristics under loaded conditions, but can achieve a no load slew rate of over 1700 volts per microsecond - nearly 2 volts per nanosecond.

For higher power applications, the UC1710 “Miller Killer” will produce an average current of 4.5 amps AT slew rates of 150 volts per microsecond. With lighter loads it will deliver an average current of 1.5 amps at a slew rate of approximately 500 volts per microsecond. In most applications, the UC1710 will easily outperform “homebrew” discrete mosfet transistor totem pole drive techniques.

Each device in this new generation of MOSFET drivers is significantly more responsive than the earlier counterparts for a given application - whether it’s higher speed (UC1711), higher peak current (UC1710) or a combination of both (UC1708).

DRIVER CONSIDERATIONS

As previously demonstrated, the ideal MOSFET gate drive IC is a unique blend of both high speed switching and high peak current capability. Initially, the high speed is required to bring the gate voltage from zero to the plateau, but the current is low. Once the plateau is intersected, the driver voltage is fairly constant, and the IC must switch modes. Instantly, the driver current snaps to its maximum as charge is injected to overcome the FET’s Miller effects. Finally, a combination of both high slew rate and high current is needed to complete the gate drive cycle.

At turn-off this sequence is reversed, first demanding both high slew rate and high current simultaneously. This is followed by the plateau region which is limited only by the maximum driver current. Finally, there is high speed discharge of the gate to zero volts.

Optimization of a driver for this type of application can be difficult. In general, the MOSFET driver IC output stage is designed to switch as fast as the manufacturer’s process will allow.

CROSS CONDUCTION

There are numerous tradeoffs involved in the design of these drivers beyond the obvious choices of number of outputs and peak current capability. Cross-conduction is defined as the conduction of current through both of the totem pole transistors simultaneously from Vin to ground. It is an unproductive loss in the output stage which results in unnecessary heating of the driver and wasted power. Cross conduction is the result of turning one transistor ON before the opposing one is fully off, a compromise often necessary to minimize the input to output propagation delays.

An interesting observation is that cross-conduction is less of a concern with large capacitive loads (FETs) than with unloaded or lightly loaded driver outputs. Any capacitive load will reduce the slew of the output stage, slowing down its dv/dt. This causes a portion of the cross conduction current to flow from the load, rather than from the input supply through the driver’s opposite output transistor. The power loss associated with a drivers inherent cross-conduction is unchanged with large capacitive loads, however it is not caused by a “shoot-through” of supply current.

DRIVER PERFORMANCE

There are a variety of applications for MOSFET drivers - each with its own unique set of speed and peak current requirements. Most general purpose drivers feature 1.5 amp peak totem-pole outputs which deliver rise and fall times of approximately 40 nanoseconds into 1 nanoFarad. Propagation delays are in the neighborhood of 40 to 50 nanoseconds, making these devices quite adaptable to numerous power supply and motor control applications. These specifications can be used for a comparison to those of a new series of higher speed and higher current devices, specifically, the UC1708, UC1710 and the UC1711 power MOSFET drivers. Each member in this group of “third” generation driver ICs features significant performance improvements over their predecessors with one parameter optimized for a specific set of applications.

MOSFET DRIVER IC FEATURE AND PERFORMANCE OVERVIEW
TABLE 2.

Feature	UC1708	UC1770	UC1711
Number of outputs	2	1	2
Peak output current (per output)	3A	6A	I.5 A
Noninverting input-output logic	YES	YES	
Inverting input-output logic		YES	YES
Maximum supply voltage Vcc	35v	20V	40V
Typical supply current Icc (1.)	16ma	30ma	17ma
Remote Enable	YES		
Shutdown Input	YES	YES (2)	
Seperate grounds, signal and power	YES (3)	YES (3)	
Seperate Vin and Vc pins		YES (3)	
8 pin DIL package	YES	YES	YES
16 pin DIL package	YES	YES	YES
5 pin TO-220 package		YES	

Note 1. Typical Vc plus Vcc current measured at 200KHZ, 50% duty cycle and no load
Note 2. Using the device's other input
Note 3. Package dependent

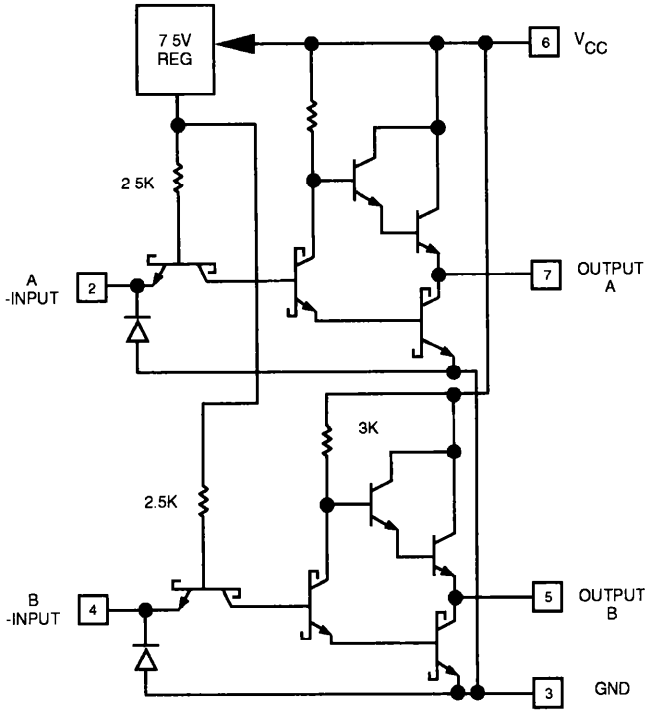
PROPAGATION DELAYS

The power supply industry's trend towards higher power densities has thrust switching frequencies well beyond one megaHertz in many low to medium power systems. With a one microsecond total conversion period, or less, the FET switching transitions should be in the order of low tens of nanoseconds to yield high efficiency. Additionally, the propagation delays from the driver input to output should be around ten nanoseconds for quick response.

UC1711

The UC1711 device features typical propagation delays of three and ten nanoseconds at no load, depending on the transition. Coupled with dual 1.5 amp peak totem-pole outputs, this device is optimized for high frequency FET drive applications. Its all NPN Schottky transistor construction is not only fast, but radiation tolerant as well.

UC1711 BLOCK DIAGRAM



GATE DRIVE POWER CONSIDERATIONS

Perhaps the most popular misconception in the power supply industry is that a FET gates require NO power from the auxiliary supply - that both turn-on and turn-off are miraculously power free. Another fallacy is that the driver consumes all the measured supply current, Icc, and none of it is used to transition the gates. Obviously, both of these statements are false.

In reality, the power required by the gate itself can be quite substantial in high frequency applications. Calculation of this begins by listing the specified total gate charge for the FET device, Qg.

The gate power utilized in charging and discharging a capacitor at frequency "F" is:

P(cap) = C * V^2 * F

Substituting the gate charge for capacitance multiplied by voltage (Q=C*V) in this equation results in:

P(gate) = Qg * V * F

The gate power required verses FET size and switching frequencies is tabulated for some common applications in Table 3. Table 4. transforms this power into driver input current at a nominal 12 volt bias.

GATE POWER (mW) VS. SWITCHING FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	10	18	28	36	46	90	136	180
SIZE 2	16	30	46	60	76	153	226	300
SIZE 3	28	54	82	108	136	275	406	504
SIZE 4	48	96	144	192	240	480	720	960
SIZE 5	100	200	300	400	550	1W	1.5W	2W
SIZE 6	144	288	432	576	720	1.4W	2W	>2w

Table 3.

DC SUPPLY CURRENT (mA) VS. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1 MEG
SIZE 1	1	1	2	4	5	6	10	12
SIZE 2	1	2	4	5	6	10	16	20
SIZE 3	2	4	6	8	10	16	26	36
SIZE 4	4	8	10	12	16	32	48	64
SIZE 5	8	14	20	26	32	66	100	130
SIZE 6	10	20	28	38	48	96	144	190

Table 4.

The driver output stage can be modelled as a resistance to the respective auxiliary supply rail driving an ideal FET capacitor. All of the power used to charge and discharge the MOSFET gate capacitor is completely transferred into heat by the driver. This gate power loss adds to the driver's own power loss - resulting in a net driver power dissipation equal to it's input voltage, Vcc, multiplied by the sum of the gate and driver currents, lg + Icc. This can be calculated or determined empirically by measuring the driver DC input voltage and current.

THERMAL CONSIDERATIONS

Proper IC package selection and/or device heatsinking is the only method available to insure a safe operating junction temperature, tj. All IC's are specified and graded for various junction temperature ranges, and priced accordingly. As a precaution, it should be noted that using a device outside its tested temperature range can result in poor performance, parameters which run outside their specifications, and quite possibly - no operation at all.

JUNCTION TEMPERATURE

The junction temperature of the driver IC is obtained by first calculating the device's thermal rise above the ambient temperature. This is obtained by multiplying the average input power (Vin*lin) by the device's thermal impedance to air, theta JA (Oja). This term is then added to the ambient temperature to yield the resulting junction temperature, Tj.

If the driver is thermally attached to a heatsink or "cold plate", then the thermal impedance from the device junction to it's package case, theta JC (Ojc), is used to determine the thermal rise. Likewise, this thermal rise is added to the heatsink temperature to determine the junction temperature. In either case, the maximum junction temperature (tj(max)) should be determined and checked against the device's absolute maximum specification.

Average supply currents for each of the three drivers of interest varies primarily with the switching frequency. Rather than listing each driver independently, an rough approximation of 25 milliamps will be used as the driver current, regardless of the specific device utilized and switching frequency. In addition, a typical supply voltage of 12 volts results in a power dissipation by the driver itself of 300 milliwatts.

The calculated gate power of Table 5. has been added to the estimated 300mW of device power to formulate Table 6. - the driver total power dissipation. This is of particular interest in selecting a driver package (8 pin, TO-220, etc.) and heat sink determination for a specific maximum junction temperature, or rise. Typical junction temperature rises vs. frequency and FET size for a IC package, and recommendations are shown in table 7.

AVERAGE POWER DISSIPATION (mW) VS. FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	310	318	328	336	346	390	436	480
SIZE 2	316	330	346	360	376	452	526	600
SIZE 3	328	354	382	408	436	570	706	840
SIZE 4	348	396	444	492	540	780	1.0W	1.3w
SIZE 5	400	500	600	700	800	900	1.7W	2.4W
SIZE 6	444	588	732	876	1.OW	1.7W	2.5W	3.1w

Table 5.

PACKAGE RECOMMENDATIONS

For P(diss) = or < 500mW
A: 8 pin DIL, <40 C rise
B: 8 pin DIL, <45 C rise
C: 8 pin DIL, <50 C rise

For P(diss) = or > 500mW (using heatsink)
D: 8 pin DIL, <40 C rise
E: 8 pin DIL, <50 C rise

For P(diss) > 500mW
F: TO-220 recommended

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1 MEG
SIZE 1	A	A	B	B	B	C	D	D
SIZE 2	A	B	B	B	C	D	D	D
SIZE 3	B	B	C	D	D	D	E	F
SIZE 4	B	C	D	D	D	F	F	F
SIZE 5	C	D	D	E	F	F	F	F
SIZE 6	D	D	E	F	F	F	F	F

Table 6.

HIGH POWER APPLICATIONS

Most high power applications require the use of "monster" MOSFETs or several large FETs in parallel for each switch. Generally, these are low to medium frequency applications (less than 200kHz) where obtaining a low Rds(on) is of primary concern to minimize the DC switch loss. It is not uncommon to find two, three and even four large devices used in parallel, although some of these combinations are unlikely from a cost versus performance standpoint. Table seven displays the individual FET device characteristics and several popular parallel arrangements. Listed in descending order is Rds(on) at room temperature and the total gate charge required. This will ultimately be used to determine the gate drive current in Table 8., total power dissipation in Table 9., and driver IC recommendation in Table 10 for various applications.

PARALLELED MOSFET CHARACTERISTICS - TABLE 7.

MOSFET ARRANGEMENT	Rds(on) effective	Qg(nC) total	MOSFET ARRANGEMENT	Rds(on) effective	Qg(nC) total
1 X SIZE 4	0.85	63	2 X SIZE 5	0.200	260
1 X SIZE 5	0.40	130	2 X SIZE 6	0.135	380
1X SIZE 6	0.27	190	3 X SIZE 5 (1)	0.133	390
2 X SIZE 4 (1)	0.425	126	4 X SIZE 5 (1)	0.100	520
3XSIZE4(1)	0.283	189	3 X SIZE 6 (2)	0.090	570
4 X SIZE 4 (1)	0.213	252	4 X SIZE 6 (2)	0.068	760

1. Consider another selection 2. Consider a "Monster" FET

AVERAGE SUPPLY CURRENT (mA) VS. FREQUENCY AND FET SELECTION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	31	39	45	51	65	77
2 X SIZE 6	135	35	45	53	63	83	101
3 X SIZE 6	90	39	53	69	73	91	139
4 X SIZE 6	68	45	63	82	101	139	177

*Includes 25mA of driver supply current

Table 8

POWER DISSIPATION (mW) VS. FREQUENCY AND APPLICATION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	372	468	540	612	780	924
2 X SIZE 6	135	420	540	636	756	1.0W	1.2W
3 X SIZE 6	90	468	636	828	876	1.1W	1.7W
4 X SIZE 6	68	540	756	984	1.2W	1.7W	2.1W

* Includes **300mW** of driver dissipation

Table 9.

DRIVER IC AND PACKAGE SELECTION GUIDE

Selection Guide for < 50 C rise

A: 8 pin DIL or 20 pin PLCC
B: 8 pin DIL with heatsink. or TO-220.
C: TO-220 with heatsink

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	A	B	C	C	C	C
2 X SIZE 6	135	B	C	C	C	C	C
3 X SIZE 6	90	B	C	C	C	C	C
4 X SIZE 6	68	C	C	C	C	C	C

Table 10.

UC1710 DRIVER PERFORMANCE

Although capacitive in nature, the FET "Miller" effects and demands on the driver differ significantly than a true capacitor load as previously described.

Table 11. shows the typical response of the UC1710 "Miller Killer" driving a single APT5025BN (size 6) device and paralleled MOSFET combinations for reference.

UC1710 RISE, FALL AND DELAY TIMES VS. LOADS

TEST CONDITIONS		Tp LH	Tt LH	Tp HL	Tt HL	Tp +Tt LH	Tt +TP HL
NO LOAD	VDS	28	12	36	12	40	50
ONE	0	28	26	38	30	54	68
APT5025	350	28	35	40	30	63	70
TWO	0	28	38	40	36	66	76
APT5025	350	28	48	42	38	76	80
THREE	0	28	48	42	48	76	90
APT5025	350	28	60	44	58	88	92

Table 11.

PERFORMANCE COMPARISONS

"HOMEBREW" TOTEM-POLES VS. INTEGRATED CIRCUIT DRIVERS

The prior lack of "off-the-shelf" high current or high speed drivers had prompted many to design their own gate drive circuits. Traditionally, an NPN-PNP emitter follower arrangement had been used in lower frequency applications as shown in Figure 7.

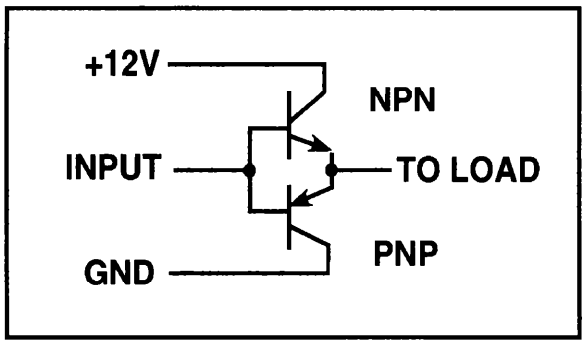


Figure 7

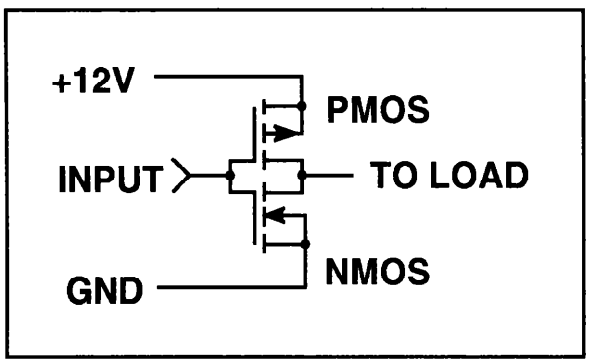


Figure 8

For higher speed applications, a P and N channel FET pair can be used as shown in figure 8. The circuit is configured with the P channel MOS as the upper side switch to simplify the auxiliary bias. Otherwise, a gate drive potential of ten volts above the auxiliary bias would required.

Unfortunately, this configuration has a few drawbacks First, it leads to an inverting logic flow from the driver input to its output, complicating matters especially during power-up and power-down sequences. Without a clever undervoltage lockout circuit the main power switch will tend to be ON as the auxiliary supply voltage is raised or lowered while the PWM is OFF.

Cross conduction of both FETs is unavoidable with this configuration due to the difference between the gate threshold voltages of each device. Both P and N channel devices are cross conducting while their input drive waveform is above Vgs(th) of the N device and below that of the P device. One technique to minimize the cross conduction peak current is to add some resistance between the FETs. While this does minimize the "shoot-through" current, it also limits the peak current available to the load. This somewhat defeats the purpose of using the MOSFETs in the first place to deliver high currents. The resistor serves an additional purpose of damping the gate drive oscillations during the transitions. In a practical application, two resistors can be used in the place of one with the center-tap connecting to the FET gate, or load as shown in figure 9.

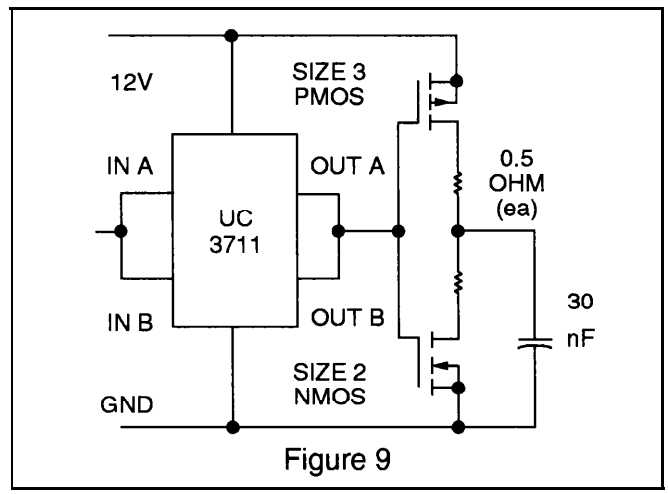
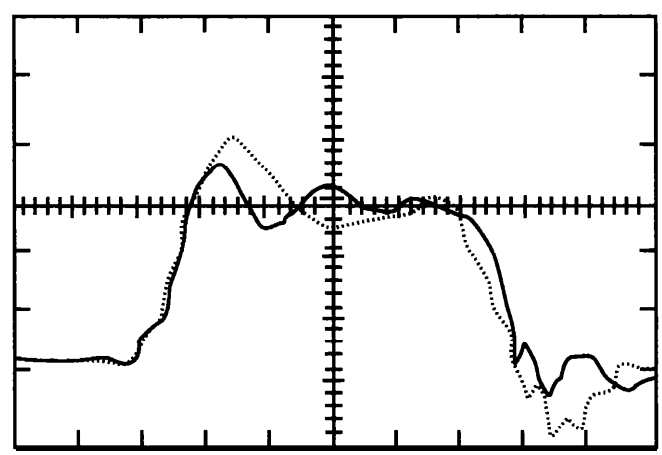


Figure 9

The performance of the circuit in figure 9 was evaluated and compared to that of the UC1710 driver into a 30 nanoFarad load. A size three P type FET and a size two N channel device were connected in series with two one-half ohm resistors to limit the shoot-through current. These FETs were driven from the UC1711 dual driver which can deliver 3 Amp peak gate drive currents for rapid transitions. The results of this test are shown in figure 10.

Driver Performance into 30nF load

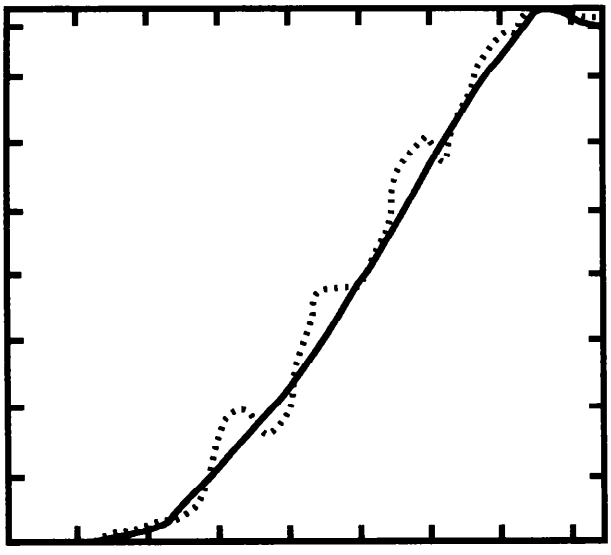


Lines: solid=UC3710, dashed=discrete
Figure 10. - VERT: 5V/DIV: HORIZ: 50 nS/DIV

The test results indicate very similar performance into this load from either technique. Obviously, the "homebrew" approach utilizes a total of three devices in comparison to a single UC1710 driver to obtain essentially the same high speed performance. Additionally, the cost of the P channel FET alone may exceed the price of the UC1710 device, not to mention the difference in PC board real estate. As a final note, the discrete FET approach required over 10 milliamps more supply current than the single UC1710 driver or a increase in supply current of twenty percent. Results of this test shown in figures 11 and 12.

RISE AND FALL TRANSITION PERFORMANCE INTO 30 nF

RISE TIMES (Fig 11.)



FALL TIMES (Fig 12.)

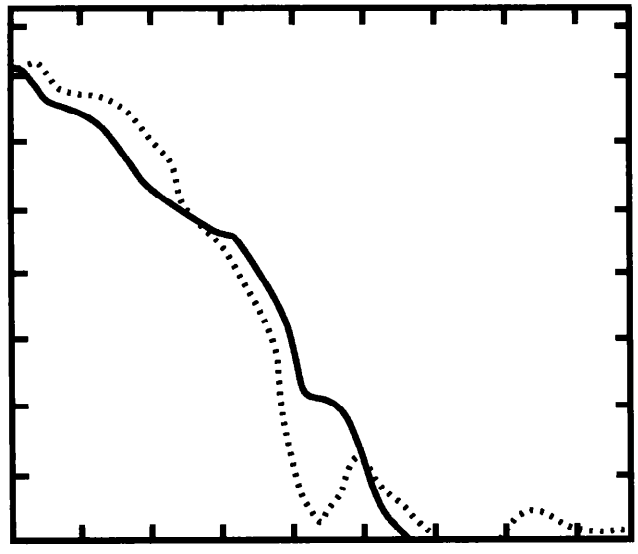


PHOTO SCALES (BOTH): VERT=2V/DIV, HORIZ=10 nS/DIV
LINES: SOLID = UC3710; DASHED = DISCRETE CIRCUIT OF FIGURE 9.

POWER DEVICES

IGBTs and MCTs: While existing generations of power MOSFETs continue to be enchanced for lower RDS(on) and faster recovery internal diodes, alternative new devices have also been introduced. Among the most popular, and viable for high voltage high power applications are IGBTs (Insulated Gate Bipolar transistors) and MCTs (MOS Controlled Thyristors). Although frequently drawn as an NPN structure, the IGBT actually resembles a PNP bipolar transistor with an internal MOS device to control the base drive. Indicative by its description, the MCT is essentially an SCR structure also utilitzing a MOS drive stage. Both devices offer significant cost advantages over MOSFETs for a given power capability.

MOSFET, IGBT and MCT Gate Drives: There are numerous reasons for driving the MOSFET gate to a negative potential during the device's off state. Degradation of the gate turn-on threshold over time and especially following high levels of irradiation are amongst the most common. However, with IGBTs, the important concern is the ability to keep the device off following turn-off with a high drain current flowing. On larger IGBT's with ratings up to 300 Amps, inductive effects caused by the device's package alone can "kick" the effective gate-to-emitter voltage positive by several Volts at the die - even with the gate shorted to the emitter at the package terminals Actually, this is the result of the high current flowing in the emitter lead (package) inductance which can less than 1nH. The corresponding voltage drop changes polarity at turn off, thus pulling the emitter below the gate, or ground. If high enough, a fast turn off will be followed by a parasitic turn-on of the

switch, and potential destruction of the semiconductor. Applying the correct amplitude of negative gate voltage can insure proper operation under these high current turn-off conditions. Also, the negative bias protects against turn-on from high dv/dt related changes that could couple into the gate through the "Miller" capacitance.

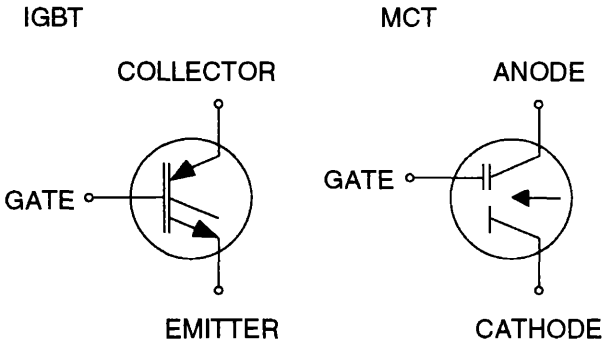


Figure 13 - IGBT and MCT Diagrams

Unlike power MOSFET switches, IGBT transconductance continues to increase with gate voltage. While most MOSFET devices peak with about 10 to 12 Volts at the gate, IGBT performance steadily improves up to the suggested 16 Volt maximum gate voltage. Typically, most IGBT manufacturers recommend a negative drive voltage between -5 and -15V. Generally, it is most convenient to derive a negative voltage equal in amplitude to the positive supply rail, and ±15V is common.

The gate charge required by an IGBT (for a given voltage and current rating) is noticeably less than that of a MOSFET. Part of this is due to the better utilization of silicon which allows the IGBT die to be considerably smaller than its FET counterpart. Additionally, the IGBT (being a bipolar transistor) does not suffer from the severe "Miller" effects of the MOS devices, easing the drive requirements in a given application. However, because of their advantages, most available IGBTs have fairly high gate charge demands - simply because of their greater power handling capability.

In contrast, MCTs (MOS Controlled Thyristors) exhibit the highest silicon utilization level among power switching devices. While relatively new to the market, these devices are quickly gaining acceptance in very high power (above several kilowatts) applications because of their high voltage (1000V) and high current (to 1000A) capability. Recently introduced parts boast maximum ratings to one megawatt, ideal for large industrial motor drives and high power distribution-even at the substation level. These devices are essentially MOS controlled SCRs and are intended for low frequency switchmode conversion. They will most likely replace high power discrete transistors, Darlingtons and SCRs because of their higher efficiency and lower cost.

Gate Charge and Effective Capacitance with Negative Bias: While several MOSFET and IGBT manufacturers recommend negative gate voltages in the device's off state, few publish any curves or information about gate charge characteristics when the gate is below zero Volts. This complicates the gate drive circuit design as each IGBT, MOSFET or MCT switch must be evaluated by the user over the ranges of operation conditions. A test fixture as shown in Figure 14 can be used to provide empirical generalizations for devices of interest. A switched constant current source/sink has been configured using a simple dual op-amp to drive a "constant" 1mA at the device under test (DUT). Gate voltage versus time can be monitored which provides the exact gate charge requirements for a given device. Any application specific requirements can also be accommodated by modifying the test circuit with external circuitry.

Negative Gate Charge - Empirical Data: Several MOSFET, IGBT and MCT gate charge measurements were taken to establish the general characteristics with negative gate charge and effective capacitance during this third quadrant operation was calculated and compared to of the first quadrant specifications from the manufacturers data sheets. Figure 15 demonstrates the general relationships of gate charges for comparison.

Both the IGBT and MCT have similar negative bias gate charge requirements as with an applied positive bias. The MOSFET, however, exhibits a slightly reduced gate charge in its negative bias region, somewhere between 70 and 75 percent of its positive bias charge. The MOSFET's more significant "Miller" effect in the first quadrant is responsible for this since the higher effective capacitance during the plateau region does not occur with negative bias.

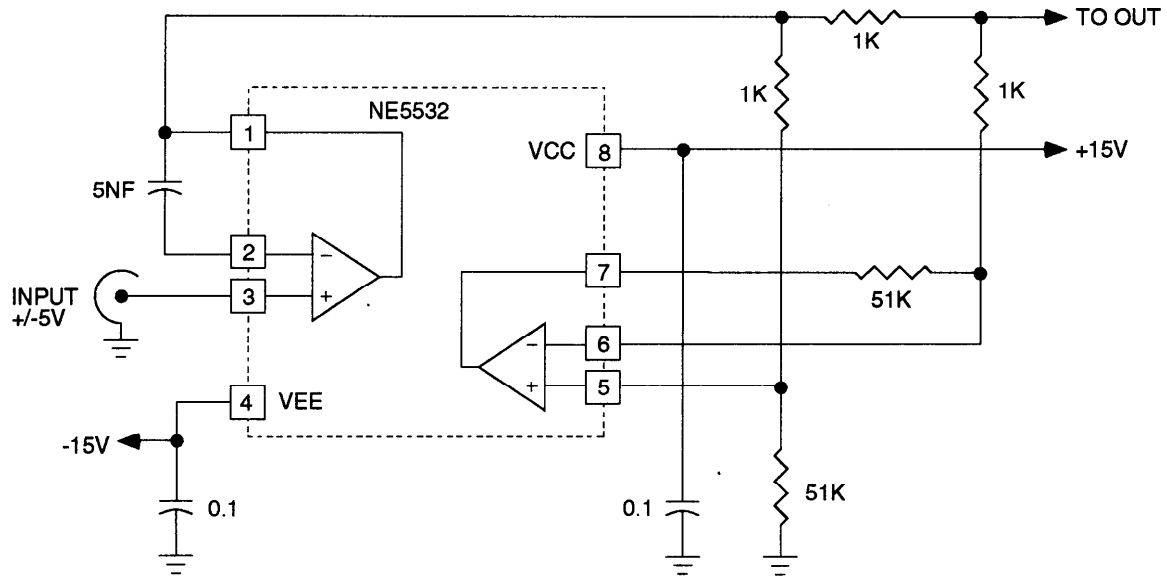


Figure 14 - Gate Charge Test Circuit

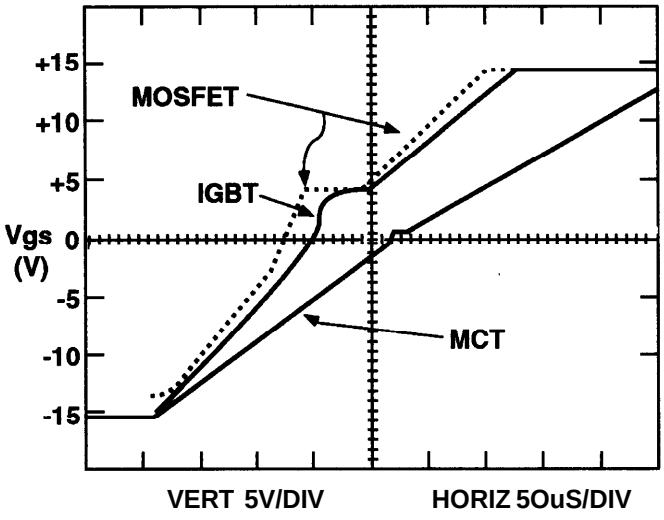


Figure 15 - Gate Charge Comparison Low to High Transition

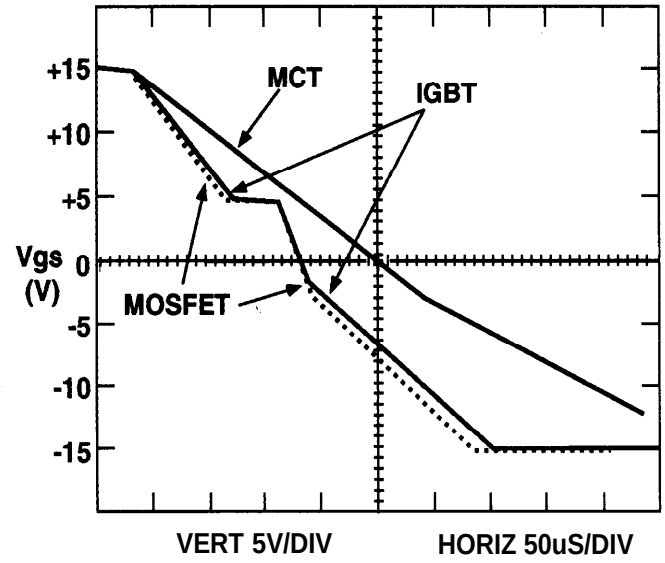


Figure 16 - Gate Drive Comparison High to Low Transition

Total Gate Power - Negative Drive Voltage Applications: All of the previously presented gate power equations still apply, however they must be modified to include the additional charge requirements of the negative supply voltage. For the sake of simplicity, a multiplication factor can be used for recalculation of the exact figures. When identical amplitudes of positive and negative supply voltages are used, for example ±15V, then the gate power utilized can be simply multiplied by a factor of two. This completes the process for the IGBTs and MCTs. The total MOSFET gate charge, on the other hand, should only be multiplied by a factor of 1.7 to 1.75 to accommodate the reduced negative bias demands. Additionally, if a negative supply voltage different than the positive rail voltage is used, for example +15 and -5, then the scaling factor must be adjusted accordingly. In this case, the new total gate power would be 1+ (-5/-15) or 1.33 times the initial 0-15V gate power for IGBTs and MCTs. The negative drive voltage scaling factor (-5/-15) would be multiplied by the 70 to 75% index if a MOSFET were used instead of an IGBT or MCT. This would result in a 1.23 to 1.25 times net increase over the initial (0-15V) gate power demand.

SUMMARY

The need for higher speed and higher current FET driver ICs has become increasingly apparent as power conversion switching frequencies are pushed towards and beyond one megaHertz. Likewise, the quest for higher overall efficiencies has resulted in creation of large, even “monster” size MOSFET geometries. These industry trends have stimulated the development of innovative MOSFET driver ICs - ones which would significantly outperform any of their predecessors, including discrete versions.

A new generation of high speed and high current MOSFET drivers has been presented. Each optimized for a unique blend of these attributes, the UC1708, UC1710 and the UC1711 devices successfully conquer the challenges of obtaining rapid transitions in MOSFET gate drive circuits.

REFERENCES

UNITRODE Application Note U-118, ”New Driver IC’s Optimize High Speed Power MOSFET Switching Characteristics”, UNITRODE LINEAR IC DATA-BOOK, IC 600

INTERNATIONAL RECTIFIER Application Notes AN-937, AN-947 and Datasheets, I.R. HEXFET Power MOSFET Designers Manual HDB-4

ADVANCED POWER TECHNOLOGY Databook 1989

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220
UC1706/3706 UC1707/3707	Dual High Current MOSFET Compatible Output Driver Dual Uncommitted High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Conversion (1706Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	16 Pin DIL "Batwing"
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25n Sec Rise and Fall Times • 25n Sec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8-Pin DIL 16-Pin DIL
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8-Pin DIL
UC1710/3710	High CurrentSpeed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8- Pin DIL 5- Pin TO-220
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 35nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8-Pin DIL
UC3724 UC3725 (PAIR)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600kHz Carrier Capability • Local Current Limiting Feature	8-Pin DIL (Pair)

UNITRODE CORPORATION
7 CONTINENTAL BLVD.. MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.