PoE Powered Device for 24 VAC Building Power Applications

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ABSTRACT

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1 Introduction

Power over Ethernet (PoE), as defined in the IEEE 802.3-2005 (clause 33) standard, provides both data and power over structured cabling. Power is supplied to the cable by Power Sourcing Equipment (PSE) that may be located at the Ethernet router/hub or between the router/hub and the Powered Device (PD). The PSE applies a nominal 48 VDC to the cable after a process that confirms a PD is connected. The PD typically includes a DC/DC converter that converts the 48 VDC to voltages required by the PD circuitry.

The PD will usually provide an auxiliary input that allows the PD to be powered from an auxiliary power source instead of the PSE. Traditionally, this auxiliary power source has been in the form of a local wall adapter. The auxiliary power source might be used as the primary source for non-PoE Ethernet systems, as a backup source for PoE systems, or as a primary source to lessen the load on the PSE of PoE systems. In addition to being capable of operating over the voltage range associated with either power source, the PD would preferably be capable of also establishing priority between the available power sources.

Commercial building infrastructures usually include one or more low voltage power systems in addition to the mains power wiring. These low voltage power systems typically provide 24 VAC to various types of devices such as security cameras, thermostats, card readers, door openers, and other conventional building control devices. Since many of the devices now being used in a building environment also utilize the building's Ethernet or PoE system, it would be desirable to have a PD that is capable of being powered by either a PoE system or the building's low voltage power system.

This application report introduces a reference design for an IEEE 802.3-2005 compliant PD which provides an auxiliary input that can accept 24 VAC building power. Although the report focuses on 24 VAC systems, the reference design could also be used for polarity-insensitive 24 VDC systems. The design utilizes a wide-input range flyback converter employing the Texas Instruments TPS23753. The TPS23753 includes a PD interface, a DC/DC controller, and an auxiliary power detect (APD) feature. Refer to datasheet SLVS853 for more information on using the TPS23753.

2 24 VAC Building Power PD Schematic

Figure 1 shows the schematic of a reference design for a 24 VAC Building Power PD. A bill of materials for this reference design is included in Appendix A, Table A-1. The reference design includes a typical 100baseT/PoE front-end that comprises the data transformers and 75 ohm network terminations. The TPS23753 IC, which is a combined PD interface and DC/DC controller, is employed in a standard isolated flyback topology to produce a 12V at 0.85A (10.2W) output. The 24 VAC auxiliary input circuit, depicted in the highlighted section of the schematic and further discussed in Section 4 below, is shown to connect to the *Vdd*, *RTN*, and *APD* nodes of the overall circuit.

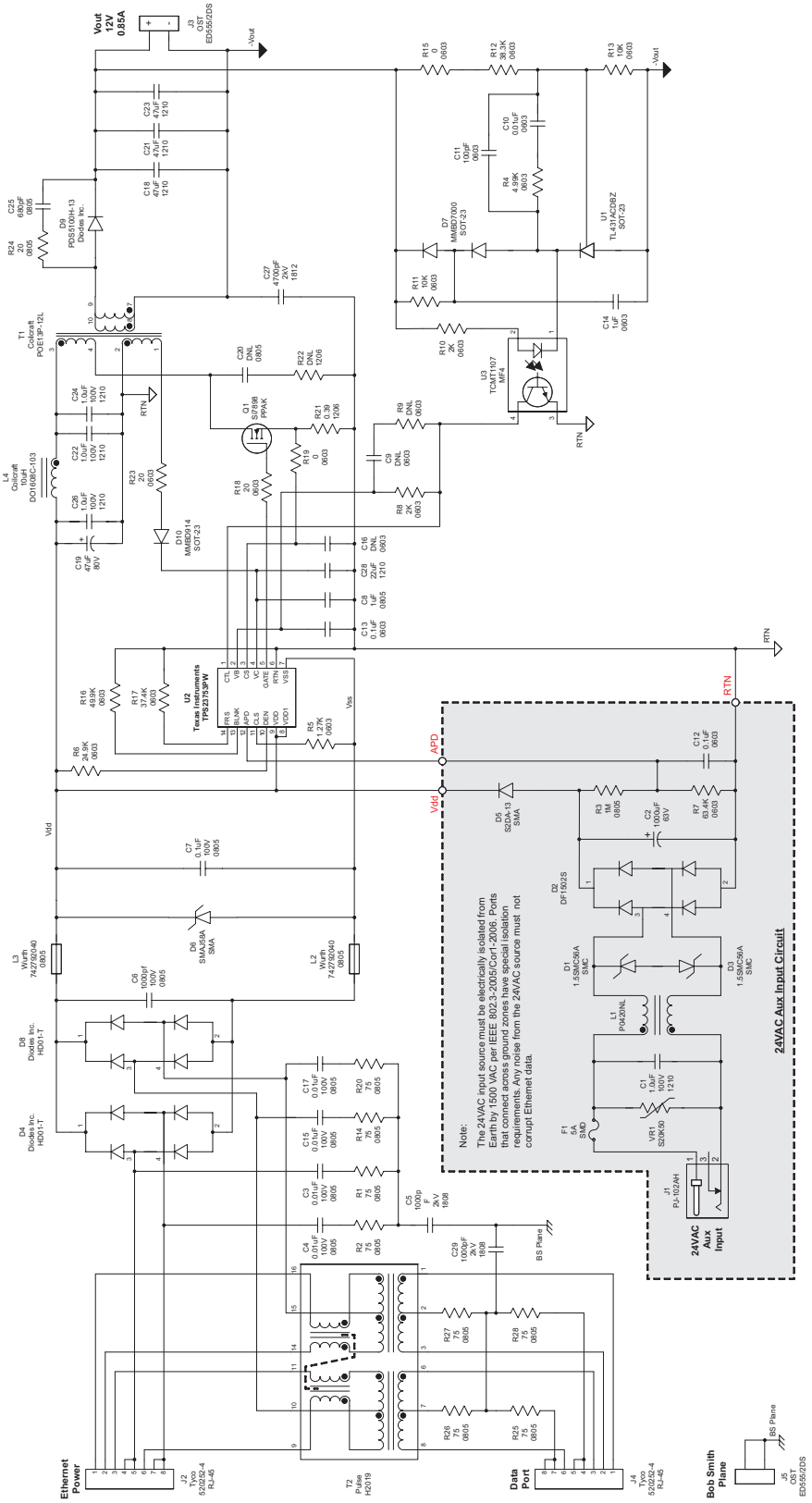

Figure 1. 24 VAC Building Power PD Schematic

3 24 VAC Building Power PD Demonstration Board

Figure 2 shows a photo of the actual demo board used for the 24 VAC Building Power PD reference design. Figure 3 through Figure 5 show the circuit board layout. The circuit board consists of two layers of 2 oz. copper on a FR-406 substrate with an overall thickness of 0.062". The overall circuit occupies approximately 60% of the 4" × 4" board size, which was chosen for convenience.

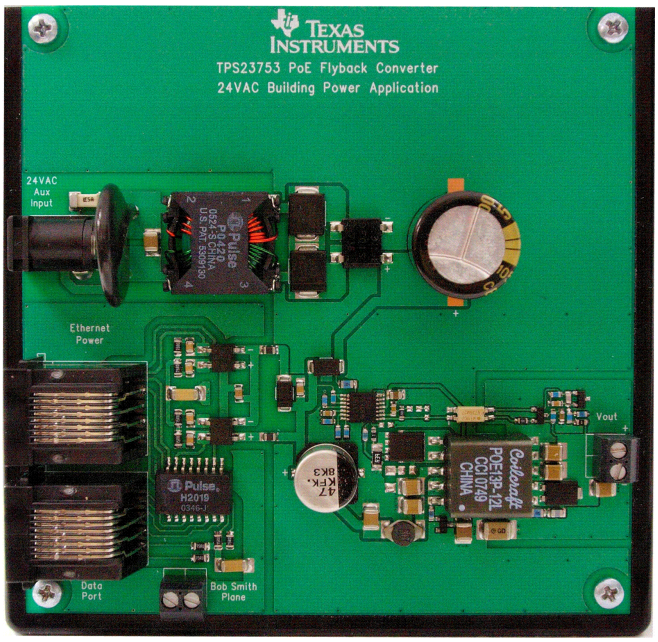

Figure 2. Building Power PD Demo Board

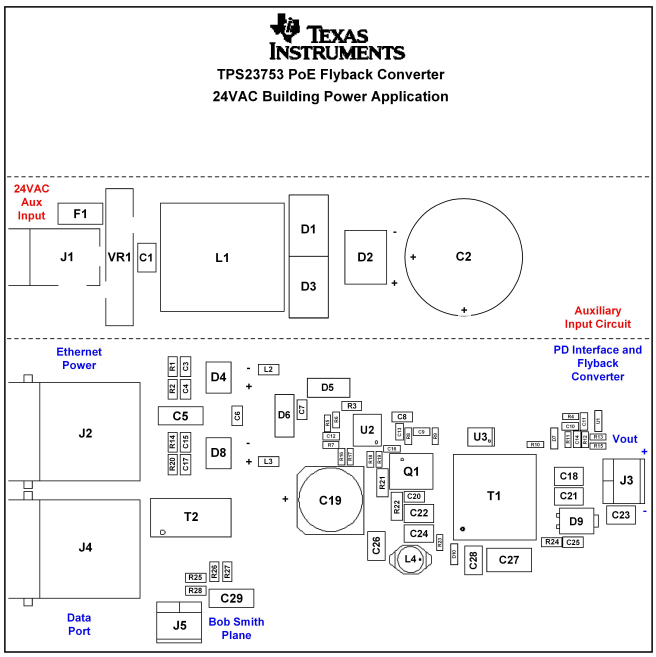

Figure 3. Demo Board - Component Layout

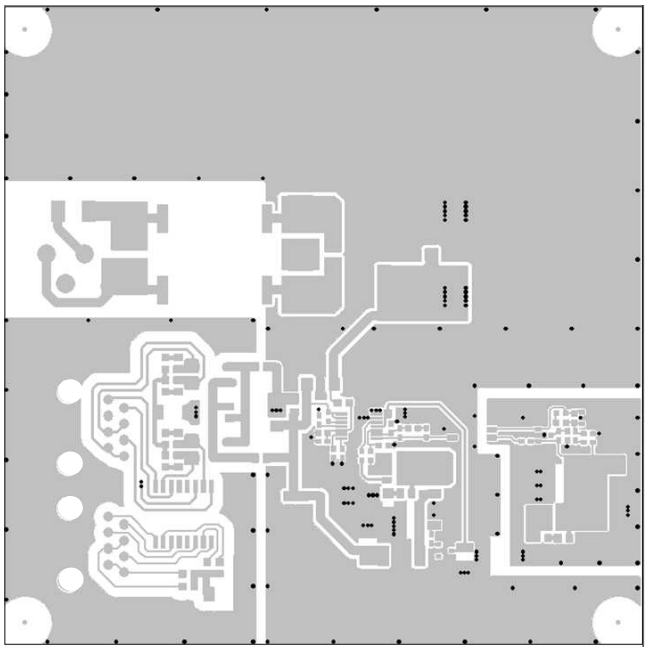

Figure 4. Demo Board – Top Copper

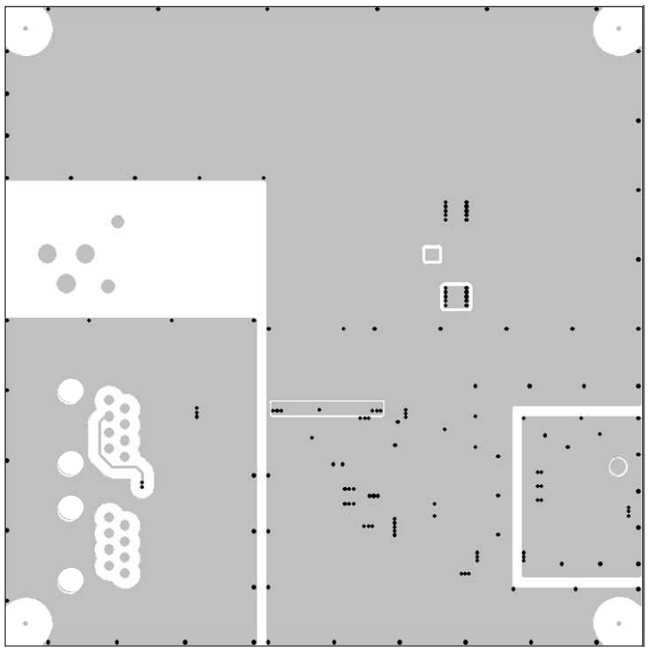

Figure 5. Demo Board – Bottom Copper

4 24 VAC Auxiliary Input Circuit

Referring to Figure 1, the 24 VAC auxiliary input circuit is shown to include the following items:

- Input fuse F1 for local current fault protection.
- MOV VR1 and back-to-back transorbs D1/D3 for input transient protection.
- Common-mode choke L1 and filter capacitor C1 for EMI filtering.
- Bridge Rectifier D2 for full-wave rectification of the 24 VAC input.
- Smoothing capacitor C2 to reduce the pulsating DC ripple voltage on the rectified output and limit the minimum DC voltage at the ripple *valley*.
- Voltage divider R3/R7 to monitor the auxiliary input voltage and provide an auxiliary power detect signal to the APD pin of the TPS23753.
- OR-ing diode D5 to OR the auxiliary input into the positive rail of the PSE derived input voltage (*Vdd*), while isolating smoothing capacitor C2 and voltage divider R3/R7 from the PSE connection.

The transient protection devices are included in the auxiliary input circuit to protect the PD against the possible harsh environment associated with the building's low voltage power system. The nature of some of the loads connected to the system may create large voltage spikes on the system wiring. In addition to these load-related transients, the system may also be prone to line surges due to lightning activity that is coupled into the building's mains power system. The installation class and transient performance criteria of the application needs to be considered when selecting the appropriate protection devices. In some cases, a fuse with a higher I^2t rating may need to be used in order to accommodate transient-related currents.

Common-mode choke L1 is included to suppress any common-mode noise emanating from the converter onto the 24 VAC system wiring. The choke also helps with suppressing incoming transients and can be used to provide some level of in-rush current limiting as discussed in Section 5.

As noted in the schematic of Figure 1, the 24 VAC source used for the auxiliary input must comply with the isolation requirements of IEEE 802.3-2005 (see Section 10, Reference 4). To comply with this standard, the 24 VAC power system must be isolated from earth ground by 1500 VAC, must not cross ground zone boundaries, and should not otherwise compromise the Ethernet network. Special attention needs to be paid to safety agency requirements when designing equipment that interfaces between separate networks.

5 24 VAC Building Power PD Design Considerations

The flyback converter used for the 24 VAC Building Power PD will need to operate over an input voltage range that covers the voltage range associated with the PoE system and the voltage range associated with the 24 VAC source. The 57 VDC maximum voltage associated with the PSE of the PoE system will dictate the high end of the overall range, while the minimum DC voltage associated with the ripple of the rectified 24 VAC source will determine the low end of the overall range.

The minimum DC operating voltage, measured at the *Vdd* node of Figure 1, is a primary focus for the 24 VAC Building Power PD design. This minimum voltage affects the maximum duty cycle of the flyback converter and the maximum current through the auxiliary input components and the primary-side power components. The following items relating to the minimum DC operating voltage have been considered for the reference design:

- The tolerance of the 24 VAC input needs to be established. The 24 VAC tolerance will normally depend on the tolerance of the 120 VAC mains voltage (U.S.) and the line and load regulation of the 24 VAC source. An overall tolerance of 20% at auxiliary input jack J1 is assumed for the reference design (i.e., 19.2 VAC_{min} to 28.8 VAC_{max}).
- Any voltage drops associated with the 24 VAC input circuit, including bridge rectifier D2 and OR-ing diode D5, will need to be accounted for in the design. A total drop of 2.8V is assumed for the reference design.

- Smoothing capacitor C2 plays a major role in establishing the minimum DC voltage. The value of this capacitor determines the amount of ripple at the output of bridge rectifier D2. The minimum DC voltage seen at *Vdd* will be equal to the valley of this ripple minus the voltage drop of Or-ing diode D5. The amount of acceptable ripple, the bridge rectifier repetitive peak current, and the capacitor ripple current need to be considered when choosing the capacitor value. A 1000μF 63V 16 mm × 31.5 mm electrolytic is used for the reference design. At low line (19.2 VAC) and maximum load, a ripple voltage of 3V and a repetitive peak rectifier current of approximately 2.3A are expected when using this capacitor. The capacitor has a 120 Hz ripple current rating which exceeds the 975 mA actually measured. Rectifier bridge D2, common-mode choke L1, and input fuse F1 have been sized to accommodate the 2.3A repetitive peak current.
- Based on the above voltage values, the minimum DC voltage seen at the *Vdd* node of the reference design can be calculated as follows:

$$\mathrm{Vdd}_{\mathrm{min}} = (19.2\,\mathrm{VAC} \times 1.414) - (2.8\mathrm{V}) - (3\mathrm{V}) = 21.34\,\mathrm{V}$$

- Flyback transformer T1 used for the reference design has a primary to secondary turns ratio of 2:1. Based on this turns ratio and a minimum *Vdd* of 21.34V, the flyback converter will have a maximum duty cycle of 53% before considering losses. The maximum duty cycle will be closer to 56% when considering losses, which is well within the 80% ±4% maximum duty cycle capability of the TPS23753 controller. The TPS23753 also includes internal slope compensation to ensure a stable current control loop at greater than 50% duty cycles.

During initial application of the 24 VAC input, a certain amount of in-rush current will be present to charge smoothing capacitor C2. The amount of in-rush current will primarily depend on the current sourcing capability of the 24 VAC source and the series impedance (resistance and inductance) associated with its wiring. In some applications, the value of common-mode choke L2 might be chosen to appreciably add to this series impedance (in addition to providing EMI filtering). The total combined impedance needs to limit the peak in-rush current to a value not exceeding the non-repetitive peak current rating of bridge rectifier D2 and the I^2t rating of input fuse F1. The maximum peak current will occur when smoothing capacitor C2 is totally discharged and the 24 VAC source is at its high line peak of 40.7V.

6 TPS23753 APD Feature

In addition to operating over the voltage range associated with either power source, the PD should also be capable of establishing priority between the available sources. Various methods of establishing priority are used for PD applications, including those discussed in Section 10, Reference 1. The reference design introduced in this application report utilizes the auxiliary power detect (APD) feature of the TPS23753 to establish priority. A simplified block diagram demonstrating this approach is shown in Figure 6.

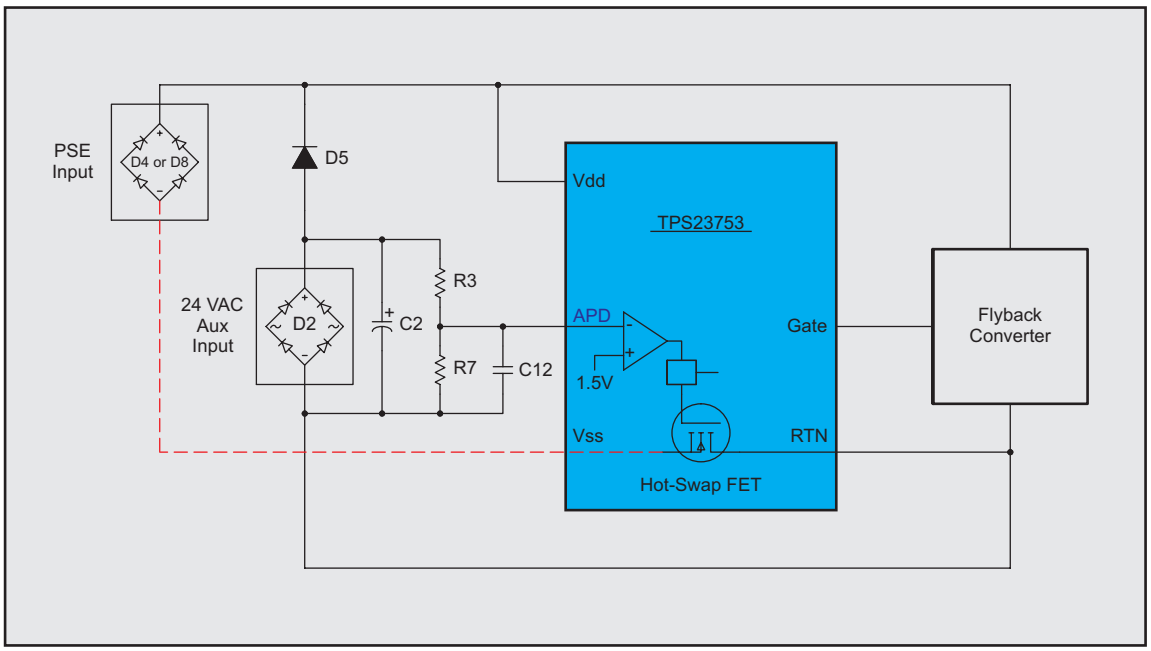

Figure 6. Simplified Block Diagram of Reference Design Priority Method

The APD feature can be configured to establish either PSE or auxiliary input priority. The configuration shown in Figure 6 is used in the reference design to give priority to the 24 VAC auxiliary input. Voltage divider R3/R7 monitors the rectified auxiliary input voltage and provides an auxiliary power detect signal to the APD input of the TPS23753. The 120 Hz ripple that exists across smoothing capacitor C2 is filtered from the APD signal by using C12. The voltage divider is chosen to cause the APD input to reach a 1.5V threshold when the 24 VAC source is at its minimum specification. The APD input includes 0.3V of hysteresis to prevent chatter once this threshold is reached.

When the APD input reaches 1.5V, the TPS23753 disables the internal hot-swap FET connected between its Vss and RTN pins. With the FET disabled, there is no longer a return path for the PSE to power the flyback converter (as indicated by the dashed-line Vss connection). Since the auxiliary input circuit is referenced to RTN instead of Vss, the 24 VAC source will take over powering the flyback converter, even though its voltage will normally be lower than the PSE voltage. The 24 VAC source will continue to have priority over the PSE as long as the APD input remains above 1.2V (1.5V minus hysteresis).

In a PoE system, the PSE will continue to provide power to the PD as long as the PD presents a valid maintain power signature (MPS). When the TPS23753 disables its internal hot-swap FET due to the presence of the 24 VAC source, the PSE should recognize that it no longer needs to provide power to the PD due to a lack of a valid MPS. This will allow the PSE to remove its voltage from the PD and reallocate its resources. The PSE will then enter its detection phase so that it can reapply power to the PD if the 24 VAC auxiliary input is subsequently removed.

7 Performance Data

Actual performance data for the 24 VAC Building Power PD reference design is included in this section. The data demonstrates the performance when operating from either the 24 VAC auxiliary input or the 48 VDC Ethernet input while at 25°C. A simplified block diagram of the test setup is shown in Figure 7. A DC power supply is used to represent the possible voltage range of the Ethernet power source, while a 24 VAC wall adapter and a variac are used to represent the possible voltage range of the 24 VAC building power source.

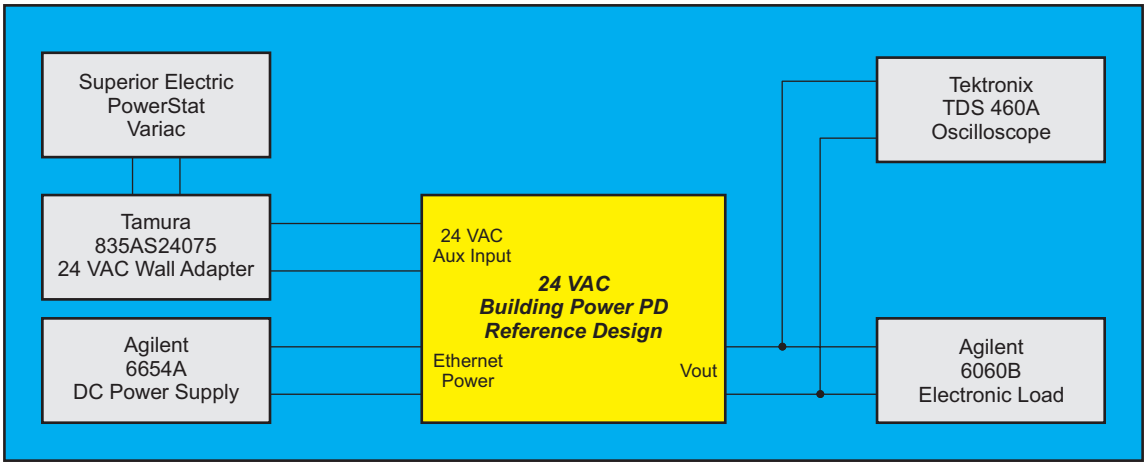

Figure 7. Simplified Block Diagram of Reference Design Test Setup

Figure 8 shows the end-to-end efficiency of the reference design over the 19.2 VAC to 28.8 VAC range of the 24 VAC auxiliary input. The efficiency measurements include all of the losses from the J1 auxiliary input connector to the J3 output connector. The AC input power measurements are based on *real* power.

Figure 9 shows the end-to-end efficiency of the reference design over the 36 VDC to 57 VDC range of the 48 VDC Ethernet input. The efficiency measurements include all of the losses from the J2 Ethernet input connector to the J3 output connector.

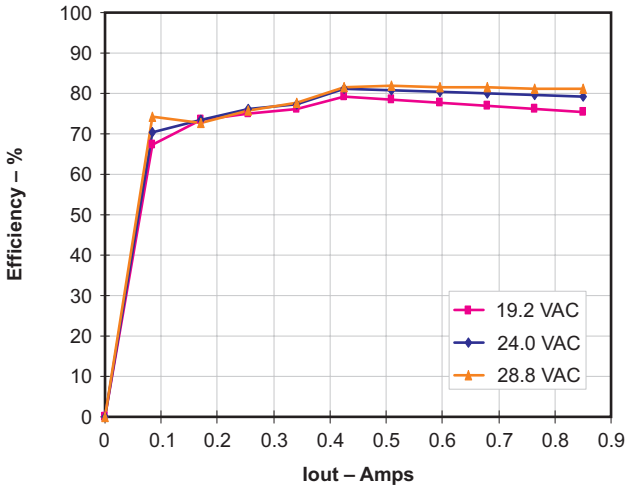

Figure 8. End-to-End Efficiency for Auxiliary Input

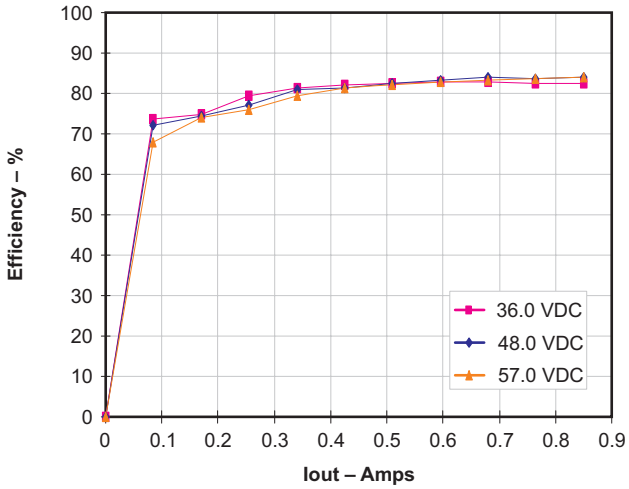

Figure 9. End-to-End Efficiency for Ethernet Input

Figure 10 shows the line and load regulation of the reference design over the 19.2 VAC to 28.8 VAC range of the 24 VAC auxiliary input.

Figure 11 shows the line and load regulation of the reference design over the 36 VDC to 57 VDC range of the 48 VDC Ethernet input.

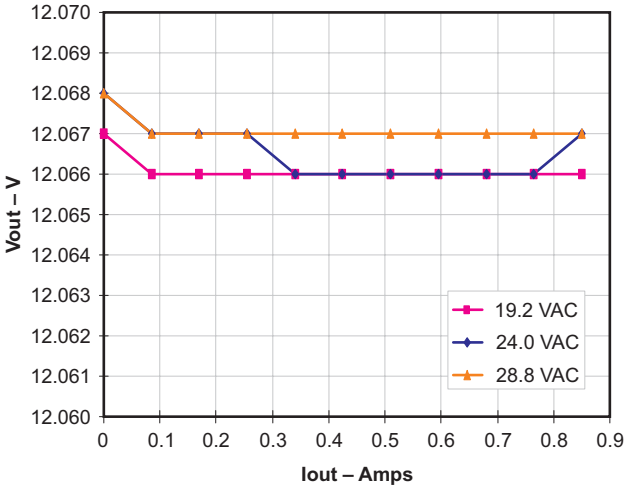

Figure 10. Line and Load Regulation for Auxiliary Input

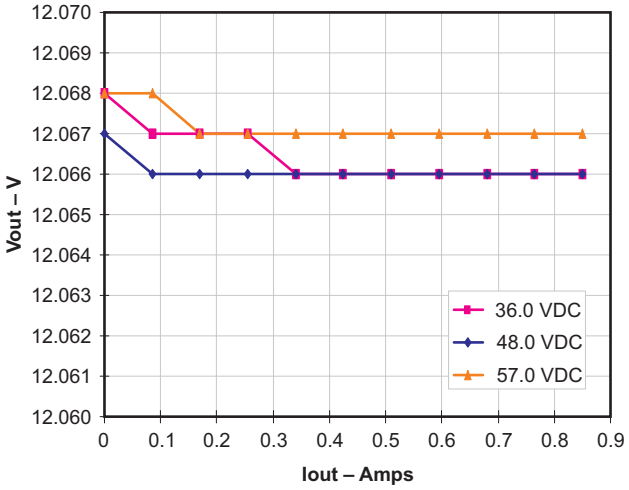

Figure 11. Line and Load Regulation for Ethernet Input

Figure 12 shows the output ripple of the reference design at maximum load over the 19.2 VAC to 28.8 VAC range of the 24 VAC auxiliary input.

Figure 13 shows the output ripple of the reference design at maximum load over the 36 VDC to 57 VDC range of the 48 VDC Ethernet input.

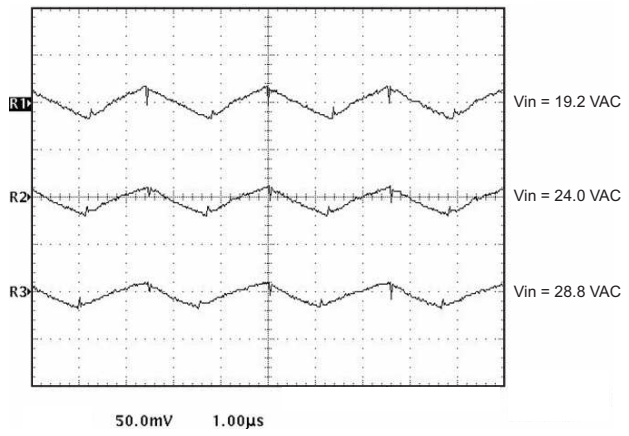

Figure 12. Output Ripple for Auxiliary Input

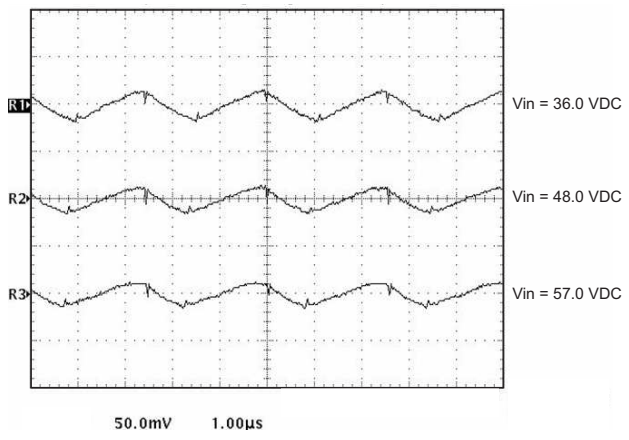

Figure 13. Output Ripple for Ethernet Input

Figure 14 shows the output noise of the reference design at maximum load over the 19.2 VAC to 28.8 VAC range of the 24 VAC auxiliary input. The output noise modulation is associated with the attenuated 120 Hz ripple of the full-wave rectified auxiliary input.

Figure 15 shows the output noise of the reference design at maximum load over the 36 VDC to 57 VDC range of the 48 VDC Ethernet input.

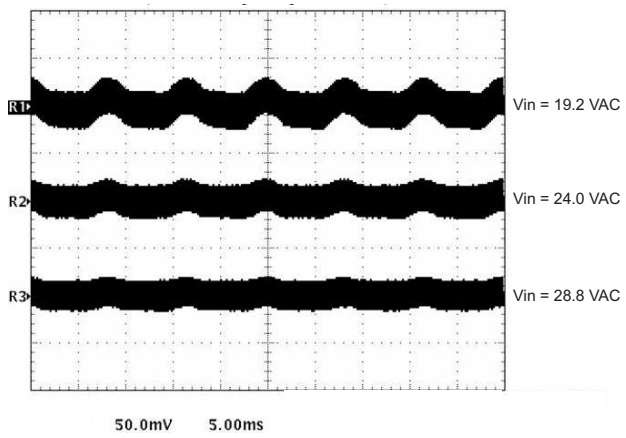

Figure 14. Output Noise for Auxiliary Input

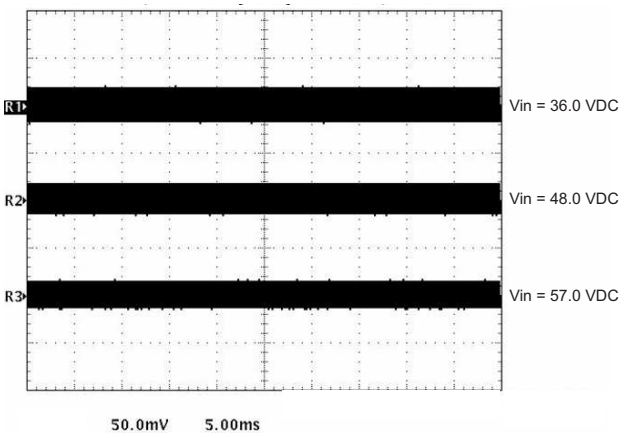

Figure 15. Output Noise for Ethernet Input

Figure 16 shows the output voltage start-up of the reference design under no load and full load for the nominal 24 VAC auxiliary input condition.

Figure 17 shows the output voltage start-up of the reference design under no load and full load for the nominal 48 VDC Ethernet input condition.

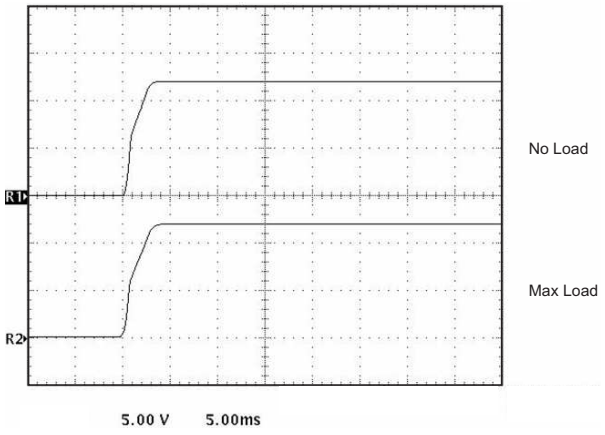

Figure 16. Output Voltage Start-up for Auxiliary Input

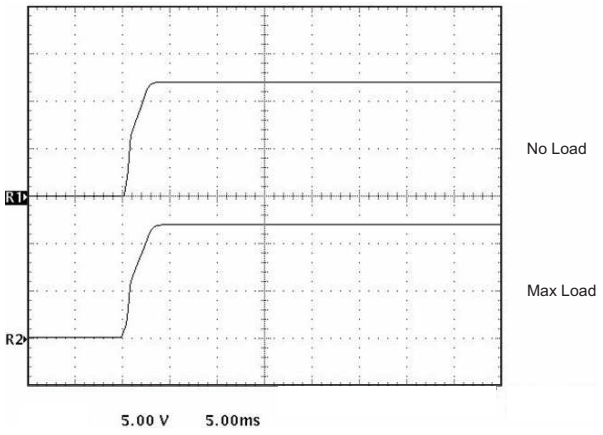

Figure 17. Output Voltage Start-up for Ethernet Input

Figure 18 shows the output transient response of the reference design for the nominal 24 VAC auxiliary input condition. The load step is from 50% to 100% with a slew rate of 0.5A/µs.

Figure 19 shows the output transient response of the reference design for the nominal 48 VDC Ethernet input condition. The load step is from 50% to 100% with a slew rate of 0.5A/µs.

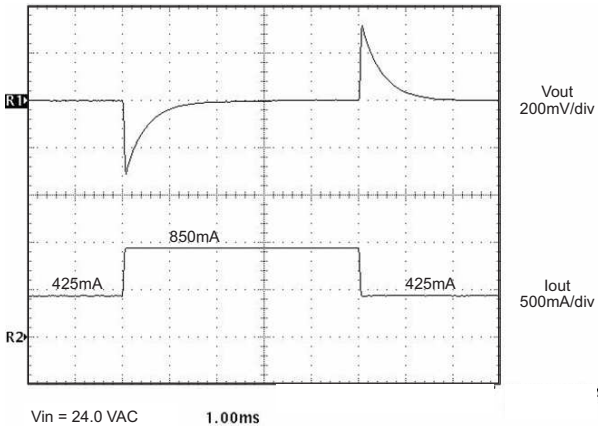

Figure 18. Transient Response for Auxiliary Input

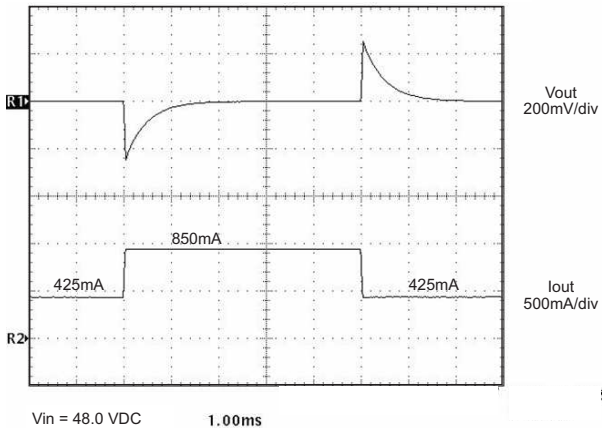

Figure 19. Transient Response for Ethernet Input

8 Input Priority Operation

Actual operation of the input priority method discussed in Section 6 is demonstrated in this section. A simplified block diagram of the test setup is shown in Figure 20. A single-port midspan injector is used as the PSE input, while a 24 VAC wall adapter is used to represent the 24 VAC building power source.

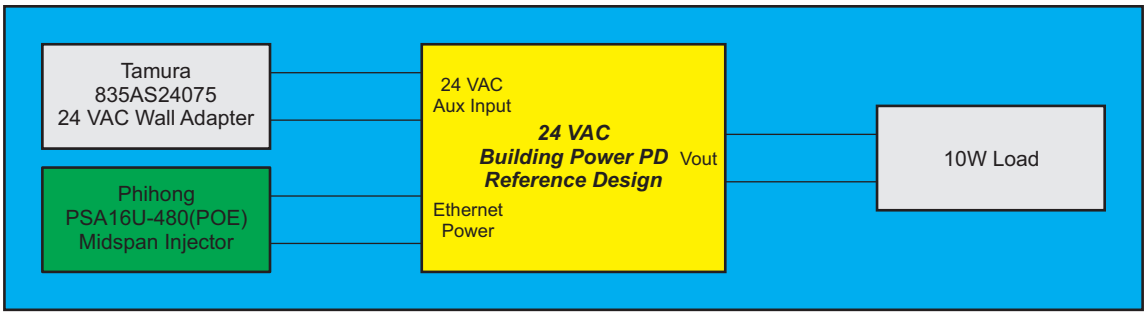

Figure 20. Simplified Block Diagram of Input Priority Operation Test Setup

Figure 21 shows the operation when the 24 VAC input is applied while the PD is being actively powered by the PSE input. The presence of the 24 VAC source is indicated by the rectified voltage across the C2 bulk capacitor used to filter the auxiliary input. Prior to application of the 24 VAC input, the flyback converter input (i.e. Vdd node) is seen to be approximately equal to the PSE voltage. After application of the 24 VAC input, the Vdd node is seen to be approximately equal to the voltage across C2. Vout remains present during this transition to the 24 VAC input. With the 24 VAC present and powering the flyback converter, the PD no longer presents an MPS to the PSE, so the PSE is seen to remove its powering voltage and enter its detection mode.

Figure 22 shows the operation when the 24 VAC input is removed. Prior to removal of the 24 VAC input, the PSE is seen to be in its detection mode. After removal of the 24 VAC input, the PD is seen to power down while awaiting the next PSE detection sequence. After this next detection sequence occurs, the PSE is seen to reapply its powering voltage to the PD.

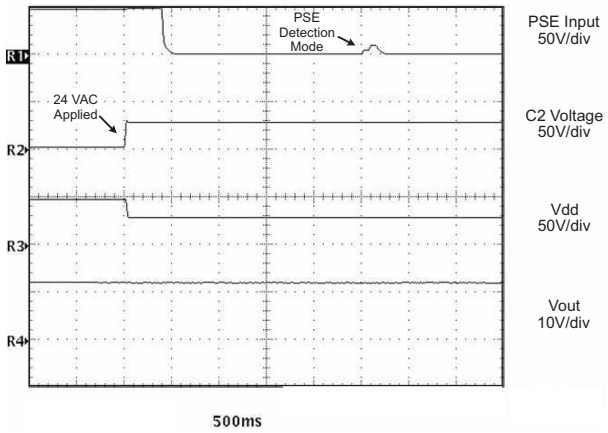

Figure 21. Application of 24 VAC Auxiliary Input

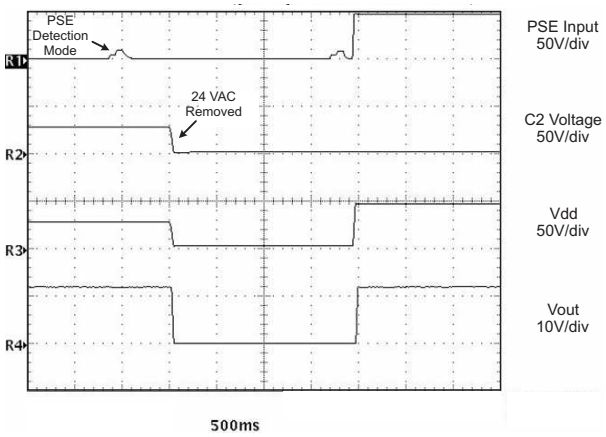

Figure 22. Removal of 24 VAC Auxiliary Input

9 Summary

This application report presents a PoE PD reference design that is compatible with the 24 VAC low voltage power systems available within most commercial building environments. This 24 VAC Building Power PD, which can be powered by the PSE of a conventional PoE system or by the building's low voltage power system, provides a versatile solution for building control applications. The reference design uses the Texas Instruments TPS23753 PD interface and DC/DC controller in a flyback converter topology to provide a 12V output over the wide input range presented by the two different power systems. The reference design further demonstrates how the auxiliary power detect (APD) feature of the TPS23753 can be used to give priority to the 24 VAC building power input.

10 References

1. *Wall Adapter Powers IEEE 802.3af Powered Device*, Edward Jung, Application Report (SLVA220), Texas Instruments, January 2006
2. *TPS23753: IEEE 802.3-2005 PoE Interface and Isolated Converter Controller*, Data sheet (SLVS853), Texas Instruments, June 2008
3. *TPS23750: Integrated 100-V IEEE 802.3af PD and DC/DC Controller*, Data sheet (SLVS590A), Texas Instruments, August 2005 Revision
4. *IEEE Std 802.3-2005/Cor 1-2006*, June 2006

Appendix A Bill of Materials

Table A-1. 24 VAC Building Power PD Reference Design Bill of Materials

QTY	REFERENCE DESIGNATOR	DESCRIPTION	SIZE	MFR	PART NUMBER
0	C9	Not Used	0603	Std	Std
0	C16	Not Used	0603	Std	Std
0	C20	Not Used	0805	Std	Std
1	C11	Capacitor, Ceramic, 100 pF, 50 V, COG, 5%	0603	Std	Std
1	C25	Capacitor, Ceramic, 680 pF, 100 V, COG, 5%	0805	Std	Std
1	C6	Capacitor, Ceramic, 1000 pF, 100 V, X7R, 10%	0805	Std	Std
2	C5, C29	Capacitor, Ceramic, 1000 pF, 2 kV, X7R, 10%	1808	Johanson	202R29W102KV4E
1	C27	Capacitor, Ceramic, 4700 pF, 2 kV, X7R, 10%	1812	Murata	GR443DR73D472KW01L
1	C10	Capacitor, Ceramic, 0.01, 50 V, X7R, 10%	0603	Std	Std
4	C3, C4, C15, C17	Capacitor, Ceramic, 0.01 µF, 100 V, X7R, 10%	0805	Std	Std
2	C12, C13	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 10%	0603	Std	Std
1	C7	Capacitor, Ceramic, 0.1 µF, 100 V, X7R, 10%	0805	Murata	GCM21BR72A104KA37L
1	C14	Capacitor, Ceramic, 1 µF, 16 V, X5R, 10%	0603	Std	Std
1	C8	Capacitor, Ceramic, 1 µF, 16 V, X7R, 10%	0805	Std	Std
4	C1, C22, C24, C26	Capacitor, Ceramic, 1 µF, 100 V, X7R, 10%	1210	TDK	C3225X7R2A105K
1	C28	Capacitor, Ceramic, 22 µF, 16 V, X5R, 20%	1210	TDK	C3225X5R1C226M
3	C18, C21, C23	Capacitor, Ceramic, 47 µF, 16 V, X5R, 20%	1210	Murata	GRM32ER61C476M
1	C19	Capacitor, Aluminum, 47 µF, 80 V, 20%,	10 mm × 10.2 mm	Panasonic	EEEFK1K470P
1	C2	Capacitor, Aluminum, 1000 µF, 63 V, 20%	16 mm × 31.5 mm	Panasonic	EEUFC1J102U
2	D1, D3	Diode, TVS, 56 V ,1500 W	SMC	On Semi	1.5SMC56A
1	D2	Bridge Rectifier, 200 V, 1.5 A	DF-S	Diodes Inc.	DF1502S
2	D4, D8	Bridge Rectifier, 100 V, 0.8 A	MINI DIP4	Diodes, Inc	HD01-T
1	D5	Diode, Rectifier, 200 V, 1.5 A	SMA	Diodes Inc.	S2DA-13
1	D6	Diode, TVS, 58 V 1W	SMA	Diodes Inc.	SMAJ58A
1	D7	Diode, Dual Series, 100 V, 200 mA	SOT-23	On Semi	MMBD7000
1	D9	Diode, Schottky, 100 V, 5 A	PowerDi-5	Diodes Inc.	PDS5100H-13
1	D10	Diode, Switching, 100 V, 200 mA	SOT-23	On Semi	MMBD914
1	F1	Fuse, 125 V, 5 A, SMD	2512	Littelfuse	0451005
1	J1	Connector, 2.1 mm Power Jack, 5 A	0.35" × 0.57"	CUI Inc.	PJ-102AH
2	J2, J4	Connector, Jack Modular, 8 Position	0.705" x 0.820"	AMP	520252
2	J3, J5	Terminal Block, 2 pin, 6 A, 3.5 mm	0.27" × 0.25"	OST	ED555/2DS

Table A-1. 24 VAC Building Power PD Reference Design Bill of Materials (continued)

QTY	REFERENCE DESIGNATOR	DESCRIPTION	SIZE	MFR	PART NUMBER
1	L1	Common-Mode Choke, 1.32 mH, 3.3 A	0.67" × 0.77"	Pulse GCI	P0420NL G088214LF
2	L2, L3	Ferrite Bead, 600 Ω, 2A	0805	Wurth	742792040
1	L4	Inductor, 10 µH, 1.1 A, 160 mΩ	0.26" × 0.09"	Coilcraft	DO1608C-103
1	Q1	MOSFET, 150 V, 3A, 95 mΩ	PPAK	Vishay	Si7898DP
0	R9	Not Used	0603	Std	Std
0	R22	Not Used	1206	Std	Std
2	R15, R19	Resistor, Chip, 0 Ω, 1/16W, 5%	0603	Std	Std
1	R21	Resistor, Chip, 0.39 Ω, 1/4W, 1%	1206	Std	Std
2	R18, R23	Resistor, Chip, 20 Ω, 1/16W, 1%	0603	Std	Std
1	R24	Resistor, Chip, 20 Ω, 1/10W, 1%	0805	Std	Std
8	R1, R2, R14, R20, R25–R28	Resistor, Chip, 75 Ω, 1/10W, 1%	0805	Std	Std
1	R5	Resistor, Chip, 1.27 kΩ, 1/16W, 1%	0603	Std	Std
2	R8, R10	Resistor, Chip, 2 kΩ, 1/16W, 1%	0603	Std	Std
1	R4	Resistor, Chip, 4.99 kΩ, 1/16W, 1%	0603	Std	Std
2	R11, R13	Resistor, Chip, 10 kΩ, 1/16W, 1%	0603	Std	Std
1	R6	Resistor, Chip, 24.9 kΩ, 1/16W, 1%	0603	Std	Std
1	R17	Resistor, Chip, 37.4 kΩ, 1/16W, 1%	0603	Std	Std
1	R12	Resistor, Chip, 38.3 kΩ, 1/16W, 1%	0603	Std	Std
1	R16	Resistor, Chip, 49.9 kΩ, 1/16W, 1%	0603	Std	Std
1	R7	Resistor, Chip, 63.4 kΩ, 1/16W, 1%	0603	Std	Std
1	R3	Resistor, Chip, 1MΩ, 1/10W, 1%	0805	Std	Std
1	T1	XFMR, Flyback, 12V, 1.08A, 13W	0.530" x 0.699"	Coilcraft	POE13P-12L
1	T2	XFMR, Center-tapped, VOIP	0.500" × 0.370"	Pulse	H2019
1	U1	IC, Shunt Regulator, 2.495 V, 1%	SOT23-3	TI	TL431ACDBZR
1	U2	IC, IEEE 802.3-2005 PoE Interface and DC/DC Controller	PW	TI	TPS23753PW
1	U3	IC, Photocoupler, 3750 VRMS, 80–160% CTR	MF4	Vishay	TCMT1107
1	VR1	MOV, 65V, 1W	20mm disc	Epcos Panasonic	SIOV-S20K50 ERZV20D820

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