TPS40211 – SEPIC Design for MR-16 LED

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ABSTRACT

This document describes a reference design for multifaceted reflector MR-16 LED lighting by using the TPS40211 to construct a SEPIC converter. This driver provides 700 mA to a string of three white LEDs and has the capability to operate with 12 Vac or 12 Vdc. The TPS40211 has been selected for SEPIC application because it offers many advantages – long lifetime as the discard of E-cap in the design and good performance in power factor. This document presents a thorough analysis of SEPIC converter operation and performance along with design optimization guidelines. Experimental results obtained on 10-V/700-mA MR-16 lighting are provided.

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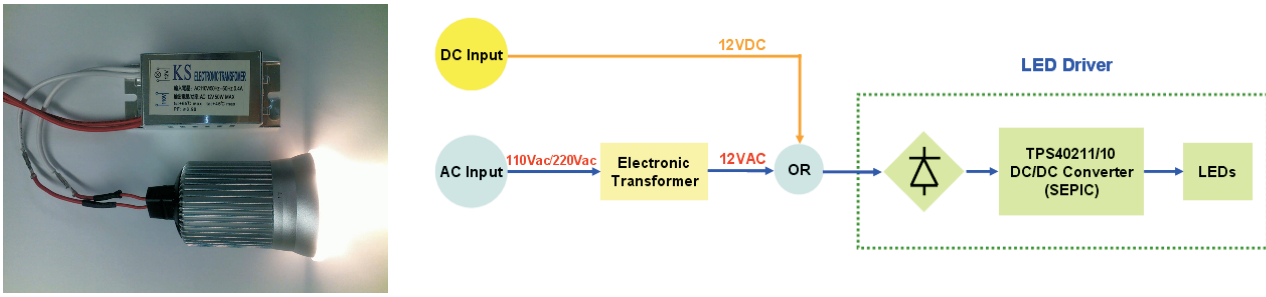
1 Introduction

This document provides the detail description of the implementation of the MR-16 LED lighting design by using the TPS40211 dc/dc controller. The block diagram of a 10-V, 700-mA, MR-16 LED lighting system is shown in Figure 1. The input voltage source of the LED driver can be supplied from a 12-Vdc input or a 12-Vac input, which is converted from a universal ac input via an electronic transformer, respectively. In addition, in order to keep the lumen of LED constant, the lighting system of the MR-16 is made of a constant current control scheme for the feedback loop circuit.



(a) MR-16 LED Lamp with Electronic Transformer **(b) System Block Diagram**

Figure 1. Block Diagram of 10-V, 700-mA, MR-16 LED Lighting System

2 Features

- Power driver without E-Cap design
- Longer lifetime of LED lamp
- Power factor higher than 0.9
- Compatible with 12-Vac electronic transformers without glitter
- Output current accuracy less than 1%
- Improve input inrush current
- OVP, OCP, and SCP protection

3 Application Schematic

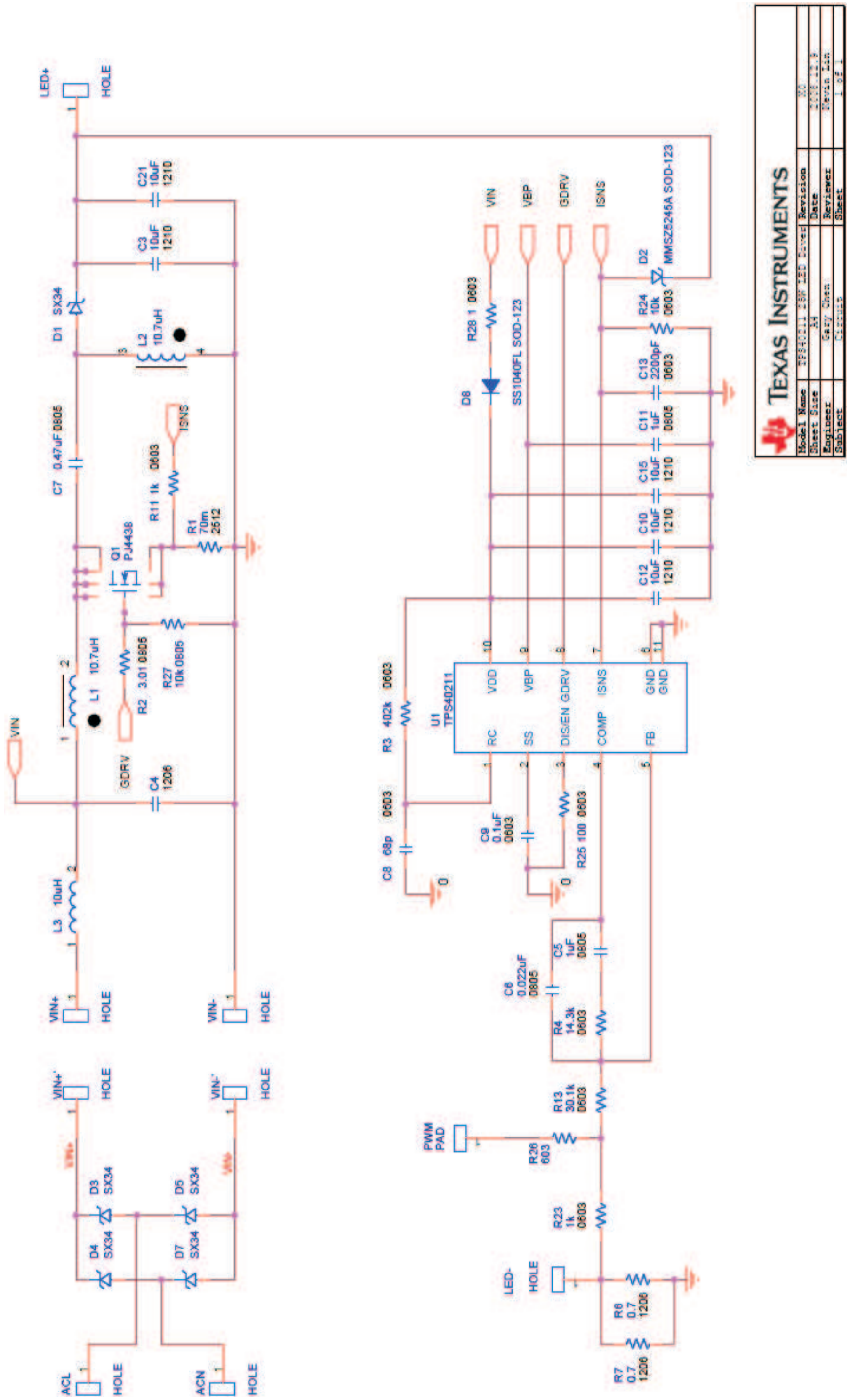


Figure 2. MR-16 Design Example – I/P: 12 Vdc/12 Vac, O/P: 10-V at 700-mA LED Driver

4 Basic Operation

The SEPIC converter topology shown in Figure 3 consists of an input capacitor (C_{IN}), output capacitor (C_{OUT}), coupled inductors (L1, L2), ac coupling capacitor (C_P), power MOSFET (Q1), and freewheel diode (D1).The SEPIC converter is operated in the continuous conduction mode (CCM) during the switching-on period shown in Figure 6. The SEPIC converter is operated in the continuous conduction mode (CCM) during the switching-off period shown in Figure 7. The waveforms of the SEPIC converter switching voltage and current are shown in Figure 4 and Figure 5, respectively.

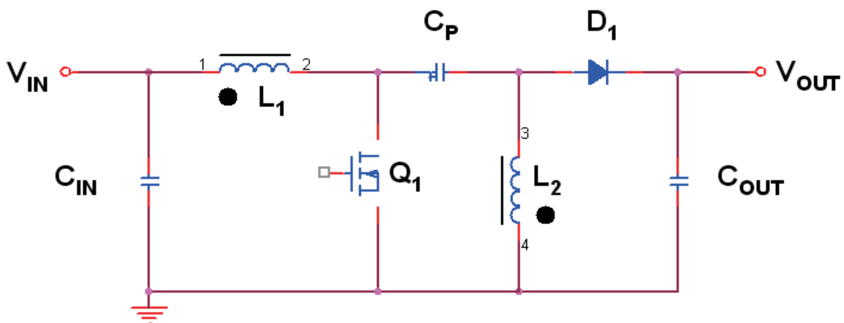


Figure 3. Simple Circuit Diagram of SEPIC Converter

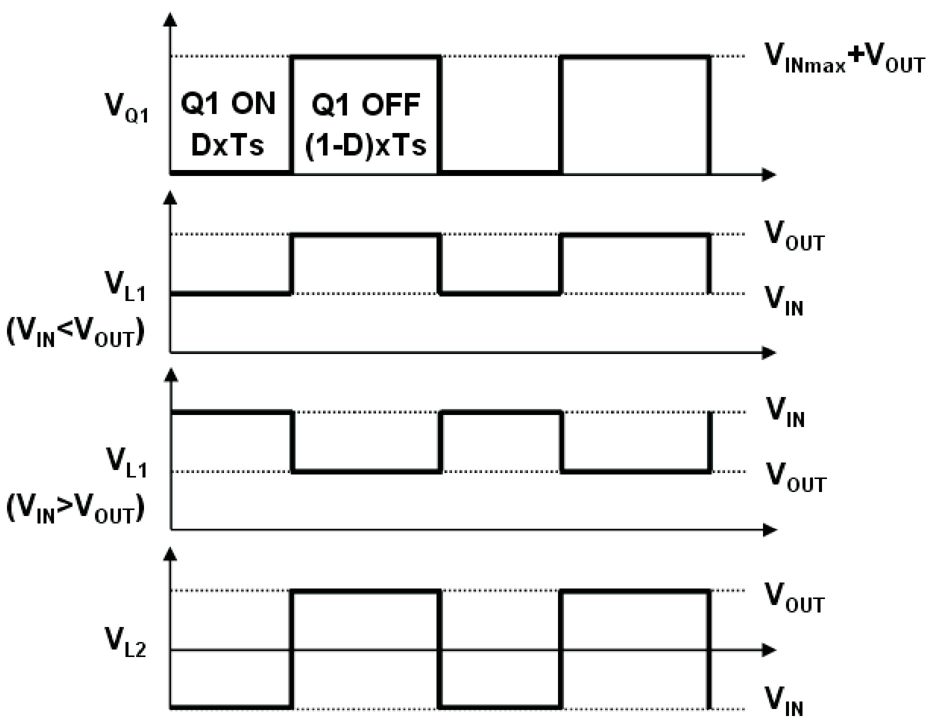


Figure 4. SEPIC Component Voltages During CCM

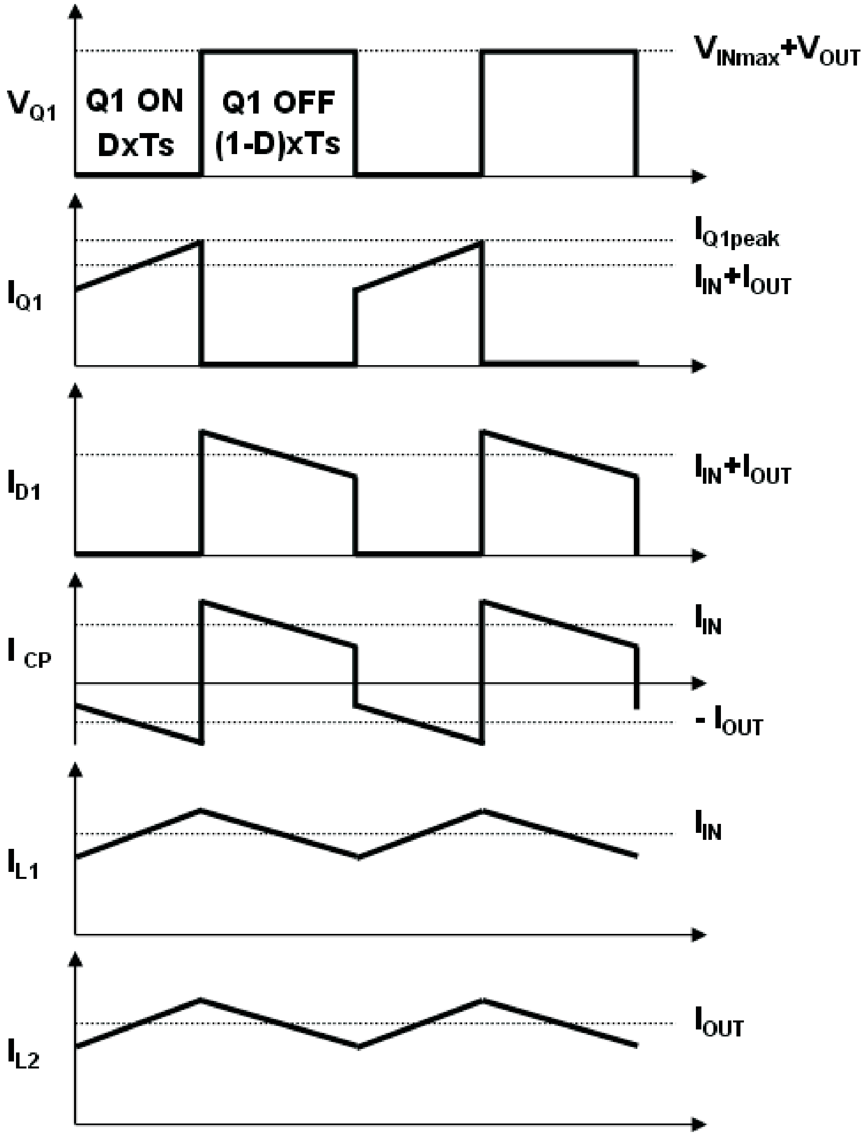


Figure 5. SEPIC Component Currents During CCM

4.1 During Switching Turnon

During the switch (Q1) ON time, the voltage across both inductors is equal to V_{IN}. When the switch is ON, capacitor Cp is connected in parallel with L2. The voltage across L2 is the same as the capacitor voltage, $-V_{IN}$. Diode D1 is the reverse bias, and the load current is being supplied by capacitor COUT. During this period, energy is being stored in L1 from the input and in L2 from Cp.

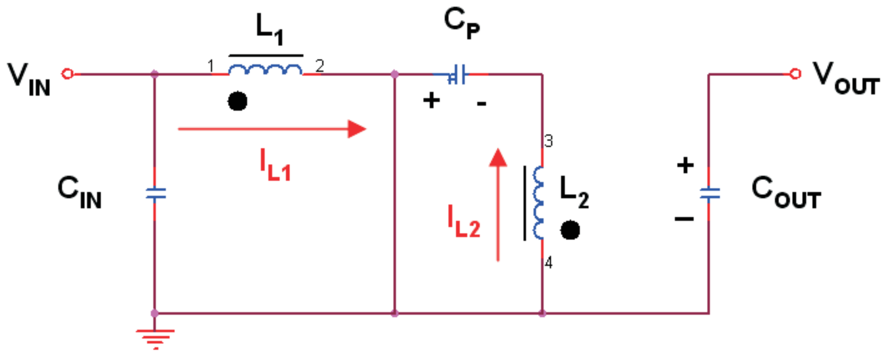


Figure 6. SEPIC During CCM Operation When Q1 is Switching ON

4.2 During Switching Turnoff

During the switch (Q1) OFF time, the current in L1 continues to flow through Cp and D1, and then into C_{OUT}. In the meantime, the Cp is charged and ready for the next cycle. The current in L2 also flows into C_{OUT} and the load, ensuring that C_{OUT} is ready for the next cycle.

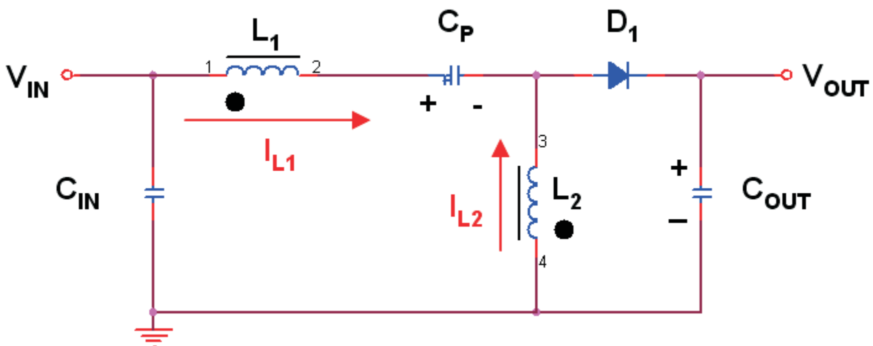


Figure 7. SEPIC During CCM Operation When Q1 is Switching OFF

5 SEPIC Converter Design Guide

This SEPIC converter uses current mode control to simplify the stabilization of the control loop. Peak current in the FET is limited by the pulse current limiting of the TPS40211. Switching frequency is 560 kHz, allowing low output current handling and low output ripple with small inductors and capacitors while remaining in the continuous inductor current mode. When the converter is operated in continuous conduction mode and the duty cycle is 50% or greater, the remedy for this condition is to apply a compensating ramp from the oscillator to the signal going to the pulse width modulator.

5.1 Duty Cycle Consideration

Assuming 100% efficiency, the duty cycle, D, for a SEPIC converter operated in CCM is given by

- Calculate minimum duty cycle

$$\text{Dmin} = \frac{V_{OUT} + V_D}{V_{INmax} + V_{OUT} + V_D} \tag{1}$$

  where V_D is the forward voltage drop of the Schottky diode D1.

- Calculate maximum duty cycle

$$\text{Dmax} = \frac{V_{OUT} + V_D}{V_{INmin} + V_{OUT} + V_D} \tag{2}$$

5.2 Inductor Selection

The inductance ripple current is to allow approximately 20% to 40% of the maximum input current at the minimum input voltage. The ripple current is given by

$$\Delta I_L = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} \times 40\% \quad (3)$$

To account for load transients, the coupled inductor's saturation current rating needs to be at least 20% higher than the steady-state peak current in the high-side inductor, is given by

$$I_{L1peak} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} \times \left[1 + \frac{40\%}{2}\right] \quad (4)$$

$$I_{L2peak} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

Ideally, a single core wound the same number of windings; the mutual inductance forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, because the inductors do not have equal inductance, the ripple currents are not exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what is needed. With two separate inductors, the inductance is given by

$$L1 = L2 > \frac{V_{INmin} \times D_{max}}{2f s \times \Delta I_L} \quad (6)$$

The converter is ensured to be operated in a continuous conduction mode (CCM) at light load; the inductor value L1 and L2 is given by

$$L1 = L2 > \frac{V_{INmax} \times D_{min}}{f s \times I_{OUT}\left[\frac{V_{OUT}}{V_{INmax}} + 1\right]} \quad (7)$$

5.3 Output Capacitor Selection

When the Q1 is on, the output capacitor must provide the load current. The output capacitor, therefore, must have enough capacitance. In this EVM design, the ceramic capacitors are used, the ESR can be ignored and the equation is given by

$$C_{OUT} \geq \frac{I_{OUT} \times D_{max}}{\Delta V_{RPL} \times f s} \quad (8)$$

where ΔV_{RPL} is the output voltage ripple which is desired by the requirement of the design.

5.4 Input Capacitor Selection

The input capacitor can be very small, because of the filtering properties of the SEPIC topology. Usually, C_{IN} can be ten times smaller than C_{OUT}.

$$C_{IN} = \frac{C_{OUT}}{10} \quad (9)$$

5.5 Coupling Capacitor Selection

The coupling capacitor, C_P, sees large RMS current relative to the output power:

$$I_{CPrms} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} \times \sqrt{\frac{1 - D_{max}}{D_{max}}} \tag{10}$$

The coupling capacitor C_P is given by

$$C_P = \frac{I_{OUT} \times D_{max}}{\Delta V_{CP} \times f s} \tag{11}$$

where ΔV_{CP} is the ripple voltage which is across C_P.

The maximum voltage across C_P is V_{IN}.

5.6 Power MOSFET Consideration

This topology places higher stresses on both the Q1 and the D1 than do other PWM topologies. The power MOSFET, Q1, must be carefully selected for handling the peak voltage and current. The current rating of the power FET determines the SEPIC converter's maximum output current. The maximum voltage across the drain to the source is $V_{INmax} + V_{OUT}$. The peak current is given by:

$$I_{Q1peak} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} + I_{OUT} + \Delta I_L \tag{12}$$

The RMS current of the Q1 is given by

$$I_{Q1rms} = \frac{V_{OUT} \times I_{OUT}}{V_{INmin} \times \eta \times \sqrt{D_{max}}} \tag{13}$$

5.7 Output Diode Consideration

The output diode D1 must be able to handle the same peak current as Q1, I_{Q1peak} do. The diode must also be able to withstand a reverse voltage greater than the maximum voltage of Q1 to account for transients and ringing. Because the average diode current is the output current, the diode's package must be capable of dissipating up to $P_{D1} = I_{OUT} \times V_D$.

6 TPS40211 Design Guide

6.1 Current Sense and Overcurrent

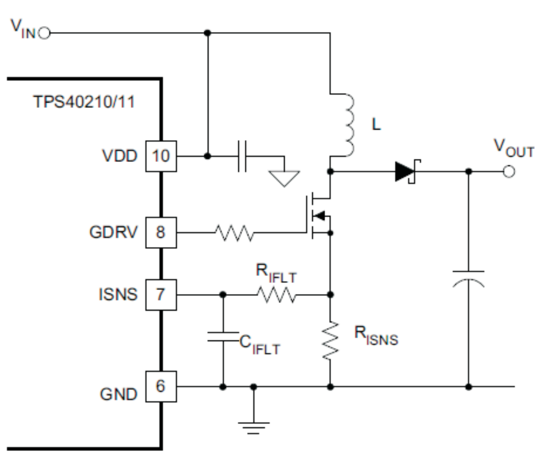


Figure 8. Current Sense Circuit

The TPS40210 and TPS40211 are current mode controllers and use resistors in series with the source terminal power FET to sense current for both the current mode control and the overcurrent protection. The device enters a current limit state, if the voltage on the ISNS pin exceeds the current limit threshold voltage V_{ISNS} from the electrical specifications table. When this happens, the controller discharges the SS capacitor through a relatively high impedance, and then attempt to restart. The load current over-current threshold is set by proper choice of R_{ISNS}. If the converter is operated in discontinuous mode, the current sense resistor is given by

$$R_{ISNS} = \frac{fs \times L1 \times V_{ISNS}}{\sqrt{2 \times L1 \times fs \times 1.5 I_{OUT} \times (V_{OUT} + V_D - V_{INmin})}} \tag{14}$$

If the converter is operated in continuous conduction mode, the current sense resistor is given by

$$R_{ISNS} = \frac{V_{ISNS}}{\frac{I_{OUT}}{1 - D_{max}} + \frac{D_{max} \times V_{INmin}}{2 \times fs \times L1}} \tag{15}$$

6.2 Soft-Start Capacitor

Because VDD > 8 V, the soft-start capacitor is given by

$$C_{SS} = 20 \times T_{SS} \times 10^{-6} \tag{16}$$

where T_{SS} is a timing of soft-start.

6.3 Setting the Oscillator Frequency

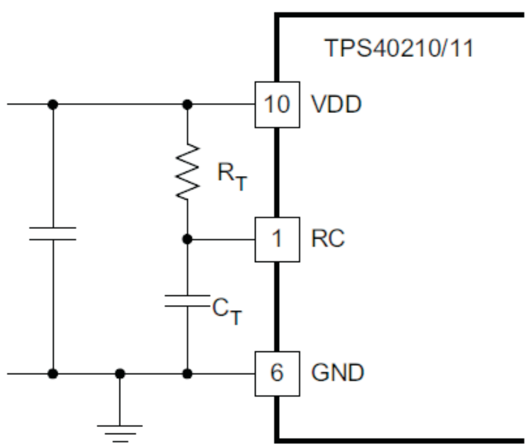


Figure 9. Oscillator Components

The oscillator frequency is determined by a resistor and capacitor connected to the RC pin of the TPS40211. The capacitor is charged to a level of approximately $V_{VDD}/20$ by current flowing through the resistor and is then discharged by a transistor internal to the TPS40211. The required resistor for a given oscillator frequency is given by

$$R_T = \frac{1}{5.8 \times 10^{-8} \times fs \times C_T + 8 \times 10^{-10} \times fs^2 + 1.4 \times 10^{-7} \times fs - 1.5 \times 10^{-4} + 1.7 \times 10^{-6} \times C_T - 4 \times 10^{-9} \times C_T^2} \tag{17}$$

Where:

- R_T is the timing resistance in kΩ
- fs is the switching frequency in kHz
- C_T is the timing capacitance in pF

For most applications, a capacitor is in the range of 68 pF to 120 pF gives the best results. Resistor values must be limited to between 100 kΩ and 1 MΩ as well.

6.4 Current Feedback Resistor

The only difference between the TPS40210 and the TPS40211 is the reference voltage that the error amplifier uses to regulate the output voltage. The TPS40211 uses a 260-mV reference and is intended for applications where the output is actually a current instead of a regulated voltage. The current in the LED string is set by the choice of the resistor R_{FB} as shown in the following equation:

$$R_{FB} = \frac{V_{FB}}{I_{OUT}} \tag{18}$$

Where V_{FB} is the reference voltage for the TPS40211 in V (0.26 V typ)

7 Design Example

Design Specifications

1. Allowed maximum input voltage (V):	V_{INmax} = 12 V
2. Allowed minimum input voltage (V):	V_{INmin} = 5 V
3. LED series number:	S_{LED} = 3
4. LED voltage drop:	V_{LED} = 3.2 V
5. Output current:	I_{OUT} = 700 mA
6. Converter efficiency:	η = 90%
7. Switching frequency:	fs = 560 kHz

Design Results

A. SEPIC Converter Design Guide

Inductance of L1 and L2:	L1 = L2 > L_{CCM}	LCCM = 7.772 µH
		L1 = L2 = 10 µH selected
Output capacitance:		C_{OUT} = 20.902 µF
		C3 + C21 = 20 µF selected
Input capacitance:		C_{IN} = 2.09 µF
		C4 = 2.2 µF selected
Coupling capacitance:		ΔC_P = 0.38 µF
		C7 = 0.47 µF selected
MOSFET current and voltage stress		
Voltage stress:		V_{Q1rate} = 21.6 V
Current stress:		V_{Q1peak} = 2.9 AV
		Selected 60-V, 6.5-A MOSFET
Diode current and voltage stress		
Voltage stress:		V_{D1rate} = 21.6 V
Current stress:		V_{D1peak} = 2.9 AV
		Selected 40-V, 4-A diode
B. TPS40211 Design Guide		
Current sense resistance:		$R_{ISNSCCM}$ = 0.044 Ω
		R1 = 50 mΩ selected
Soft-Start capacitance (F):		$C_{SS} = 1 \times 10^{-7}$
		C9 = 0.1 nF selected

Current FB resistance:	R_{FB} = 0.371 Ω
	R6=R7= 0.7 Ω selected
R-C Oscillator	
Resistance R_T (kΩ)	R_T = 402.411
	R3 = 402 kΩ selected
Capacitance C_T (pF):	C_{TT} = 68
	C8 = 68 pF selected

8 Test Data

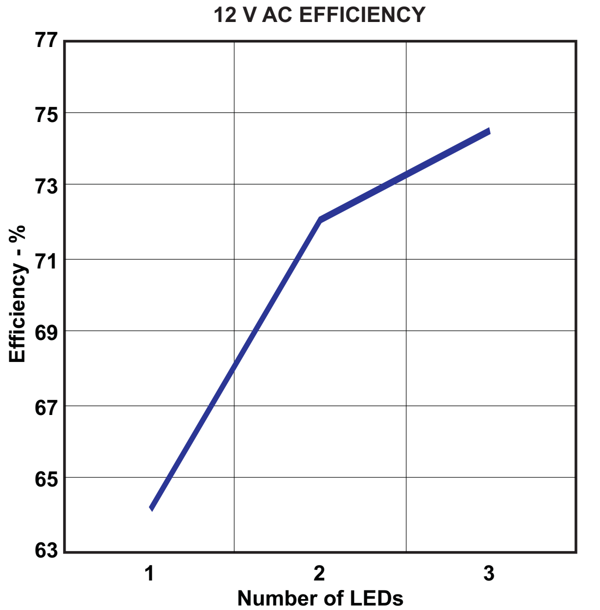


Figure 10. 12-Vac Input Efficiency With ac Transformer

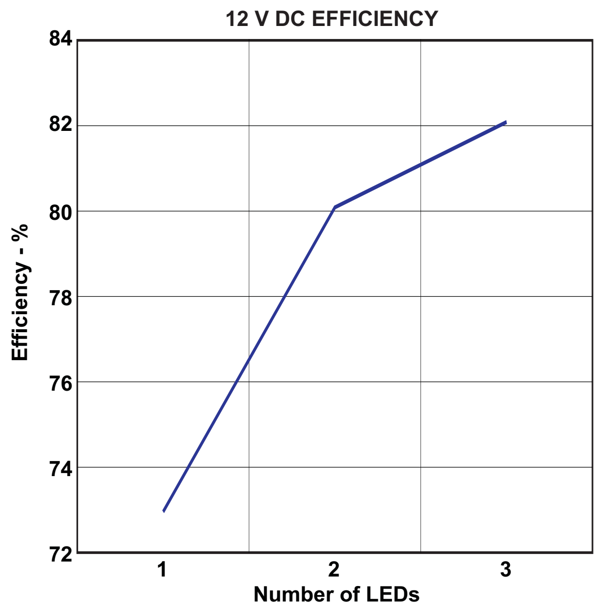


Figure 11. 12-Vdc Input Efficiency

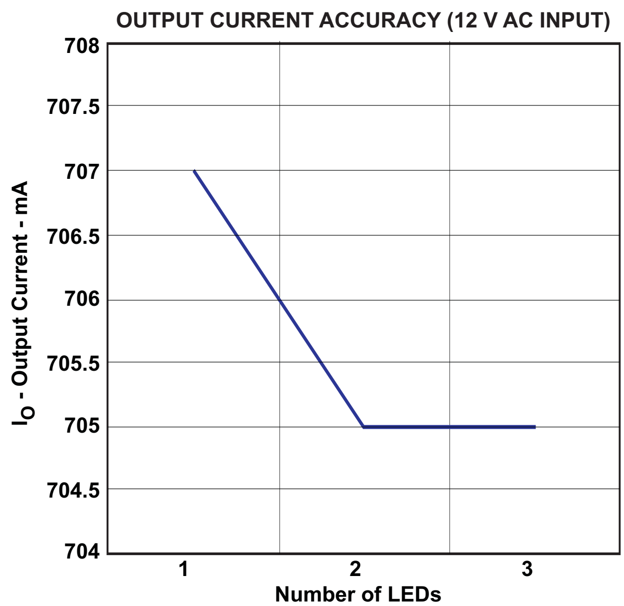


Figure 12. Output Current Accuracy Less Than 1%

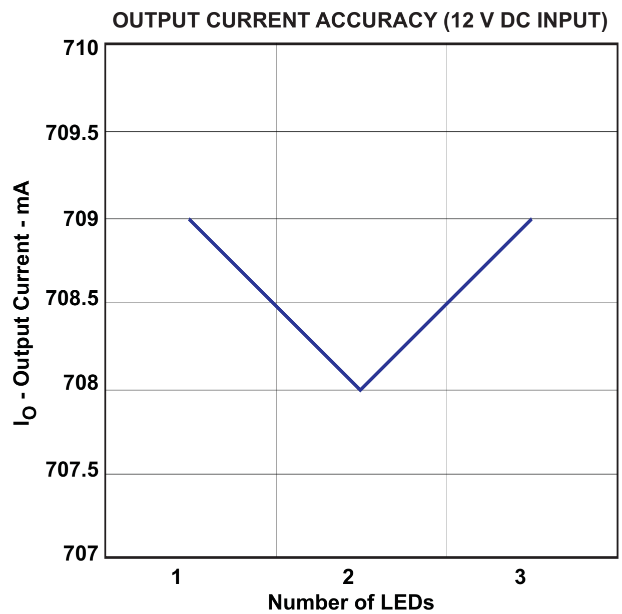


Figure 13. Output Current Accuracy Less Than 1%

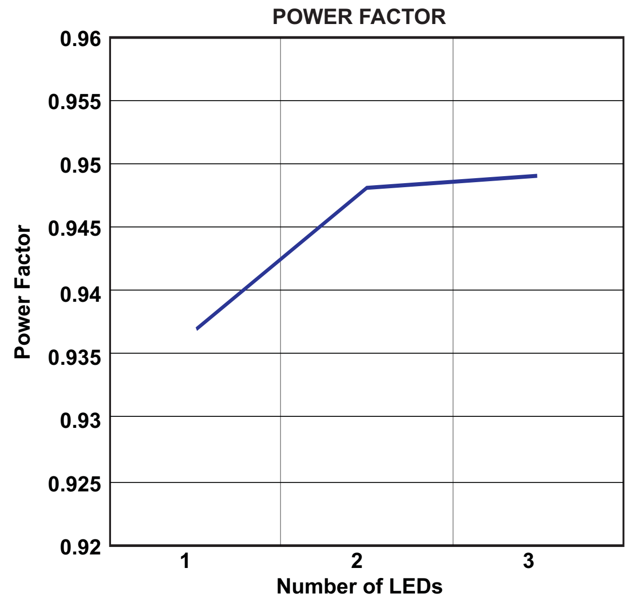


Figure 14. 12-Vac Input With ac Transformer

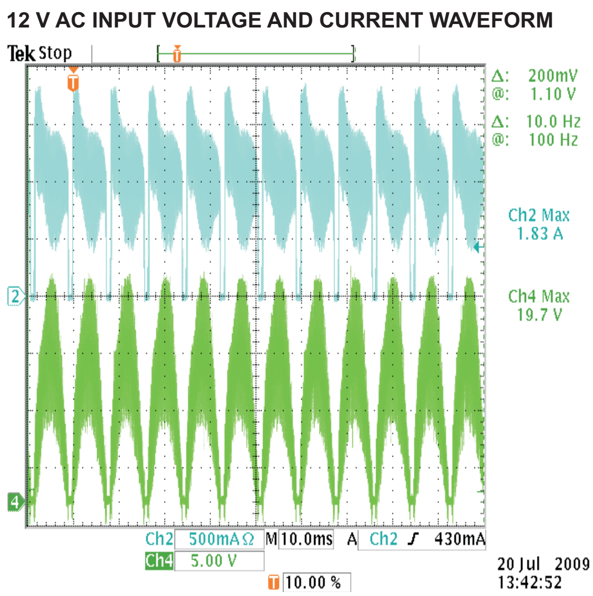


Figure 15. CH2: Input Current, CH4: Input Voltage After Rectifier

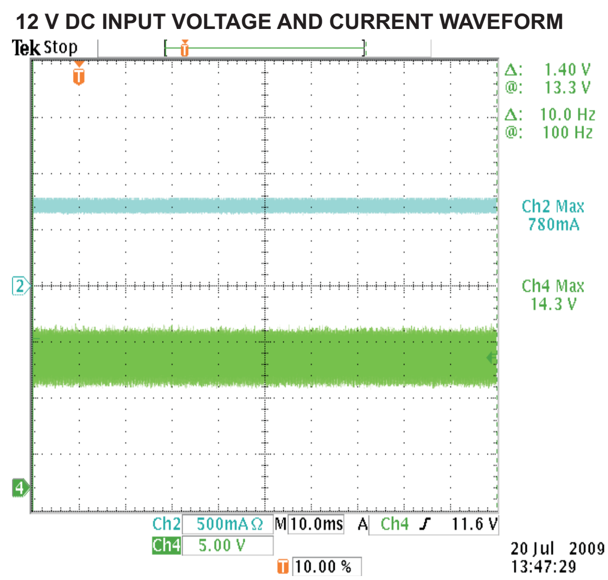


Figure 16. CH2: Output Current, CH4: Input Voltage After Rectifier

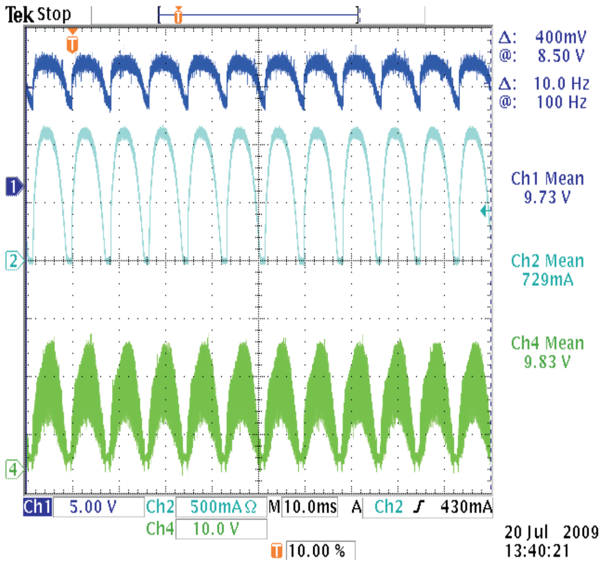


Figure 17. CH1: Output Voltage, CH2: Output Current, CH4: Input Voltage After Rectifier

12 V DC OUTPUT VOLTAGE AND CURRENT WAVEFORM

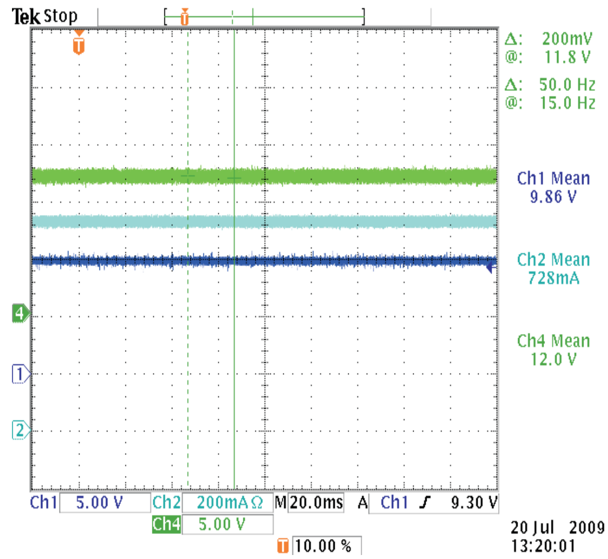


Figure 18. CH1: Output Voltage, CH2: Output Current, CH4: Input Voltage After Rectifier

12 V AC INPUT Q1 DRAIN TO SOURCE VOLTAGE STRESS

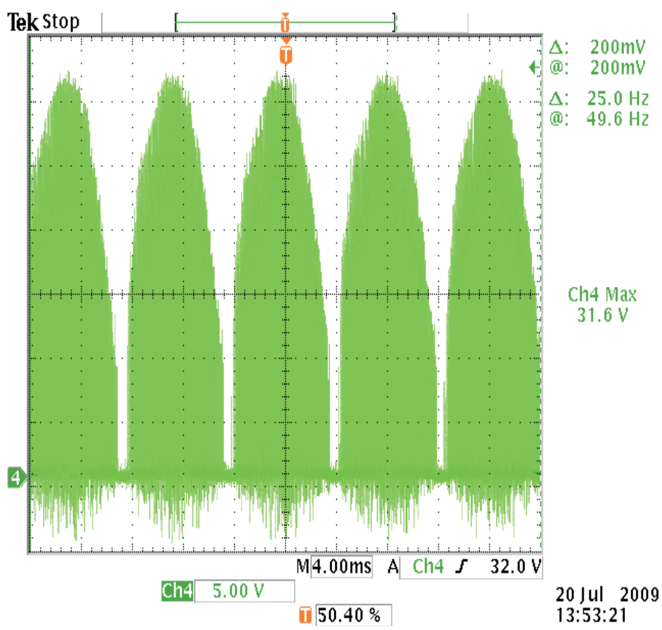


Figure 19. CH4: Q1 V_{DS}

9 EVM Assembly Drawing and Layout

A two-layer, printed-circuit board (PCB) was designed using the top and bottom layers. The dimensions of PCB are 12mm × 10mm, and the other PCB diameter is 21mm, with a design goal of maintaining all components to be a height less than 12mm that is measured from the surface of the top layer. Figure 20 shows the top-side driver photo placement for the EVM, and all other layers are also shown in Figure 21 through Figure 25, respectively.

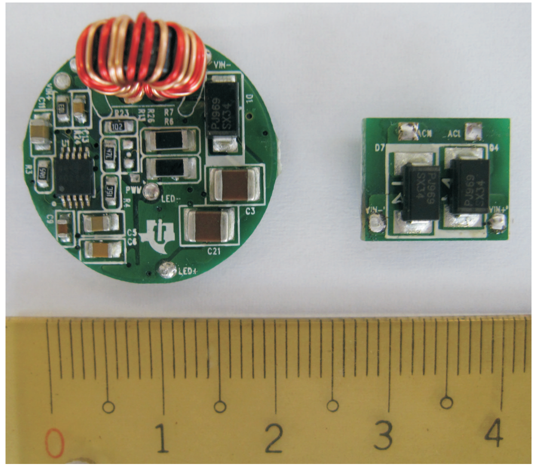


Figure 20. MR-16 Driver Photo on Top Side

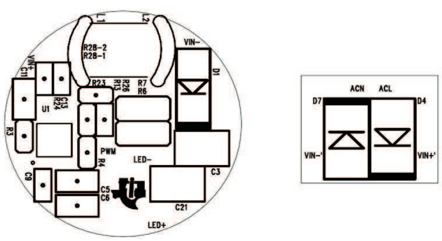


Figure 21. Top-Side Component Assembly

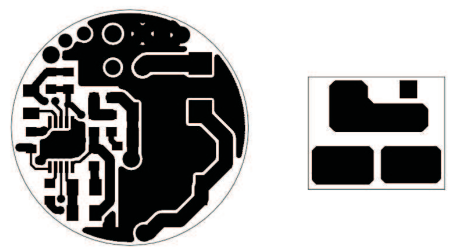


Figure 22. Top-Side Signal Trace Layer

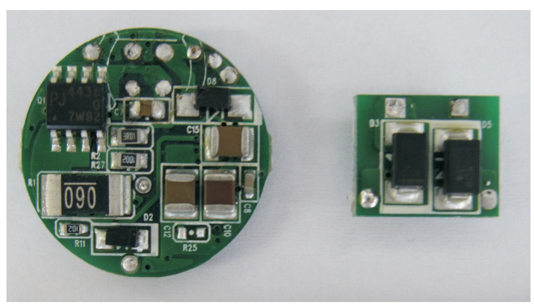


Figure 23. MR-16 Driver Photo on Bottom Side

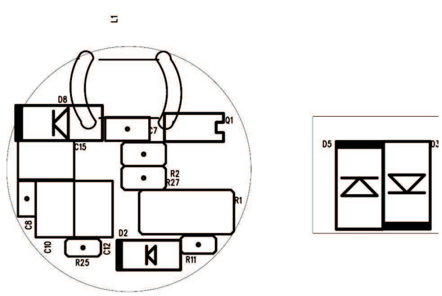


Figure 24. Bottom-Side Component Assembly

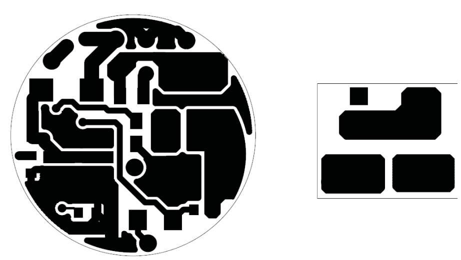


Figure 25. Bottom-Side Signal Trace Layer

10 Bill of Materials

Table 1 lists the EVM components as configured corresponding to the schematic shown in Figure 2. Part types and manufacturers can be modified according to specific application requirements.

Table 1. Bill of Materials

Count	Ref Des	Description	Part Number	MFR
1	D1	SHTKY, 40V, 3A, SMA	SX34	PANJIT
1	L1 WITH L2	10.7UH, 2A	APS-12706-NL	AXIS
1	Q1	60V 6.5A 30MOHM, SO-8	PJ4438	PANJIT
2	C21,C3	10UF, 25V 1210 X7R		PANASONIC
1	R1	70M, 2512	WSL2512R0150FEA	YAGEO
2	R6, R7	0.7 , 1206	WSL2512R3600FEA	YAGEO
1	C7	0.47UF 25V 0805		PANASONIC
1	U1	TPS40211	TPS40211	TI
3	C10, C12, C15	10UF, 25V 1210 X7R		PANASONIC
1	C11	1UF, 25V, 0805 X7R		PANASONIC
1	D8	SHTKY, 40V, 1A, SOD-123	SS1040FL	PANJIT
1	R3	402K, 0603		YAGEO
1	C8	68P, 25V 0603 NPO		PANASONIC
1	C9	0.1U, 16V 0603 X7R		PANASONIC
1	R13	30.1K, 1% 0603		YAGEO
1	R4	14.3K, 1% 0603		YAGEO
1	C5	1UF, 25V X7R, 0805		PANASONIC
1	C6	0.022UF, 50V X7R, 0805		PANASONIC
1	R23	1K, 0603		YAGEO
4	D3,D4,D5,D7	SHTKY, 40V, 3A, SMA	SX34	PANJIT
1	L3	10UH, 2A	APS-11644-NL	AXIS
1	R11	1K, 0603		YAGEO
1	C13	2200PF, 16V 0603 X7R		PANASONIC
1	D2	ZENER 15V SOD-123	MMSZ5245A	PANJIT
1	R24	10K, 0603		YAGEO
1	R2	3.01, 0805		YAGEO
1	R27	10K , 0805		YAGEO

11 References

1. *Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range* design note DN-48 (SLUA158)
2. *Designing DC/DC Converters Based on SEPIC Topology*, Texas Instruments Analog Applications Journal, 4Q 2008
3. *TPS40211, 4.5-V to 52-V Input Current Mode Boost Controller* data sheet (SLUS772)

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