Setting the SVS Voltage Monitor Threshold

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ABSTRACT

The power supply voltage for powering a microprocessor's core must fall within a given accuracy range in order for the processor to perform to its best specifications. If this input supply voltage should drift near to the operational boundary then the microprocessor will want to gracefully shutdown, or reset, before presumably losing its data or miss-performing in some way. The following application report will discuss this issue in some detail in order to arrive at a reasonable approach for adjusting the SENSE, or reset, threshold of the Supply Voltage Supervisor (SVS) circuit to assure that the microprocessor is reset properly, while accounting for the various inaccuracies of the voltage monitor/supervisor system. In most of these systems it is the lower voltage boundary that is of paramount concern and therefore this report will only focus on the lower trip threshold only.

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1 Introduction

As the system operating voltage ranges narrow the demand for tighter power supply accuracies and SVS accuracies increases. For tightest accuracies it will likely be necessary to search for a completely integrated solution containing both an accurately trimmed power supply output voltage as well as a factory trimmed SVS threshold. One such example would be the TPS75005 dual output LDO with integrated SVS intended for applications requiring load currents of less than 500 mA. Theoretically the potential accuracy of an internally trimmed sense threshold is better than one using an external resistor divider to divide down the monitored voltage to a common reference voltage, but this is not always true in practice.

More typically the power supply and SVS selection will need careful consideration if system operating voltage boundaries are to be respected. This is an iterative process where the power supply voltage accuracy, the SVS reference requirement and resistor tolerances are progressively narrowed till the total system accuracy fits within the prescribed operating window. There must not be any overlaps between the supply accuracy boundary with the SVS accuracy boundary so as to prevent false resets from non-failing supply voltages.

2 Typical SVS Application

Figure 1 shows a typical SVS configuration where Voltage Supervisor A monitors the 3.3-V supply voltage to the DSP's VI/O input and Voltage Supervisor B monitors the 1.8-V supply voltage to the DSP core at the V_{CORE} input. In this configuration if the 3.3-V supply rail should fail by falling below the SENSE threshold of the TPS3808G33 this will issue a master reset (MR/) to the TPS3808G18 which would then RESET the DSP. Or if the 1.8-V_{CORE} voltage should fail by falling below the SENSE threshold of the TPS3808G18 then this would cause a RESET to be issued directly to the DSP.

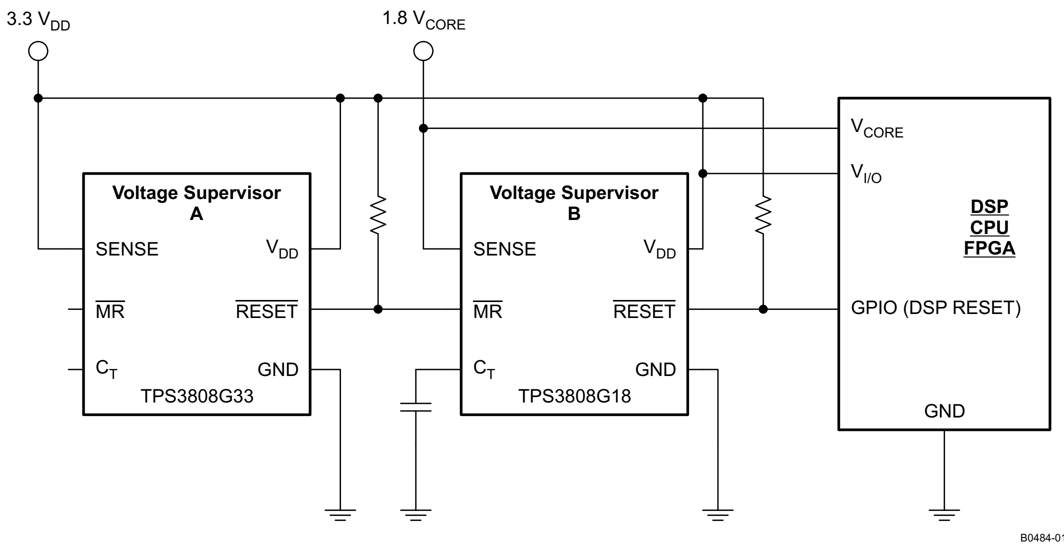

Figure 1. Typical Supply Voltage Supervisor Configuration for Protecting a DSP

The choice to employ the TPS3808 as the supervisor to monitor the respective supply voltages would have been made after finding that the DSP requires voltages be maintained within say a ±10% window of the nominal supply rails, that is, 3.3-V I/O, nominal, and 1.8 V_{CORE}, nominal, to maintain operation. Each power supply and supervisor will be selected so as to dis-allow the supply voltage from falling outside this ±10% boundary window of operation. Each power supply will have its own specified accuracy and each supervisor will monitor that supply voltage around a SENSE threshold also having its own accuracy. By example, Figure 2 illustrates the situation just described where the nominal 1.8-V supply is monitored by the TPS3808G18. The selected 1.8-V power supply might typically have been selected for its ±5% accuracy, as shown, enabling the use of the TPS3808 in such a way that the supervisor trip threshold can dependably respond within the window required by the DSP. The nominal trip, or reset, threshold for the TPS3808G18 is 1.67 V ±1.5% according to its data sheet, detected at the SENSE input. This means that this threshold relative to the nominal, 1.8-V supply voltage can be calculated to fall between –5.83% to –8.61% of that voltage as shown and which is well within the required window of the system operating voltage range.

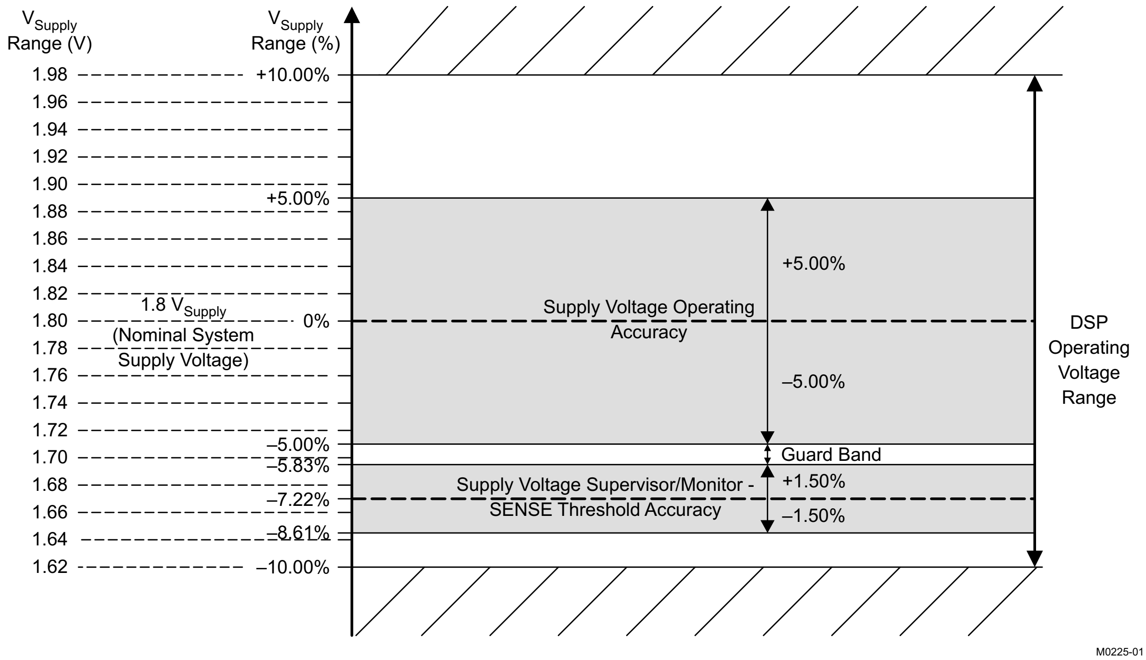

Figure 2. Illustration Depicting a Supply Voltage, the Relative SVS Reset Threshold, and Respective Accuracies Within the Required System Operating Voltage Range

3 Setting the SVS Sense Threshold when High Accuracy is Needed

The approach here is to first select a known power supply with a specified accuracy and then decide to use an adjustable SVS SENSE threshold adjusted to the average between the lowest possible supply voltage and the minimum allowable system (CPU) voltage. Of course, custom trimmed settings of fixed SVS SENSE voltage thresholds are available for a price depending on the business case. The lowest specified supply voltage, $V_{ss(min)}$, is calculated from the nominal supply voltage, $V_{ss(nom)}$, and the known supply voltage accuracy as a percent, $\%V_{Vss}$, in Equation 1.

$$V_{ss(min)} = V_{ss(nom)} \times (1 - \%V_{Vss}/100) \quad (1)$$

The desired nominal SVS SENSE threshold, $V_{th(nom)}$, is calculated in Equation 2:

$$V_{th(nom)} = [V_{ss(min)} + Vcpu_{(min)}] / 2 \quad (2)$$

where $V_{cpu(min)}$ is the minimum allowable system operating voltage.

The type of highly accurate SVS circuit required here is depicted in Figure 3 where a single channel of the quad TPS38600 is shown monitoring a 1.8-V core voltage to the system CPU. The TPS38600 was chosen for it 1% reference accuracy.

Note that in Figure 3 the SVS SENSE threshold, V_{th}, is determined by the resistor divider, R1 and R2, and is defined as the failing V_{CORE} voltage that will cause the SVS to reset.

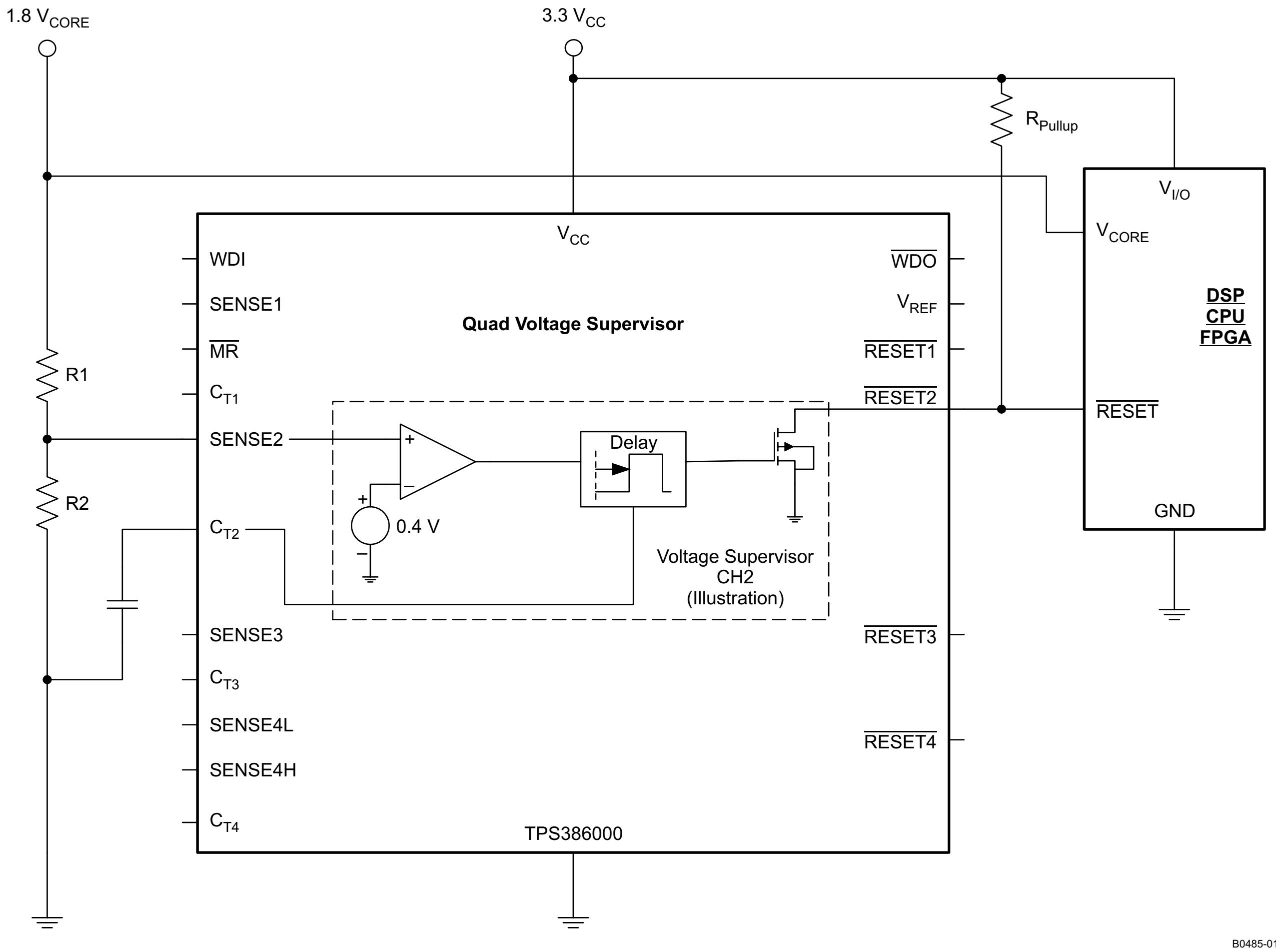

Figure 3. SVS Circuit for Monitoring a Supply Voltage for a CPU Core

The resistor values to make the nominal SVS SENSE threshold are calculated using Equation 3:

$$R2 = V_{ref} \times R1 / (V_{th(nom)} - V_{ref}) \tag{3}$$

where V_{ref} is the nominal reference voltage of the SVS device.

The accuracy of the SVS SENSE threshold is considered to be the combined result of errors contributed by the SVS reference voltage accuracy (read inaccuracy), the tolerance of the divider resistors[1] and the error by the leakage current[2] into the SENSE pin of the of the SVS. These errors are depicted by the series of equations: Equation 4, Equation 5, and Equation 6:

$$V'_{th} = V_{th(nom)} \pm V_{error(\%ref)} = [V_{ref} \times (1 + R1/R2)] \times [1 \pm (\%Ref / 100)] \tag{4}$$

Where $V_{error(\%ref)}$ is the SVS SENSE voltage threshold error due to the reference error, where %Ref is the reference error as a percent.

$$V''_{th} = V'_{th} \pm V_{error(\%RTOL)} = V'_{th} \times [1 \pm (2 \times (\%R_{TOL}/100) \times (1 - V_{th(nom)} / V_{ref}))] \tag{5}$$

Where $V_{error(\%RTOL)}$ is the voltage error introduced to $V_{th(nom)}$ due to the tolerances of the resistor divider resistors, R1 and R2.

$$V'''_{th} = V''_{th} \pm V_{error(Isense)} = V'_{th} \pm I_{SENSE} \times R1 \tag{6}$$

Where I_{SENSE} is the leakage current into the SENSE pin of the SVS device and $V_{error(Isense)}$ is the threshold voltage error caused by I_{SENSE}.

Of course the tally of all these errors is best kept ordered in a spread sheet.

Setting the SVS Sense Threshold when High Accuracy is Needed

3.1 Example

Use Figure 3 as the starting point to design an SVS circuit and power supply for a CPU requiring a 1.8-V ±5% supply for its core voltage rail. We will also decide right off to use a 1.8-V power supply whose accuracy is ±2% sense, knowing already that this is typical of what goes for a standard industry best.

Key Specifications:
CPU Core Operating Range: 1.8 V ±5% (1.71V to 1.89V)
Supply Voltage, V_{ss}: 1.8 V ±2%
Resistors R1 and R2 can have tolerances of 0.1% but 1% is preferred.
TPS38600 Product Characteristics over temp:
Vref = 0.4 V ±1%, I_{SENSE} = ±25nAmps

From Equation 1 calculate the minimum specified supply voltage, $V_{ss(min)}$, and then use Equation 2 to calculate the nominal SVS SENSE threshold, $V_{th(nom)}$.

$V_{ss(min)} = V_{ss(nom)} \times (1 - \%VVss/100) = 1.8\text{ V} \times (1 – 2\%/100) = 1.764\text{ V}$

$V_{th(nom)} = (V_{ss(min)} + Vcpu_{(min)}) / 2 = (1.764\text{ V} + 1.71\text{ V}) / 2 = 1.737\text{ V}$

Note here that the max/min SVS SENSE threshold is required to fit within an accuracy window between the CPU minimum voltage and the minimum supply voltage, Vss(min) : 1.71 V to 1.764 V

Figure 4 illustrates the nominal supply voltage, the SVS reset, and the respective accuracy ranges that allow the CPU specifications to be met by the following calculations.

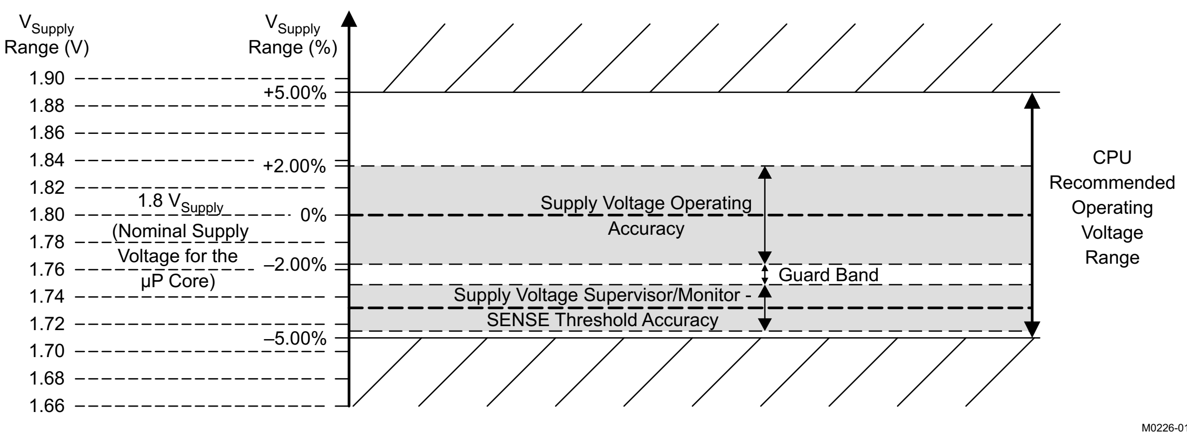

Figure 4. Illustration of a Nominal 1.8-V Power Supply, the Relative SVS Reset Threshold, and the Respective Accuracy Windows Necessary To Meet A "±5%" CPU Operating Range Requirement

Assume that R1 = 500 kΩ and calculate R2 using Equation 3.

$R2 = V_{ref} \times R1 / (V_{th(nom)} – V_{ref}) = 0.4\text{ V} \times 500\text{ k} / (1.737\text{ V} – 0.4\text{ V}) = 426894\ \Omega$

Calculate the threshold accuracy error range due to the reference accuracy using Equation 4 as follows:

$V'_{th} = V_{th(nom)} \pm V_{error(\%ref)} = [V_{ref} \times (1 + R1/R2)] \times (1 \pm (\%Ref / 100))$
$= [0.4\text{ V} \times (1 + 500\text{ k}\Omega/426894\ \Omega)] \times (1 \pm (1\% / 100)) = 1.7196\text{ V (min) to } 1.75626\text{ V (max)}$

Calculate the added threshold accuracy error, added to the range of V'_{th} above, that is due to the resistor tolerances using Equation 5:

$V''_{th} = V'_{th} \pm V_{error(\%RTOL)} = V'_{th} \times (1 \pm (2 \times (\%R_{TOL}/100) \times (1 – V_{th(nom)} / V_{ref}))$
$= 1.7196\text{ V} \times (1-(2\times 0.001 \times (1 – 1.737\text{ V}/.4\text{ V})) \text{ to } 1.75626\text{ V} \times (1+(2 \times 0.001 \times (1 – 1.737\text{ V}/0.4\text{ V}))$
$= 1.7178\text{ V (min) to } 1.5626\text{ V (max)}$

Finally, calculate the total added threshold accuracy error including that from the leakage sense current, I_{SENSE}, using Equation 6:

$V'''_{th} = V''_{th} \pm V_{error(Isense)} = V''_{th} \pm I_{SENSE} \times R1 = 1.7178\text{ V} – 25\text{ nA} \times 500\text{ k}\Omega \text{ to } 1.5626\text{ V} + 25\text{ nA} \times 500\text{ k}\Omega$
$= 1.7078\text{ V (min) to } 1.7663\text{ V (max)}$

Notice that the lowest possible SVS SENSE threshold, 1.7078 V, is actually lower than the minimum specified operating voltage of the CPU, which is 1.71 V, and the upper accuracy limit of the same threshold is above the minimum good supply voltage, $V_{ss(min)}$ of 1.764 V. **This circuit does not meet requirements.** In this case, to meet the CPU specifications all that is needed is to reduce the R1 and R2 resistances (in the same ratio) so as to reduce the error contribution due to the I_{SENSE} leakage error current.

Reduce R1 to 250 kΩ and then, by Equation 3, R2 to 2134447 Ω. Now recalculate the error using **Equation 8** to find that this new SVS SENSE threshold accuracy window does fall within the required range:

V'''_{th} = 1.7115 V (min) to 1.7625 V (max)

This is illustrated in Figure 4.

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