Functional Safety Information

LP2951-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LP2951-Q1 (WSON-8 and SOIC-8 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

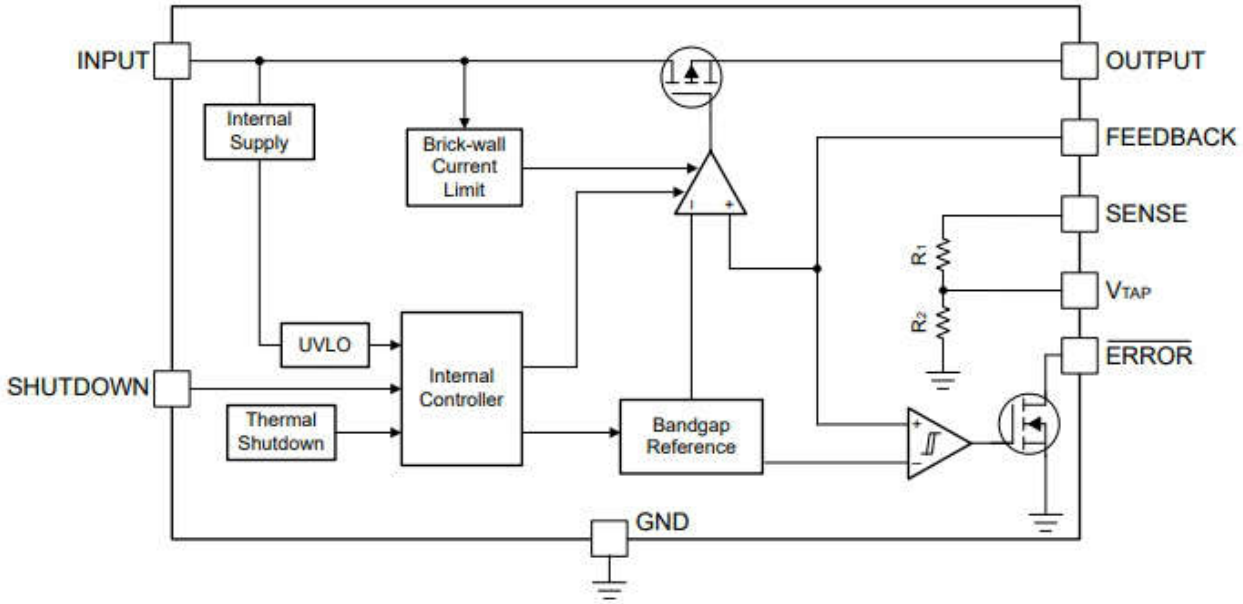

Figure 1-1. Functional Block Diagram

LP2951-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 WSON-8 Package

This section provides functional safety failure in time (FIT) rates for the WSON-8 package of the LP2951-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	4
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOIC-8 Package

This section provides functional safety failure in time (FIT) rates for the SOIC-8 package of the LP2951-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	6
Package FIT rate	8

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LP2951-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No OUTPUT (output low)	30
OUTPUT high (following input)	20
OUTPUT not in specification	35
Short circuit (any two pins)	5
ERROR - false trip or failure to trip	5
SHUTDOWN fails	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LP2951-Q1 (WSON-8 and SOIC-8 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to input (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device must maintain the same pin configuration as with the WSON-8 and SOIC-8 packages.
- Device operates with an input voltage less than 30V and an output current less than 100mA.
- Device operates across virtual junction temperatures ranging from -40°C to 125°C.
- Device operates according to the recommended operating conditions and does not exceed the absolute maximum ratings.

4.1 WSON-8 Package

Figure 4-1 shows the LP2951-Q1 pin diagram for the WSON-8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LP2951-Q1 data sheet.

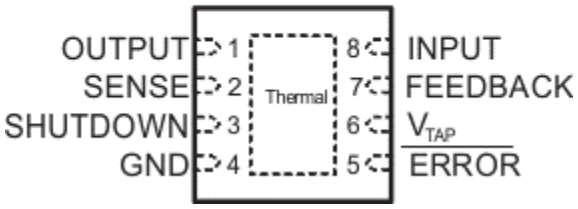

Figure 4-1. Pin Diagram (WSON-8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	Regulation is not possible, the device operates at current limit. The device can cycle in an out of thermal shutdown.	B
Sense	2	Regulation is not possible, the device operates at current limit.	B
Shutdown	3	Proper regulation without the ability to shutdown device.	B
GND	4	No effect. Normal operation.	D
Error	5	Proper regulation without the ability to error output.	B
V_{TAP}	6	(Fixed) Output is pulled low, leading to undesired fixed output.	B
		(Adjustable) No effect. Normal operation.	D
Feedback	7	(Fixed) Output is pulled low, leading to undesired fixed output.	B
		(Adjustable) Output is pulled low, leading to an undesired output.	B
Input	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	The device output is disconnected from the load.	B
Sense	2	Unable to sense the output, leading to an unknown output state	B
Shutdown	3	The device is in the low-power shutdown state if left floating.	B
GND	4	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
Error	5	No effect. Normal operation.	D
V_{TAP}	6	(Fixed) There is no connection to feedback, leading to an undesired output.	B
		(Adjustable) No effect. Normal operation.	D
Feedback	7	There is no connection to feedback, leading to an undesired output.	B
		(Adjustable) Input to device error amplifier is left floating, leading to an undesired output.	B
Input	8	Power is not supplied to the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
Output	1	Sense	No effect. Normal operation.	D
Sense	2	Shutdown	Output pin is driven low.	B
Shutdown	3	GND	Proper regulation without the ability to shutdown device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
Error	5	V_{TAP}	The device state is unknown, leading to an inaccurate reading of the output.	B
V_{TAP}	6	Feedback	(Fixed) No effect. Normal operation.	D
			(Adjustable) Unable to use external feedback resistors, leading to an undesired output.	B
Feedback	7	Input	Device can become damaged as feedback is low voltage and input is high voltage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Input

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	Regulation is not possible, leading to an undesired output state.	B
Sense	2	Device can become damaged.	A
Shutdown	3	The device is in the shutdown state.	B
GND	4	Power is not supplied to the device. System performance depends on upstream current limiting.	B
Error	5	The device state is unknown leading to an inaccurate reading of the output.	B
V_{TAP}	6	Device can become damaged.	A
Feedback	7	Device can become damaged.	A
Input	8	No effect. Normal operation.	D

4.2 SOIC-8 Package

Figure 4-2 shows the LP2951-Q1 pin diagram for the SOIC-8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LP2951-Q1 data sheet.

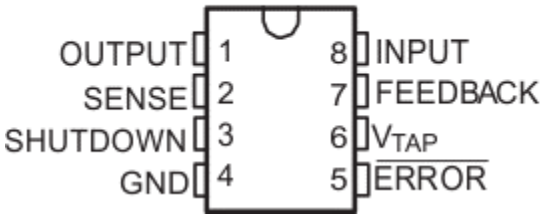

Figure 4-2. Pin Diagram (SOIC-8 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	Regulation is not possible, the device operates at current limit. The device can cycle in an out of thermal shutdown.	B
Sense	2	Regulation is not possible, the device operates at current limit.	B
Shutdown	3	Output is off when pin is pulled low.	B
GND	4	No effect. Normal operation.	D
Error	5	Proper regulation without the ability to error output.	B
V_{TAP}	6	(Fixed) Output is pulled low, leading to undesired fixed output.	B
		(Adjustable) No effect. Normal operation.	D
Feedback	7	(Fixed) Output is pulled low, leading to undesired fixed output.	B
		(Adjustable) Output is pulled low, leading to an undesired output.	B
Input	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	The device output is disconnected from the load.	B
Sense	2	Unable to sense the output, leading to an unknown output state	B
Shutdown	3	The device is in the low-power shutdown state if left floating.	B
GND	4	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
Error	5	No effect. Normal operation.	D
V_{TAP}	6	(Fixed) There is no connection to feedback, leading to an undesired output.	B
		(Adjustable) No effect. Normal operation.	D
Feedback	7	(Fixed) There is no connection to feedback, leading to an undesired output.	B
		(Adjustable) Input to device error amplifier is left floating, leading to an undesired output.	B
Input	8	Power is not supplied to the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
Output	1	Sense	No effect. Normal operation.	D
Sense	2	Shutdown	Output pin is driven low.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
Shutdown	3	GND	Proper regulation without the ability to shutdown device.	B
Error	5	V_{TAP}	The device state is unknown, leading to an inaccurate reading of the output.	B
V_{TAP}	6	Feedback	(Fixed) No effect. Normal operation.	D
			(Adjustable) Unable to use external feedback resistors, leading to an undesired output.	B
Feedback	7	Input	Device can become damaged as feedback is low voltage and input is high voltage.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to Input

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
Output	1	Regulation is not possible, leading to an undesired output state.	B
Sense	2	Device can become damaged.	A
Shutdown	3	The device is in the shutdown state.	B
GND	4	Power is not supplied to the device. System performance depends on upstream current limiting.	B
Error	5	The device state is unknown leading to an inaccurate reading of the output.	B
V_{TAP}	6	Device can become damaged.	A
Feedback	7	Device can become damaged.	A
Input	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2024) to Revision B (November 2024) **Page**

- Updated functional block diagram..... 2
- Updated Component Failure Rate Tables 2-1, 2-2, 2-3, and 2-4..... 3
- Updated information for the WSON-8 and SOIC-8 packages in the Pin FMA Tables 4-2, 4-3, 4-4, 4-5, 4-6, 4-7, 4-8, and 4-9..... 4

Changes from Revision * (January 2020) to Revision A (August 2024) **Page**

- Added component failure rates per Siemens Norm SN 29500-2..... 2

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