Functional Safety Information

TPS7B4254-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS7B4254-Q1 (SO PowerPAD package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

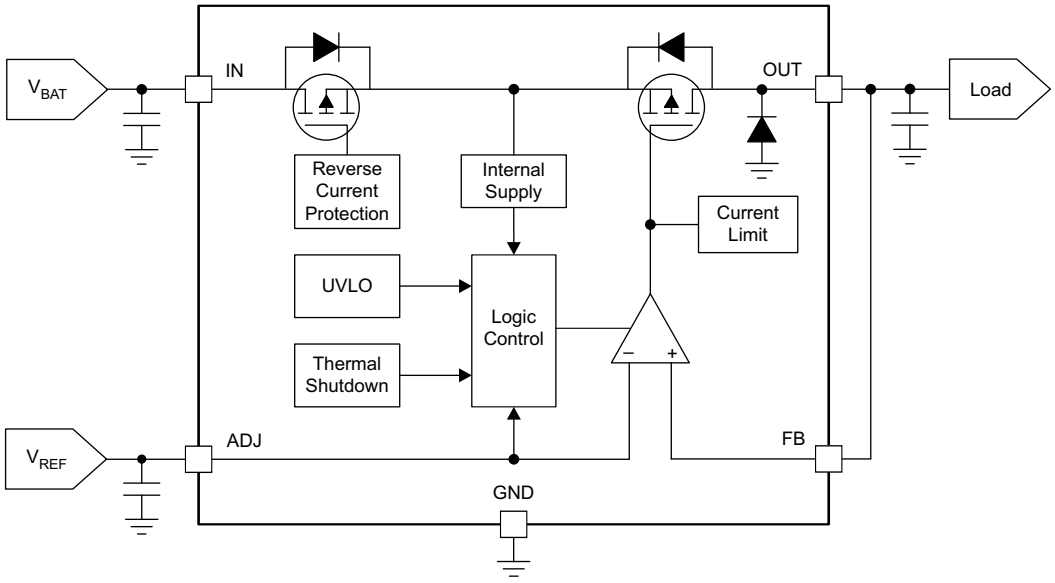

Figure 1-1. Functional Block Diagram

The TPS7B4254-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B4254-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	5
Package FIT rate	12

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator < 1 Watt	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B4254-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	50
Output high (following input)	5
Output functional not in specification	45

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B4254-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{IN} (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7B4254-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4254-Q1 data sheet.

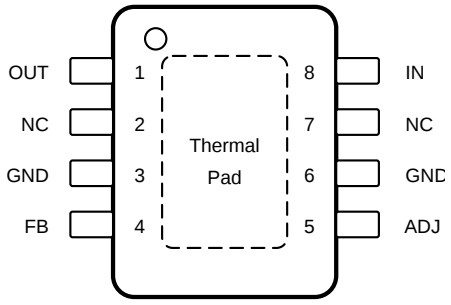

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output voltage is near or at ground. The device is in current limit and can cycle in and out of thermal shutdown depending on power dissipation.	B
NC	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
FB	4	V_{OUT} is equal to V_{IN} minus dropout because the pass transistor is driven to the rail.	B
ADJ	5	The low-dropout regulator (LDO) does not start up because ADJ is grounded.	B
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	The output is near or at ground.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The load is longer regulated.	B
NC	2	No effect. Normal operation.	D
GND	3	The device is operational as long as pin 6 (GND) is still connected, but with degraded performance.	B
FB	4	The output becomes unregulated.	B
ADJ	5	The device state is unknown. The device is either on and regulated to an unknown voltage, or the device is off.	B
GND	6	The device is operational as long as pin 6 (GND) is still connected, but with degraded performance.	B
NC	7	No effect. Normal operation.	D
IN	8	The device does not operate or start up.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	No effect. Normal operation.	D
NC	2	GND (pin 3)	No effect. Normal operation.	D
GND	3	FB (pin 4)	The output is equal to the input minus dropout because the pass transistor is driven to the rail.	B
ADJ	5	GND (pin 6)	The LDO does not start up because ADJ is grounded.	B
GND	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	IN (pin 8)	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	No output regulation. The output voltage is the same as the input voltage.	B
NC	2	No effect. Normal operation.	D
GND	3	No output regulation. The output is near or at ground.	B
FB	4	FB is damaged if V_{IN} exceeds the FB maximum rated voltage. Otherwise, the pass transistor is off and the output is low.	A/B
ADJ	5	The LDO starts up or shuts down when V_{IN} is above the ADJ threshold. The output equals the input minus the dropout voltage.	B
GND	6	No output regulation. The output is near or at ground.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2020) to Revision A (April 2023)	Page
• Added *Pin Failure Mode Analysis (Pin FMA)* section	5

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