

# Using the TPS6290x in an Inverting Buck – Boost Topology



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## ABSTRACT

The need to generate negative rail for electronic designs is a challenge engineers face everyday. This application note illustrates how to design an inverting buck – boost using the highly efficient TPS62903. This application report details component selection criteria and equations, so that designers can appropriately scale the solution to their own requirements. The document also includes a design example along with captured waveforms. The same design is applicable to the TPS62901, TPS62902, and TPS6290x-Q1.

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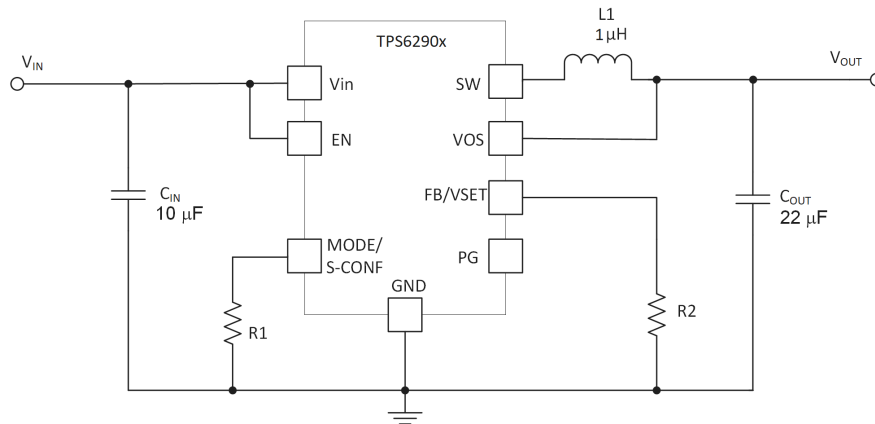
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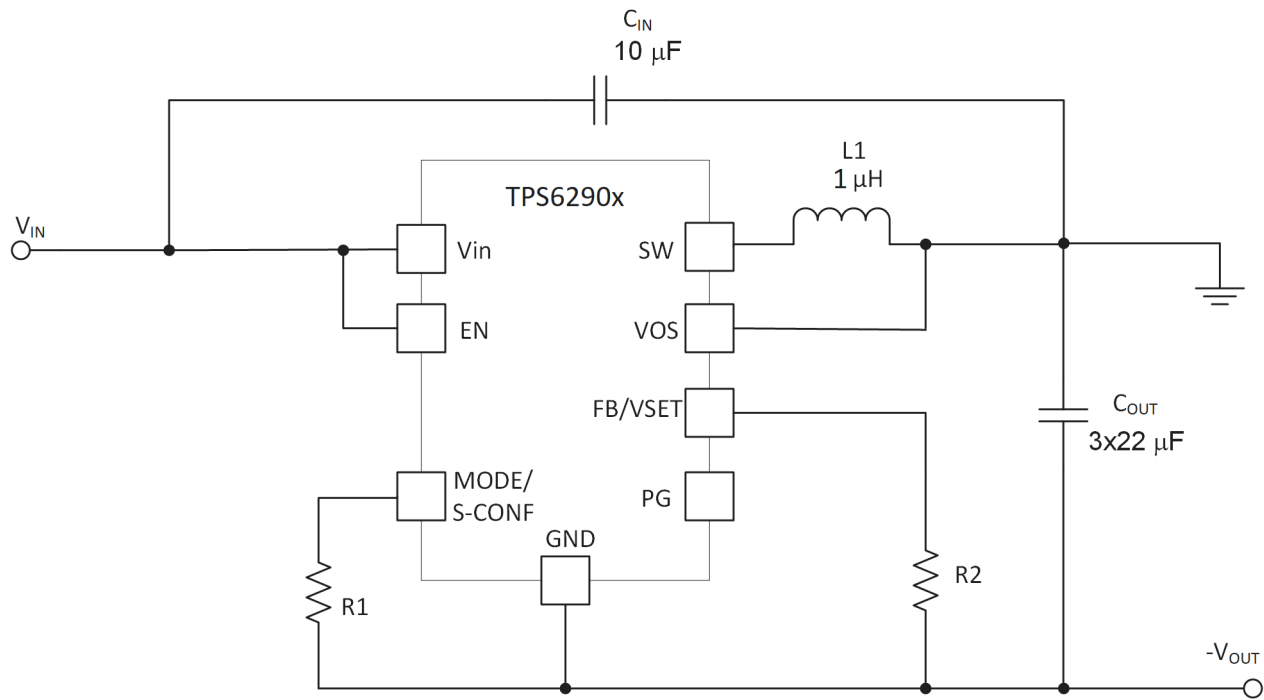
## 1 Inverting Buck – Boost Topology

### 1.1 Concept

The inverting buck – boost topology is very similar to the buck topology. In the buck configuration shown in [Figure 1-1](#), the positive connection ( $V_{OUT}$ ) is connected to the inductor and the return is connected to the integrated circuit (IC) ground. However, in the inverting buck – boost configuration shown in [Figure 1-2](#), the IC ground is used as the negative output voltage (labeled as  $-V_{OUT}$ ). What used to be the positive output in buck configuration is used as the ground (GND). This inverting buck – boost topology allows the output voltage to be inverted and is always lower than the ground.

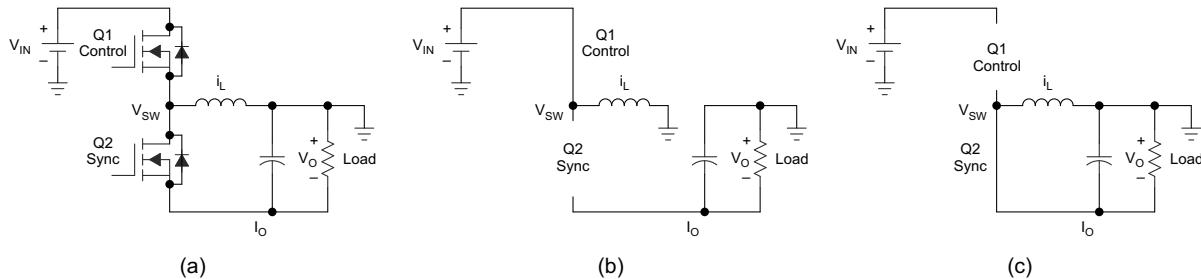


**Figure 1-1. TPS62903 Buck Topology**



**Figure 1-2. TPS62903 Inverting Buck – Boost Topology**

The circuit operation is different in the inverting buck - boost topology than in the buck topology. [Figure 1-3](#) (a) illustrates that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in [Figure 1-3](#) (b), the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in [Figure 1-3](#) (c), the inductor provides current to the load and the output capacitor. These changes affect many parameters described in the upcoming sections.



**Figure 1-3. Inverting Buck – Boost Configuration**

## 1.2 Output Current Calculations

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck - boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output capacitor and the load (see [Figure 1-3](#)). Knowing that the off time is 1-D of the switching period, then the average inductor current is:

$$I_{L(avg)} = \frac{I_{OUT}}{1-D} \quad (1)$$

The duty cycle for the typical buck converter is simply  $V_{OUT} / V_{IN}$  but the duty cycle for an inverting buck - boost converter becomes:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} \quad (2)$$

The efficiency term in [Equation 2](#) adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. Where  $V_{OUT}$  is a negative value. The peak to peak inductor ripple current is calculated as:

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} \quad (3)$$

Where,

$\Delta I_L$  (A): Peak to peak inductor ripple current

D: Duty cycle

$\eta$ : Efficiency

$f_s$  (MHz): Switching frequency

L ( $\mu$ H): Inductance

$V_{IN}$  (V): Input voltage with respect to ground, instead of IC ground or  $-V_{OUT}$ .

Finally, the maximum inductor current becomes:

$$I_{L(max)} = I_{L(avg)} + \frac{\Delta I_L}{2} \quad (4)$$

For an output voltage of  $-3.3\text{ V}$ ,  $2.5\text{ MHz}$  switching frequency,  $1\mu\text{H}$  inductor, and an input voltage of  $12\text{ V}$ , the following calculations produce the maximum allowable output current that can be delivered based on the  $4\text{ A}$  minimum current limit ( $I_{LIM}$ ) of TPS62903. The efficiency term is estimated at  $70\%$ .

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} = \frac{-3.3}{-3.3 - 12} \times \frac{1}{0.7} = 0.308 \quad (5)$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} = \frac{12 \times 0.308}{2.5\text{MHz} \times 1\mu\text{H}} = 1.4784\text{ A} \quad (6)$$

Rearranging Equation 4 and setting  $I_{L(max)}$  equal to the minimum value of  $I_{LIM}$ , as specified in the data sheet, gives:

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 4 - \frac{1.4784}{2} = 3.26\text{ A} \quad (7)$$

This result is then used in Equation 1 to calculate the maximum achievable output current:

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 3.26 \times (1 - 0.308) = 2.25\text{ A} \quad (8)$$

Increasing the inductance and/or input voltage allows higher output current in the inverting buck - boost topology. The maximum output current for the TPS62903 in the inverting buck - boost topology are frequently lower than  $3\text{ A}$  due to the fact that the average inductor current is higher than that of a typical buck. The output current for three output voltages ( $-1.2\text{ V}$ ,  $-3.3\text{ V}$ ,  $-5\text{ V}$ ) with two inductors ( $1\mu\text{H}$ ,  $2.2\mu\text{H}$ ) at  $FSW=2.5\text{ MHz}$  and different input voltages are displayed in Figure 1-4.

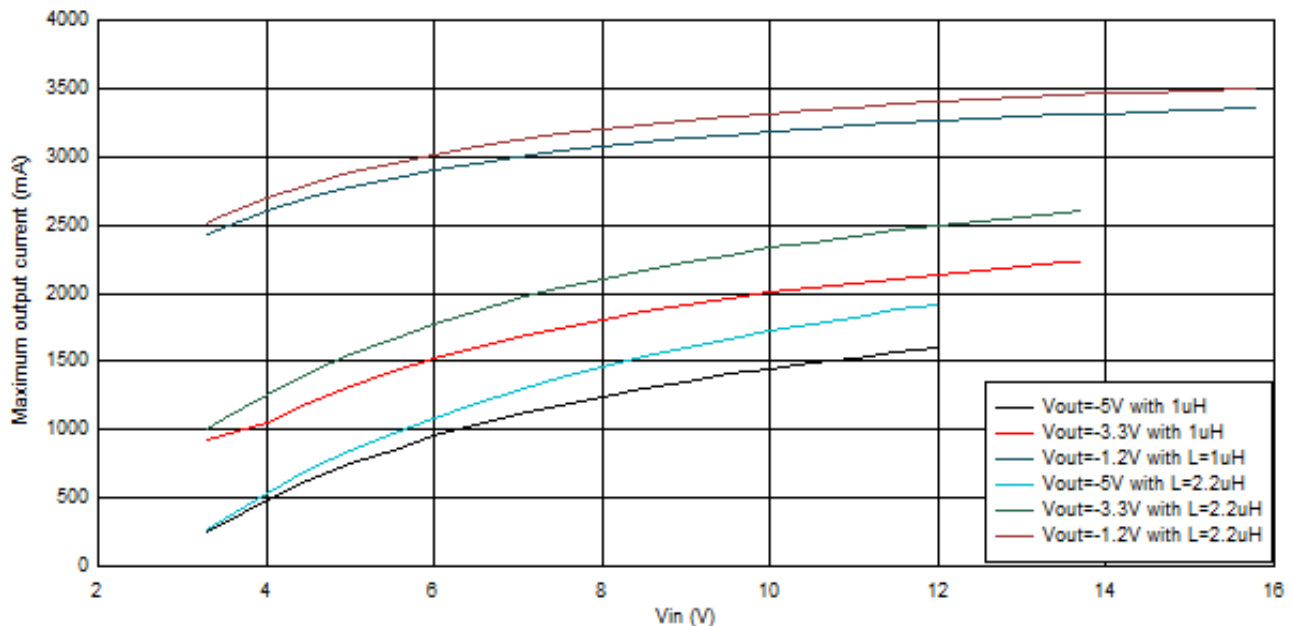


Figure 1-4. Maximum Output Current vs. Input Voltage

### 1.3 $V_{IN}$ and $V_{OUT}$ Range

The input voltage that can be applied to an inverting buck - boost converter is less than the input voltage that can be applied to the same buck converter. This is because the ground pin of the IC is connected to the negative output voltage. Therefore, the input voltage across the device is  $V_{IN}$  to  $-V_{OUT}$ , not  $V_{IN}$  to ground. Thus, the input voltage range of the TPS62903 is  $3\text{ V}$  to  $17\text{ V} + V_{OUT}$ , where  $V_{OUT}$  is a negative value. The minimum input voltage stays the same at  $3\text{ V}$  because the device will not turn on during startup when the negative  $V_{OUT}$  is not present.

The output voltage range is the same as when configured as a buck converter, but negative. The TPS62903 output voltage for the inverting buck - boost topology should be set between  $-0.6\text{ V}$  to  $-5.5\text{ V}$  for external divider and  $-0.4\text{ V}$  to  $-5.5\text{ V}$  for internal divider (VSET). It can be set the same way as in the buck configuration, with two resistors connected to the FB pin or VSET configuration. Due to the increased noise of the inverting buck - boost topology, for a more robust design, recommend use internal feedback (VSET) or use smaller value resistors than are used for the buck configuration.

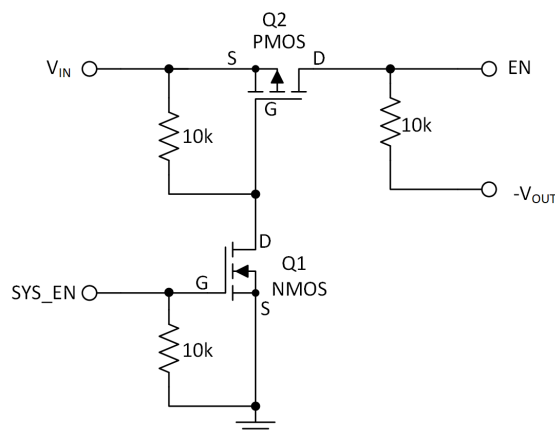
## 2 Digital Pin Configurations

### 2.1 Enable Pin

The TPS62903 is enabled once the voltage at the EN pin trips its threshold and the input voltage is above the UVLO threshold. The device stops operation once the voltage on the EN pin falls below its threshold or the input voltage falls below UVLO threshold.

Because  $-V_{OUT}$  is the IC ground in this configuration, the EN pin must be referenced to  $-V_{OUT}$  instead of ground. In the buck configuration,  $1\text{ V}$  is considered to turn on and less than  $0.9\text{ V}$  is considered to turn off. In the inverting buck-boost configuration, however, the  $-V_{OUT}$  voltage is the reference; therefore, the high threshold is  $1\text{ V} + V_{OUT}$  and the low threshold is  $0.9\text{ V} + V_{OUT}$ . Where  $V_{OUT}$  is a negative value. For example, if  $V_{OUT} = -3.3\text{ V}$ , the  $V_{EN}$  is considered at a high level for voltages above  $-2.3\text{ V}$  and at a low level for voltages below  $-2.4\text{ V}$ .

This behavior can cause difficulties enabling or disabling the device, since in some applications, the IC providing the EN signal might not be able to produce negative voltages. The level shifter circuit shown in [Figure 2-1](#) alleviates any difficulties associated with the offset EN threshold voltages by eliminating the need for negative EN signals.



$-V_{OUT}$  is the negative output voltage of the inverting buck-boost converter

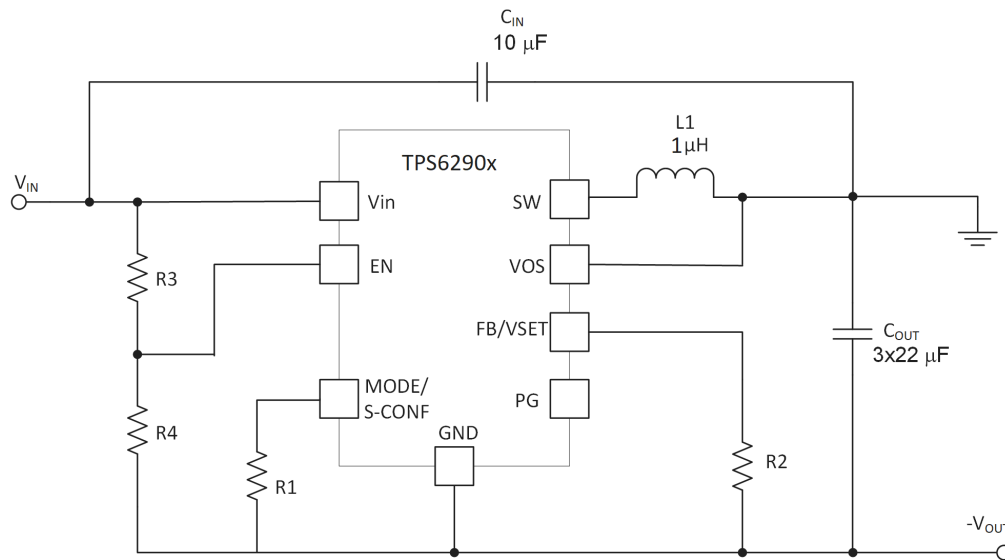
**Figure 2-1. EN Pin Level Shifter**

The positive signal (SYS\_EN) that originally drove EN is instead tied to the gate of Q1. When Q1 is off, Q2 sees  $0\text{ V}$  across its  $V_{GS}$ , and also remains off. In this state, the EN pin sees  $-3.3\text{ V}$  for  $-V_{OUT} = -3.3\text{ V}$  which is below the low level threshold and it disables the device.

When SYS\_EN provides enough positive voltage to turn Q1 on ( $V_{GS}$  threshold as specified in the MOSFET data sheet), the gate of Q2 sees ground through Q1. This drives the  $V_{GS}$  of Q2 negative and turns Q2 on. Now,  $V_{IN}$  ties to EN through Q2 and the pin is above the high level threshold, turning the device on. Be careful to ensure that the  $V_{GD}$  and  $V_{GS}$  of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint might result in MOSFET damage. A small size complementary N and P Channel 60V (D-S) MOSFET Si1029X from Vishay can be used in the design.

If the system enabling and disabling of the TPS62903 is not desired, the EN pin can be directly connected to  $V_{IN}$  or a voltage divider connected to  $V_{IN}$ . We strongly recommend to add a voltage divider placeholder (R3/R4) between  $V_{IN}$  and EN pin which is shown in [Figure 2-2](#). Recommend  $R3:R4 \geq 2:1$  ratio to ensure  $V_{IN} > 2.95\text{ V}$  UVLO before  $EN > 1\text{ V}$  which the internal circuit of device is ready before EN is fully enabled. UVLO and EN falling thresholds become relative to  $-V_{OUT}$  instead of GND. For example, UVLO falling =  $2.75\text{ V} + V_{OUT}$  and EN

falling =  $0.9\text{ V} + V_{\text{OUT}}$ . Where  $V_{\text{OUT}}$  is a negative value. Customer can scale the voltage divider R3/R4 ratio based on the real application. This is a reliable solution to eliminate any start up and shut down related issues.

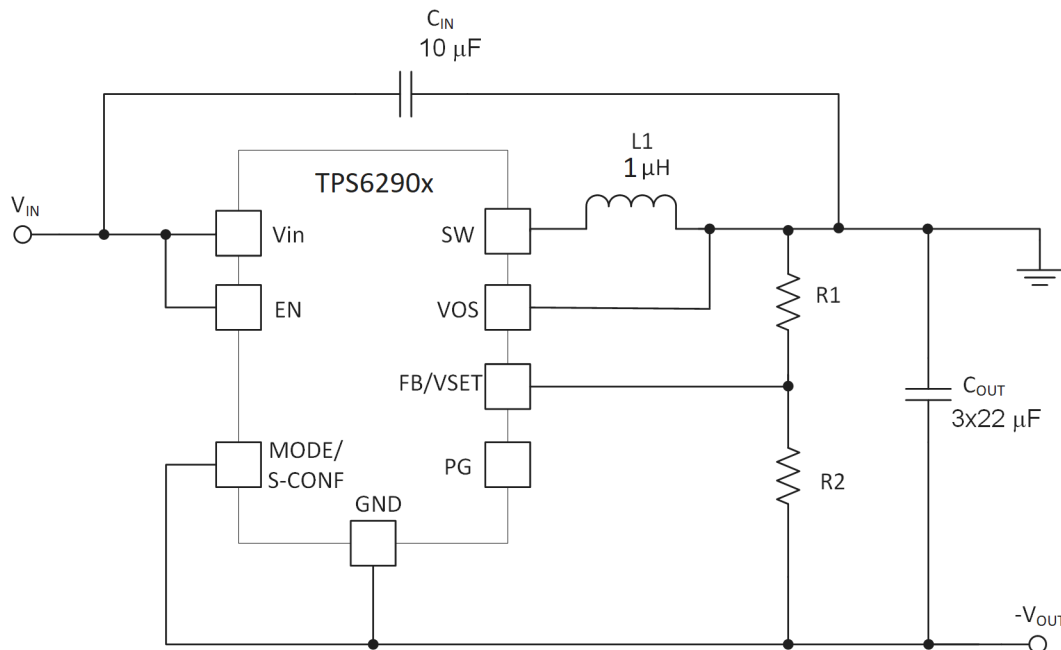


**Figure 2-2. EN Pin with Voltage Divider**

## 2.2 MODE/S-CONF Pin

TPS62903 has a MODE/S-CONF pin which can be used to customize the device behavior. Refer to schematic in [Figure 2-2](#) and [Figure 2-3](#)

- Selects device configuration (switching frequency, internal or external feedback, output discharge, Forced PWM and Auto PFM/PWM mode) by connecting a single resistor between this pin and  $-V_{OUT}$  (IC GND pin) or connecting directly to  $V_{IN}$  or  $-V_{OUT}$  (IC GND pin).
  - A 2.5 MHz switching frequency setting is recommended for inverting buck-boost application due to lower inductor ripple current. The design example selects MODE/S-CONF resistor as 26.1 k which configures internal feedback, 2.5 MHz switching frequency, Auto PFM/PWM with AEE and output discharge enabled.
  - Note that the maximum output current will be reduced while using 1uH inductor and 1MHz switching frequency. 2.2uH or larger inductance is strongly recommended for 1 MHz switching frequency configuration, otherwise special care has to be taken to make sure the half ripple current doesn't trip the negative current limit under no load condition.
- Dynamic MODE option is an advance feature which allows MODE/S-CONF pin to actively switch between Forced PWM and Auto PFM/PWM during operation. This feature provides user with the option of controlling when/if the device enters power save mode (DCM). In the inverting buck-boost topology,  $V_{IN}$  is HIGH and  $-V_{OUT}$  is LOW, but this is only possible by driving the MODE/S-CONF pin between  $V_{IN}$  and  $-V_{OUT}$ . This can be done with the same type of circuit used to drive the EN pin HIGH and LOW as shown in [Figure 2-1](#)
- The external feedback configuration shown in [Figure 2-3](#), where the MODE/S-CONF pin can be tied to  $-V_{OUT}$  directly to configure as 2.5 MHz switching frequency, Auto PFM/PWM with AEE and output discharge enabled.

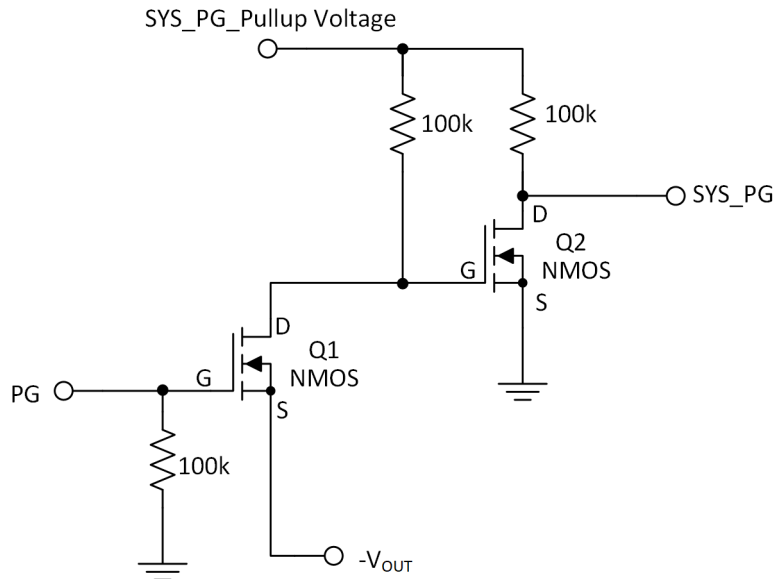


**Figure 2-3. External Feedback with 2.5 MHz Switching Frequency and Auto PFM/PWM**

## 2.3 Power Good Pin

The TPS62903 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because  $-V_{OUT}$  is the IC ground in this configuration, the PG pin is referenced to  $-V_{OUT}$  instead of ground, which means that the TPS62903 pulls PG to  $-V_{OUT}$  when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin might not be able to withstand negative voltages. The level shifter circuit shown in Figure 2-4 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it can be left floating without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 17 V above the negative output voltage (IC ground).



**Figure 2-4. PG Pin Level Shifter**

Connecting TPS62903 PG pin to the gate of Q1, when the PG pin is pulled low ( $-V_{OUT}$ ), Q1 is off and Q2 is on because its  $V_{GS}$  sees SYS\_PG\_Pullup Voltage. SYS\_PG is then pulled to ground.

When PG pin is pulled high (GND), the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS\_PG is then pulled up to its pullup voltage. Note that the pullup voltage must be at an appropriate logic level for the circuitry connected to the SYS\_PG. A small size dual N Channel 20V(D-S) MOSFET Si1902CDL from Vishay can be used in the design.



### 3 Design Considerations

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See [Selecting L and Cout for Stability](#) for a discussion of stability.

#### 3.1 Input Capacitor Selection

An input capacitor,  $C_{IN}$ , is required to provide a local bypass for the input voltage source. A low ESR input capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 10- $\mu$ F or 22- $\mu$ F ceramic capacitor is recommended from  $V_{IN}$  to ground. The  $C_{IN}$  capacitor value can be increased without any limitation for better input voltage filtering.

For the inverting buck – boost configuration of the TPS62903, it is not recommended to install a capacitor from  $V_{IN}$  to  $-V_{OUT}$ . Such a capacitor, if installed, provides an AC path from  $V_{IN}$  to  $-V_{OUT}$ . When  $V_{IN}$  is applied to the circuit, this  $dV/dt$  across a capacitor from  $V_{IN}$  to  $-V_{OUT}$  creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS62903 and is not recommended. Therefore, a capacitor from  $V_{IN}$  to  $-V_{OUT}$  is not needed or recommended. If such a capacitor ( $C_{BYP}$ ) is present, then a Schottky diode should be installed on the output per [Figure 3-1](#). Startup testing should be conducted to ensure that the SW and VOS pins are not driven more than 0.3 V below IC ground when  $V_{IN}$  is applied.

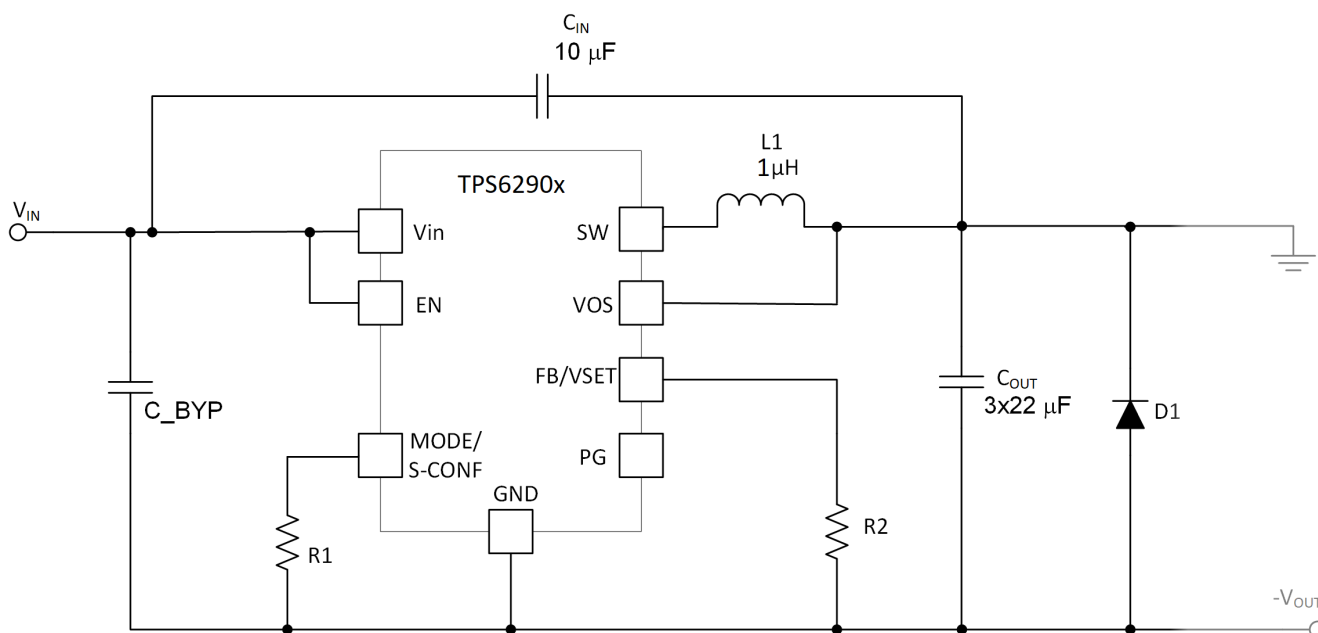


Figure 3-1. If Installing  $C_{BYP}$ , Installing Schottky D1 is Required

#### 3.2 Output Inductor Selection

When selecting the inductor value for the inverting buck - boost topology, the equations provided in the [Output Current Calculations](#) section should be used instead of the ones provided in the data sheet. These equations help to select the right inductance by designing for a maximum inductor current ( $I_{L(max)}$ ) for a given inductance.  $I_{L(max)}$  should be kept below the minimum current limit value of TPS62903 (4A) for a reliable design. The recommended output inductor for TPS62903 is in the range of 1 $\mu$ H to 2.2 $\mu$ H. See [Selecting L and Cout for Stability](#) for the stability impact of the inductor selection.

### 3.3 Stability Limits and Output Capacitor Selection

The switch node, inductor current, and the output voltage ripple during steady state are signals that need to be checked first for the stability of the system. Oscillations on the output voltage and the inductor current, and jitter on the switch node are good indicators of the instability of the system. Load transient response is another good test for stability, as described in the [Simplifying Stability Checks](#) application note.

The inverting buck - boost topology contains a right-half plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. As a result the phase margin of the closed loop response is reduced which leading to potential instability and poor load transient response. [Equation 9](#) estimates the frequency of the RHP zero. Where  $V_{OUT}$  is a negative value.

$$f_{(RHP)} = \frac{-(1-D)^2 \times V_{OUT}}{(D \times L \times I_{OUT} \times 2 \times \pi)} \quad (9)$$

It is recommended to keep the loop crossover frequency to 1/10th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. A larger output capacitance is recommended for low input (< 12 V) voltage designs. [How to Measure the Control Loop of DCS-Control™ Devices](#) explains how to measure the control loop of a DCS-Control™ device.

The recommended minimum output capacitance for TPS62903 inverting buck-boost topology is 3x22 μF. The effective output capacitance post DC-bias derating is approximately 30 μF. The output capacitance used with inverting buck-boost is larger than would normally be used with a buck due to its right-half plane zero. More output capacitance pushes the crossover frequency of the control loop down to frequency lower enough so that the right-half plane zero is sufficiently higher for stability.

## 4 Typical Performance and Waveforms

The application circuit shown in [Figure 4-1](#) is used to generate the data for typical performance. There is no reference design for the TPS6290x using inverting buck-boost topology. The buck EVM was modified to be used as an inverting buck-boost. See [How to Modify a Step-Down Converter to Inverting Buck-Boost Topology](#) for details. L1 is a 1µH inductor XGL4020-102MEC from Coilcraft. The output capacitors used 3x22 µF, 10 V, 0805, X7S ceramic capacitor. The input capacitor used 10 µF, 25V, 1206, X7R. Unless otherwise specified,  $V_{IN} = 12\text{ V}$  and  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 0\text{ A}$  to 2.1A, 2.5 MHz, Auto PFM/PWM, internal feedback (VSET).

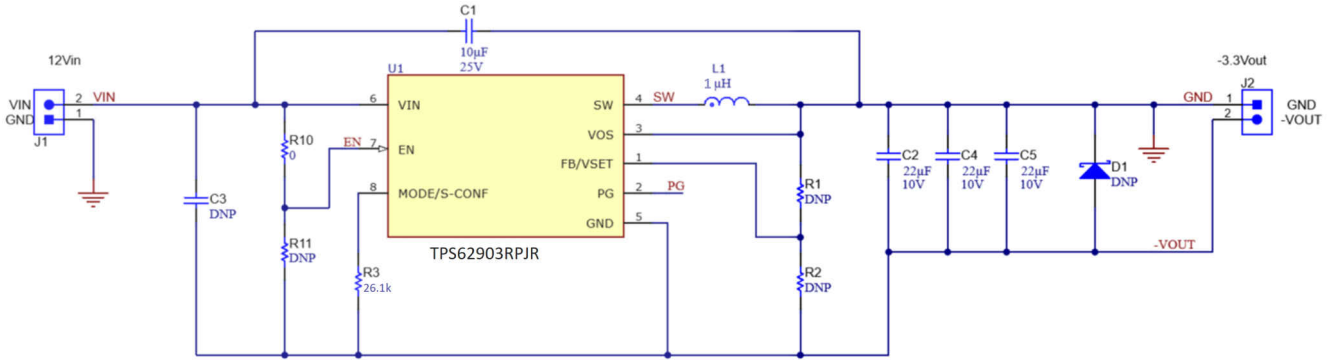


Figure 4-1. Schematic of Tested Circuit

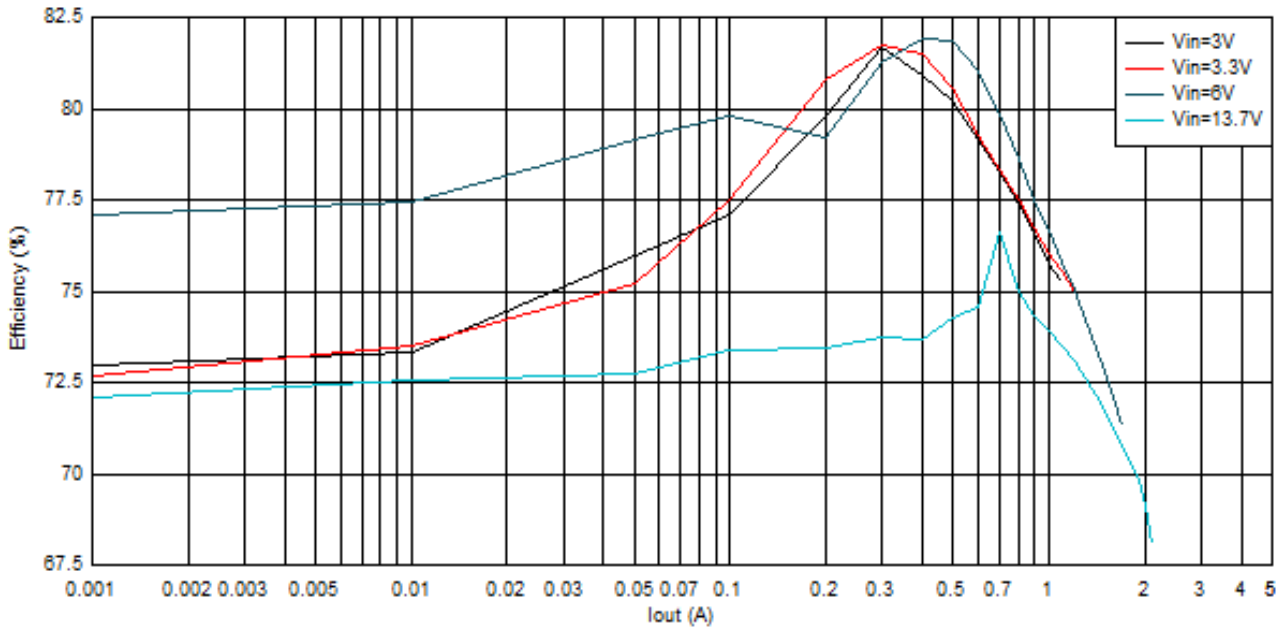


Figure 4-2. Efficiency with  $V_{OUT} = -3.3\text{ V}$

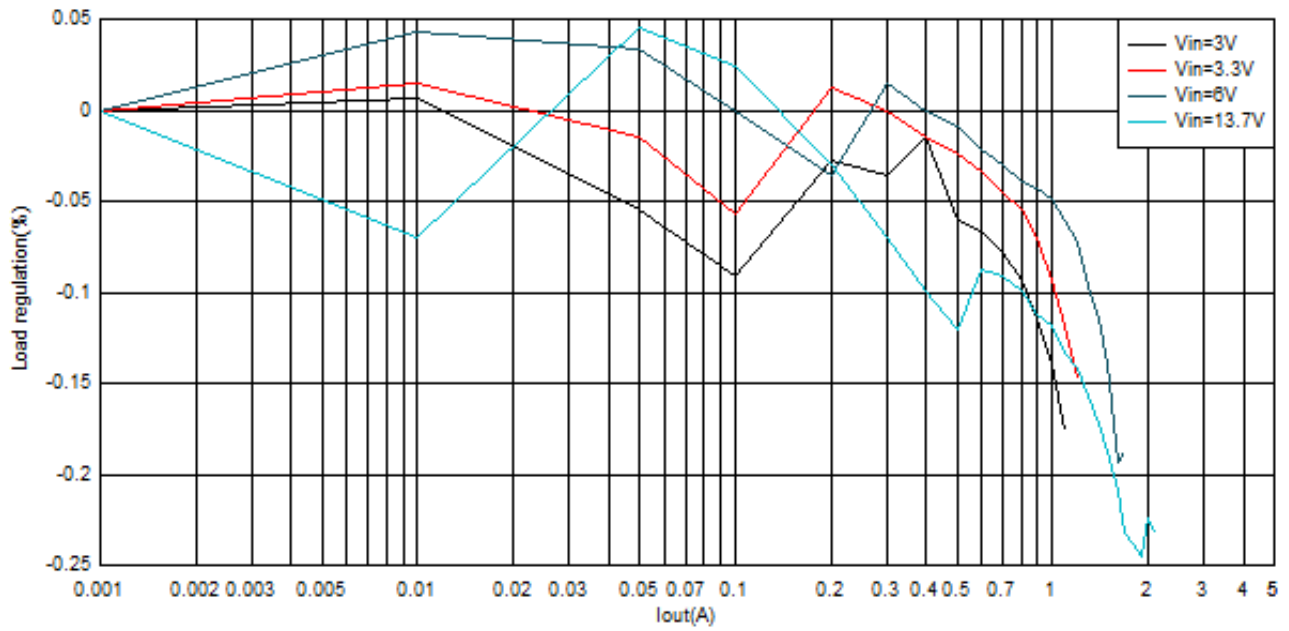


Figure 4-3. Load Regulation with  $V_{OUT} = -3.3\text{ V}$

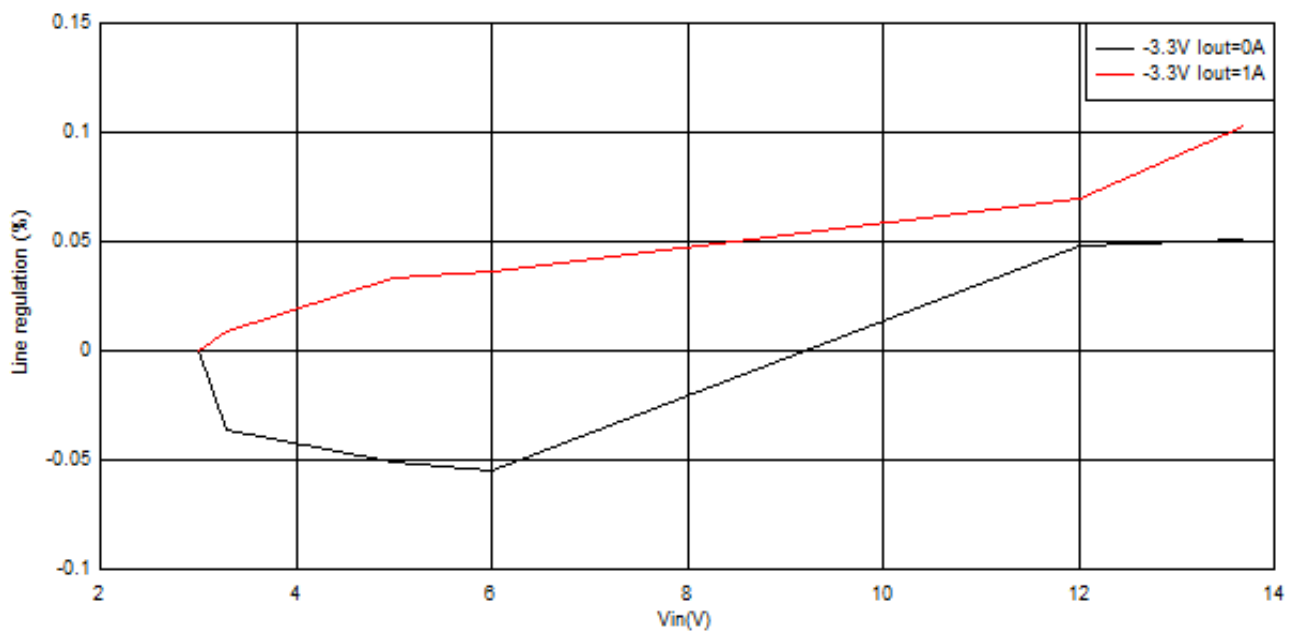


Figure 4-4. Line Regulation with  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 0\text{ A}$  and  $1\text{ A}$

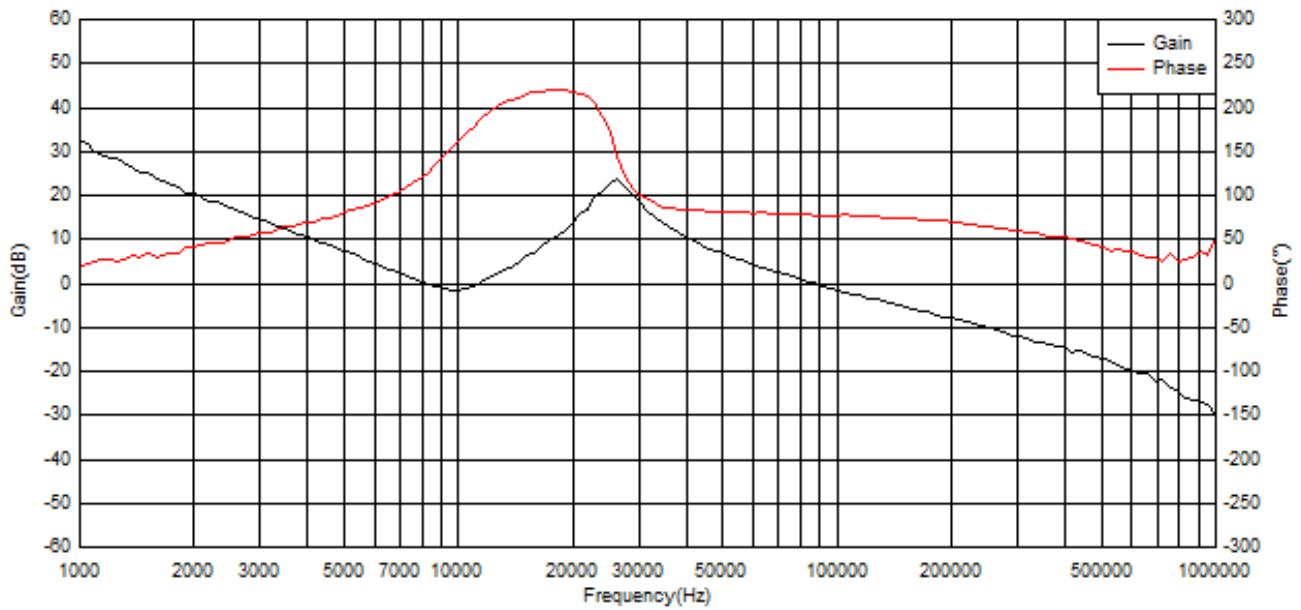


Figure 4-5. Loop Response with  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$

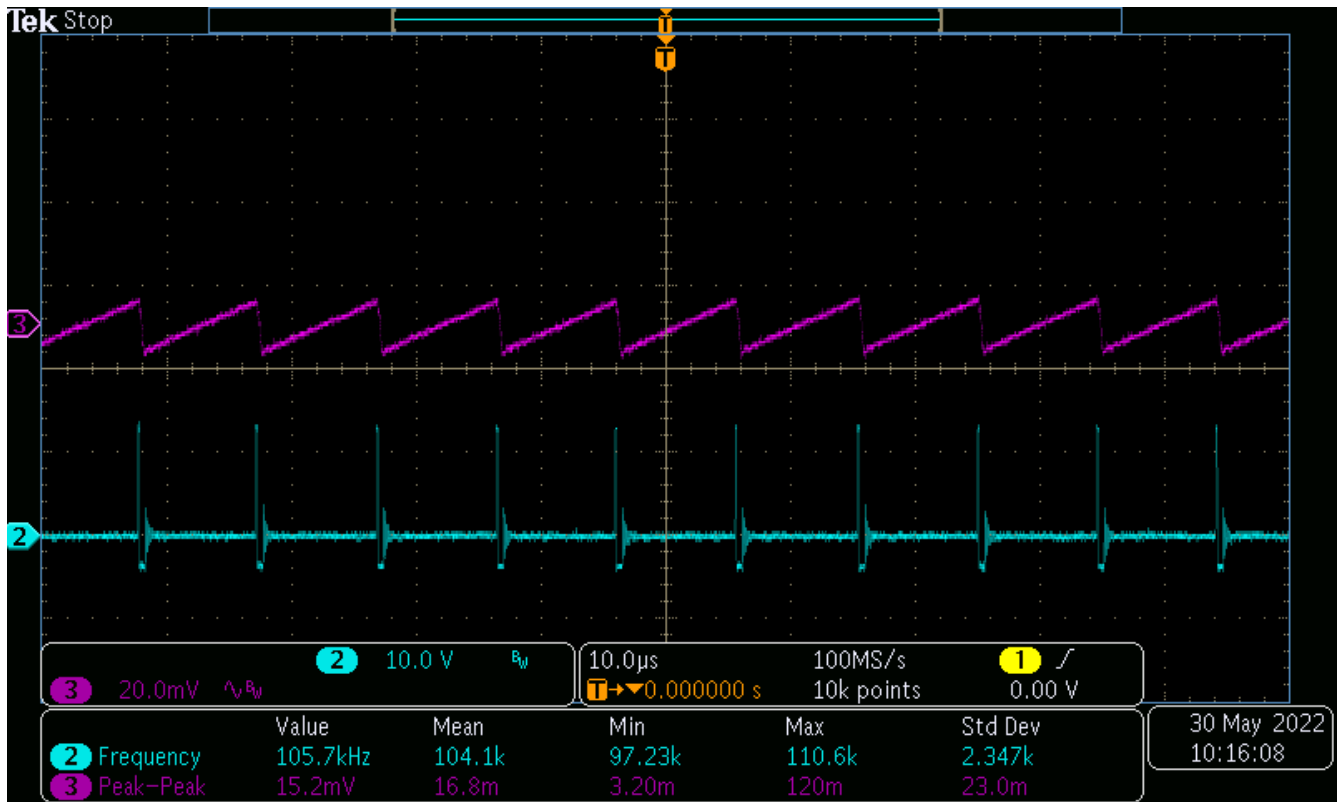


Figure 4-6. Output Voltage Ripple with  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 30\text{ mA}$

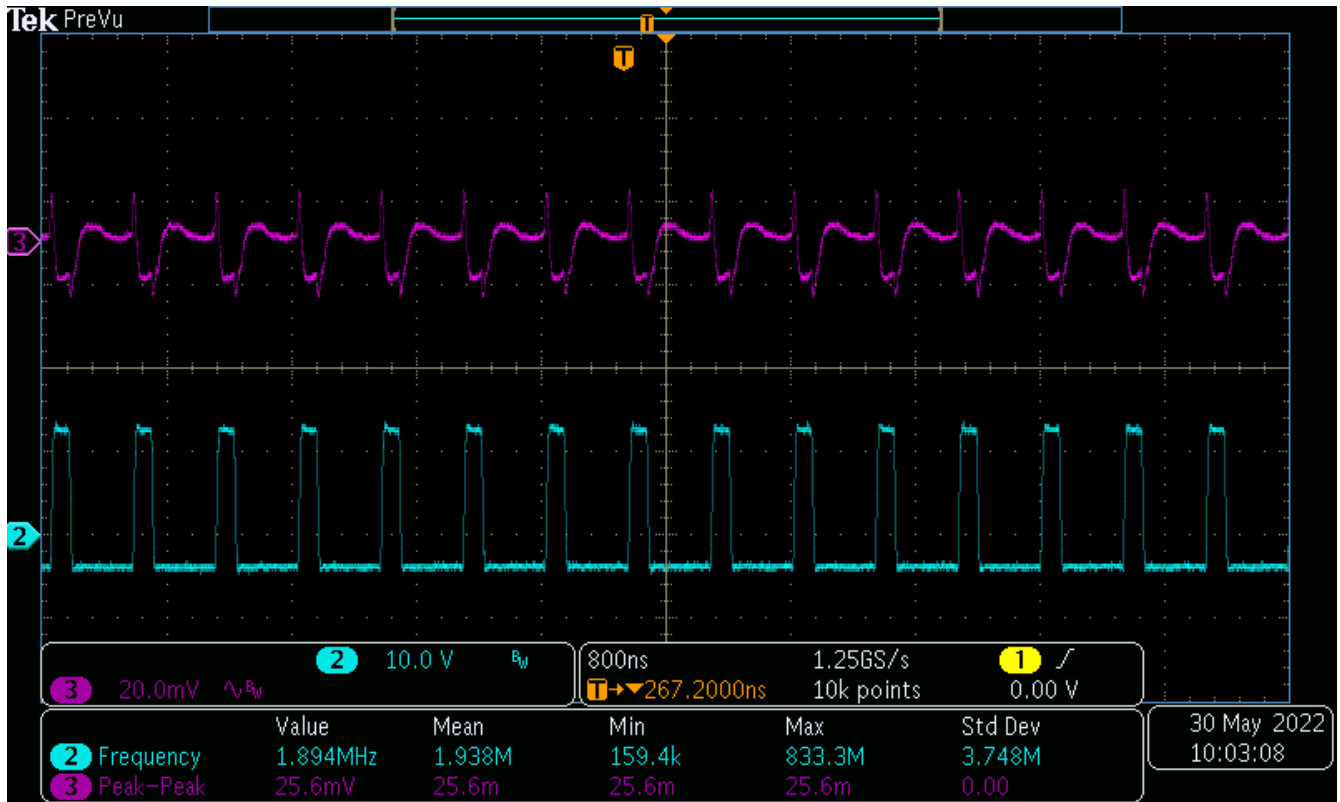


Figure 4-7. Output Voltage Ripple with  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$

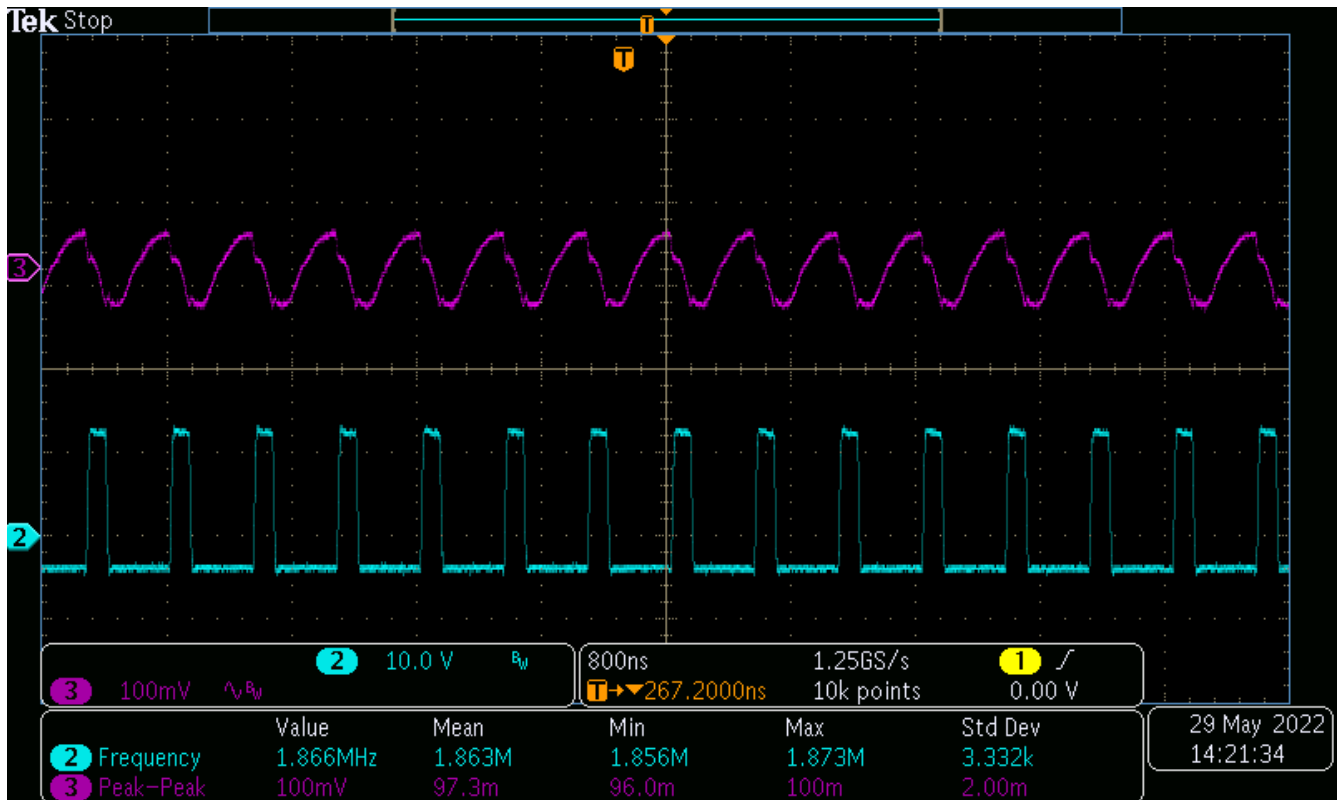


Figure 4-8. Input Voltage Ripple with  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$

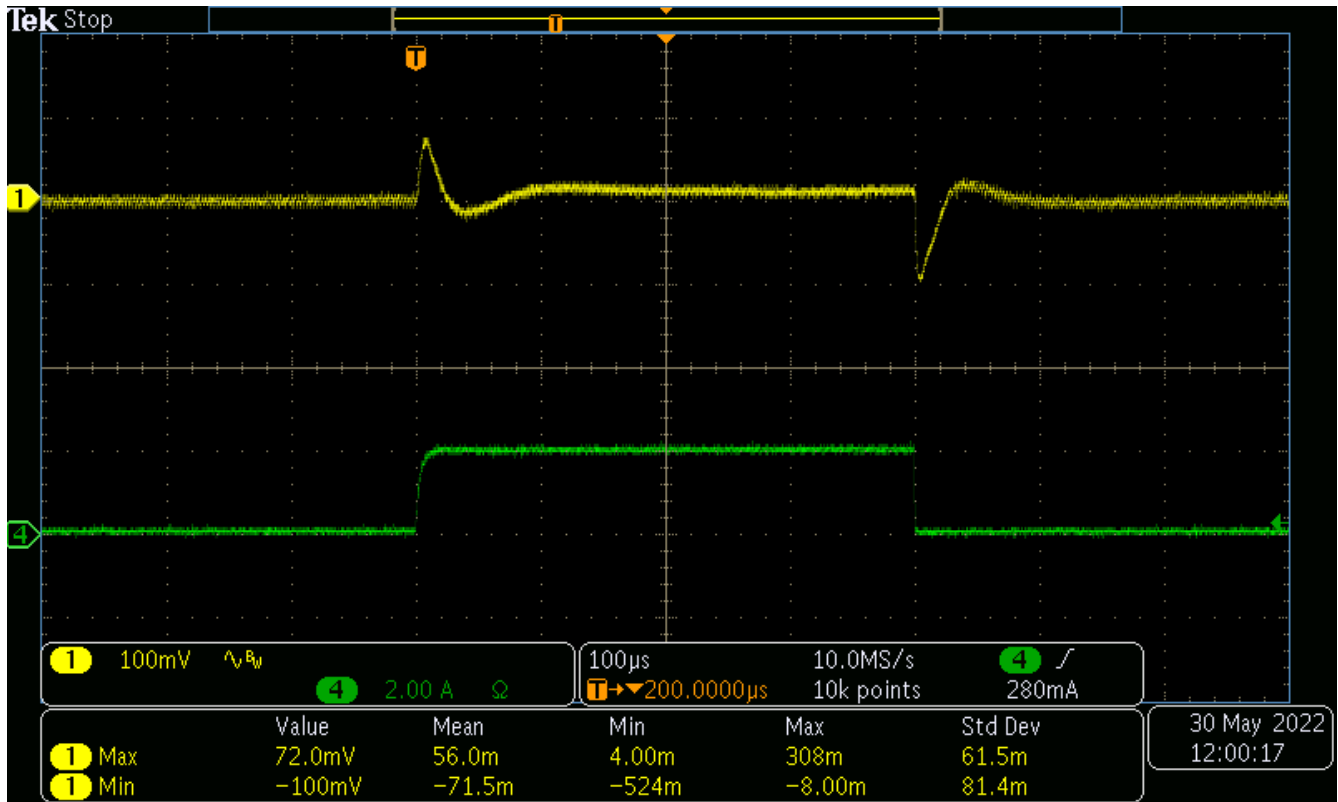


Figure 4-9. Load Transient with  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 0.1\text{ A}$  to  $2\text{ A}$

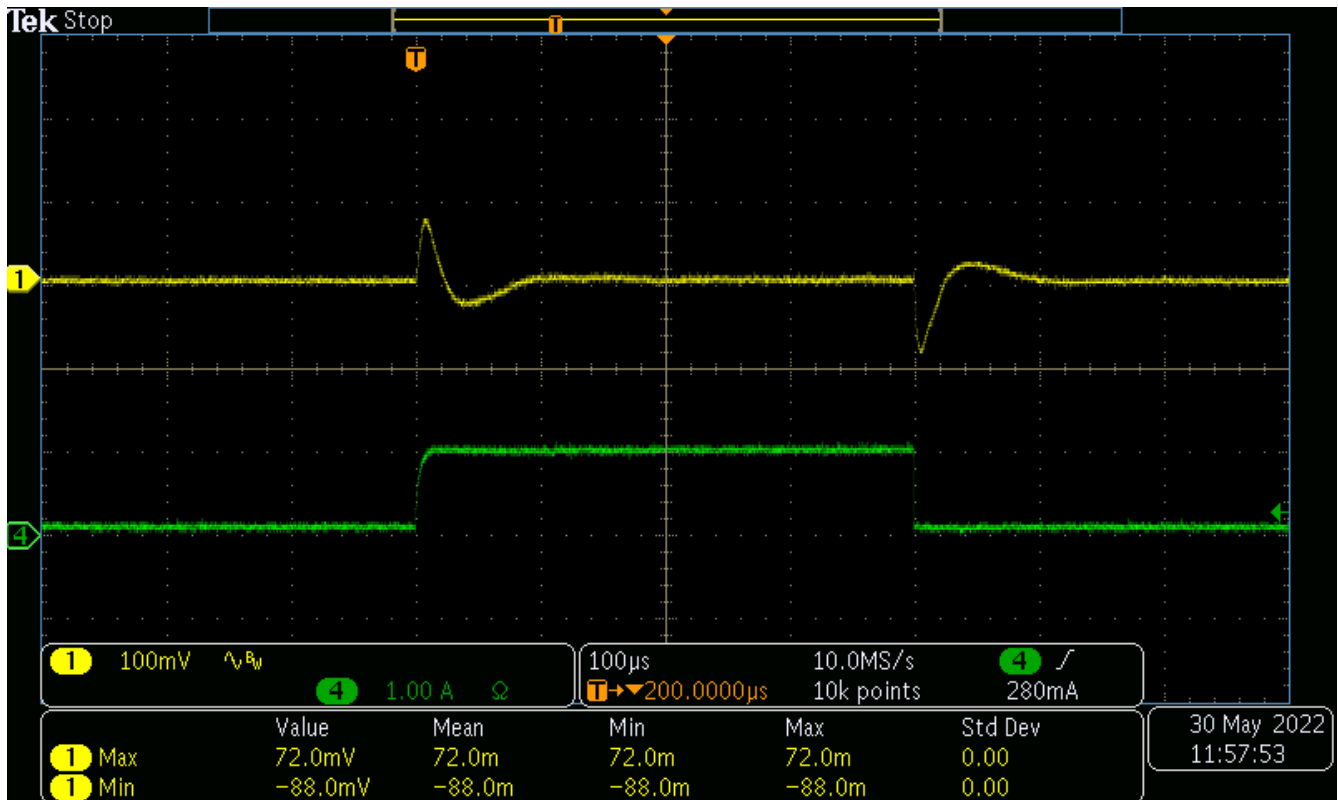


Figure 4-10. Load Transient with  $V_{IN} = 3.3\text{ V}$ ,  $V_{OUT} = -3.3\text{ V}$ ,  $I_{OUT} = 0.1\text{ A}$  to  $1\text{ A}$

## 5 Conclusion

The TPS62903 can be configured as an inverting buck boost converter to generate a negative output voltage. The inverting buck boost topology changes some system characteristics, such as input voltage range and maximum output current. This application note explains the inverting buck boost topology and how to select the external components with the changed system characteristics. Measured data from the example design is provided.



## 6 References

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3. Texas Instruments, [TPS62903-Q1 3-V to 18-V, 3-A, Automotive Low IQ Buck Converter with +165°C TJ](#) data sheet.
4. Texas Instruments, [TPS62902, 3-V to 17-V, 2A, High Efficiency and Low IQ Buck Converter in 1.5-mm × 2-mm QFN Package](#), data sheet.
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6. Texas Instruments, [Using the TPS629210-Q1 in an Inverting Buck–Boost Topology](#) application note.
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12. Texas Instruments, [Working with Inverting Buck-Boost Converters](#) application note.
13. Robert W. Erickson: *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 1997
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15. Texas Instruments, [Simplifying Stability Checks](#) application note.
16. Texas Instruments, [DCS-Control™ landing page](#).

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