Powering the TMS320DM368 With TPS650061

This document details the design considerations of a low-cost power solution for the TMS320DM368 low-power application processor with a TPS650061, three-rail Power Management Unit (PMU) or Power Management Integrated Circuit (PMIC).

Portable application solution size demands a high level of integration and the TMS320DM368 requires at least three different voltage rails with specific sequencing and reset requirements. The TPS650061 is a highly integrated, low-cost power solution providing the 1.35-, 1.8-, and 3.3-V rails and $\overline{\text{RESET}}$ signals required by the TMS320DM368. The TPS650061 has a single, step-down converter, two low-dropout regulators, and a voltage supervisor.

Included in this document is a power solution for the TMS320DM368. Power requirements, schematic, operational waveforms, and a bill of materials are provided.

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1 Power Requirements

Figure 1 presents the block diagram for the TPS650061 and the TMS320DM368 (also referred to as 'DM368).

The 'DM368 power requirements are listed in Table 1.

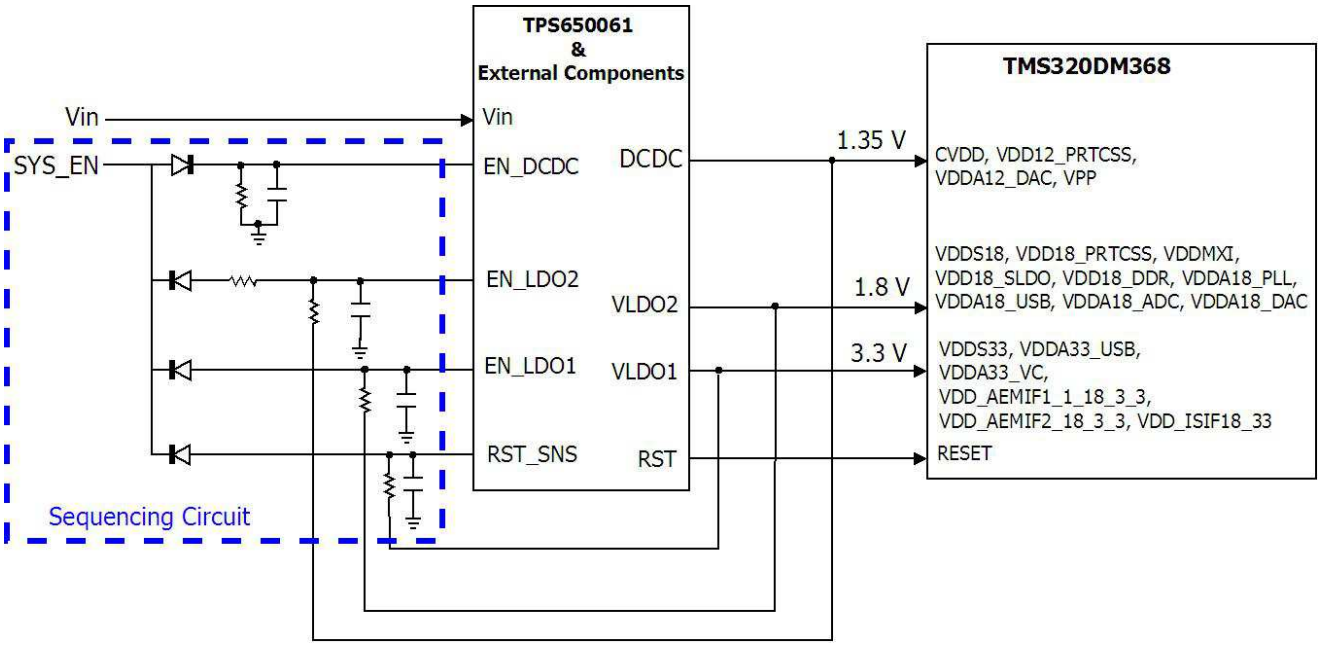

Figure 1. TPS650061 and TMS320DM368 Block Diagram

Table 1. 'DM368 Power Requirements

Rail Name	Voltage (V)	Imax (mA)	Tolerance (%)	Power On	Power Off
CVDD, VDD12_PRTCSS, VDDA12_DAC, VPP	1.35	1000	±5	First	Third
VDDS18, VDD18_PRTCSS, VDDMXI, VDD18_SLDO, VDD18_DDR, VDDA18_PLL, VDDA18_USB, VDDA18_ADC, VDDA18_DAC	1.8	125	±5	Second	Second
VDDS33, VDDA33_USB, VDDA33_VC, VDD_AEMIF1_1_18_3_3, VDD_AEMIF2_18_3_3, VDD_ISIF18_33	3.3	146	±5	Third	First

The TPS650061 meets these power requirements. Power sequencing is implemented using a simple sequencing circuit that controls the order at which the power supplies in the TPS650061 are enabled.

1.1 Power-On Sequence

Meet the 'DM368 power-on requirements by powering on the 1.35-V rail first, then both the 1.8-V rail and the 3.3-V rail power on. After all three rails are powered on, $\overline{\text{RESET}}$ is released.

Per the excerpt from the TMS320DM368 data sheet for simple power-on, the device must be powered on in the following order:

1. Power on PRTCSS/Main Core (1.35 V)
2. Power on PRTCSS/Main I/O (1.8 V)
3. Power on the Main/Analog I/O (3.3 V)

$\overline{\text{RESET}}$ must be low until all supplies are ramped up.

1.2 Power-Off Sequence

The 'DM368 power-down requirements state that the supplies must power off in the reverse order from which they are powered on. These requirements are described in the TMS320DM368 data sheet for simple power-off:

1. Power off Main/Analog I/O (3.3 V)
2. Power off PRTCSS/Main I/O (1.8 V)
3. Power off PRTCSS/Main Core (1.35 V)

If $\overline{\text{RESET}}$ is low, steps 2 and 3 may be performed simultaneously.

If $\overline{\text{RESET}}$ is not low, these steps must be followed sequentially.

1.3 Power Solution

The proper connections for the power-on and power-off sequence are shown in Figure 2.

For power-on, an external system enable signal SYS_EN is enabled HIGH. Diodes D2, D3, and D4 are reversed biased. Diode D1 is forward biased and EN1.35 is HIGH. This turns ON the 1.35-V DCDC rail. The output voltage of the DCDC converter, VO_1.35, is filtered into the enable of the LDO2 converter, EN1.8, and creates an RC (R8 and C12) delay before turning ON the 1.8-V rail. When EN1.8 reaches the turn-on threshold of the converter, VO_1.8 ramps up to nominal voltage. The output voltage of the LDO2, VO_1.8, is filtered into the enable of the LDO1 converter, EN3.3, and creates an RC (R4 and C10) delay before turning ON the 3.3-V rail. When EN3.3 reaches the turn ON threshold of the converter, VO_3.3 ramps up to nominal voltage. Lastly, the output voltage of the LDO1 converter, VO_3.3, is coupled into the reset sense-fail pin of the TPS650061, RSTSNS. The RST_SNS signal is sensed through an internal comparator in the TPS650061 and triggers the RST signal HIGH when RSTSNS reaches 0.6 V and after a time delay dictated by C4. Power-on sequence is complete.

For power-off, SYS_EN is LOW. D2, D3, and D4 are forward biased. RSTSNS becomes LOW to pull RST LOW. EN3.3 becomes LOW and VO_3.3 ramps down. The EN1.8 signal is filtered to create an RC (R7 and C12) delay between VO_3.3 ramping down and VO_1.35 ramping down. Lastly, D1 is reversed biased and capacitor C11 discharges through resistor R1 with a delay longer than the ramping down of VO_3.3 and VO1.8. Therefore, after VO_3.3 and VO_1.8 are off, the 1.35-V rail ramps down. Power-off sequence is complete.

2 Schematic, Waveforms, and Bill of Materials

2.1 Schematic

Figure 2 shows the circuit schematic detailing the external components required by the TPS650061 to achieve the 1.35-, 1.8-, and 3.3-V power rails required by the 'DM368. In addition, Figure 2 shows the sequencing circuit that achieves the proper power-on, power-off, and reset sequencing required by the ‘DM368.

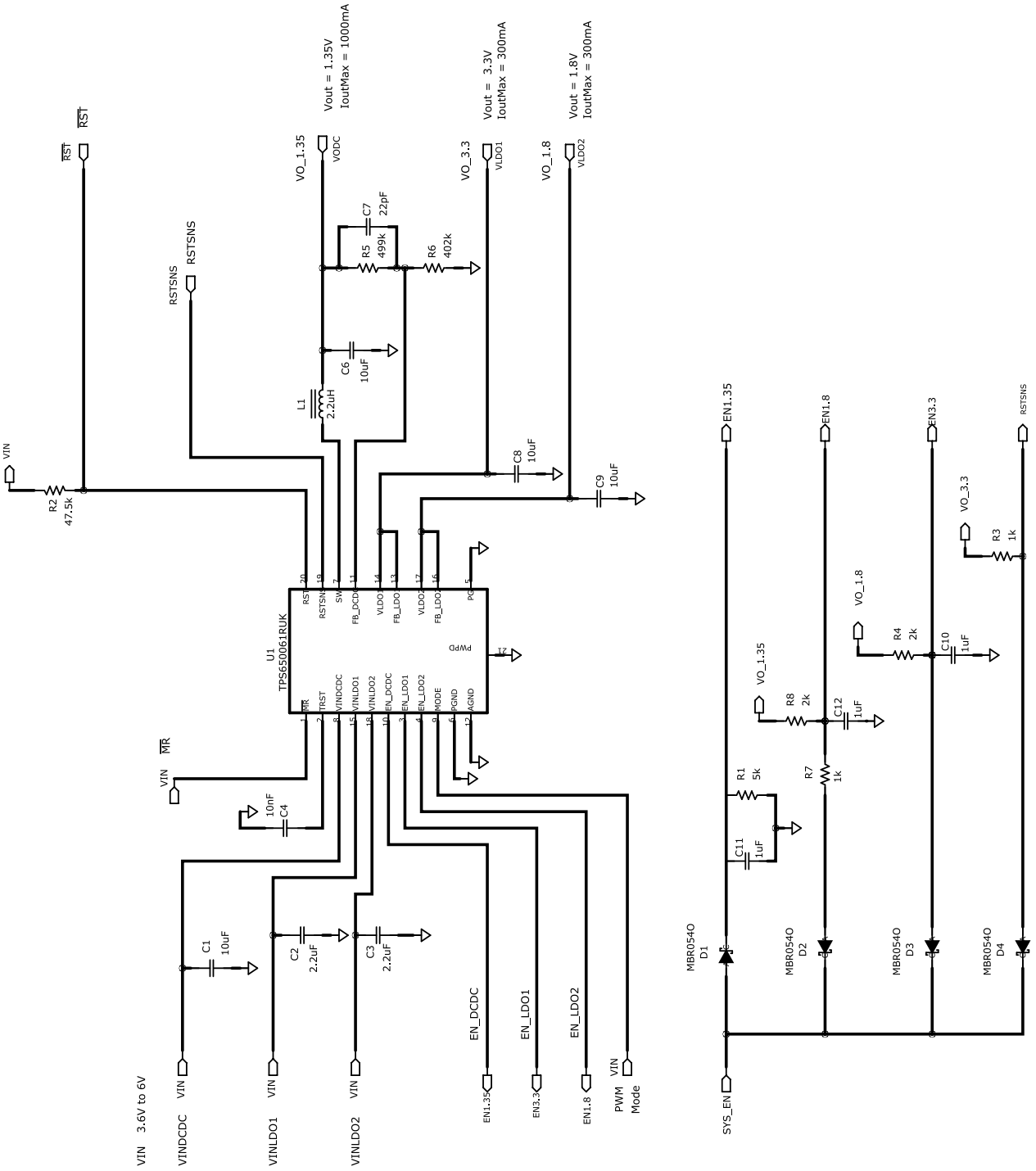

Figure 2. TPS650061 External Components and Sequencing Circuit for the ‘DM368

2.2 Waveforms

The following waveforms demonstrate the power-up and power-down sequence of the TPS650061 as required by the 'DM368. Figure 3 shows the TPS650061 power-on sequence where 1.35-V, then 1.8-V, and then 3.3-V rails ramp up when the system enable is HIGH.

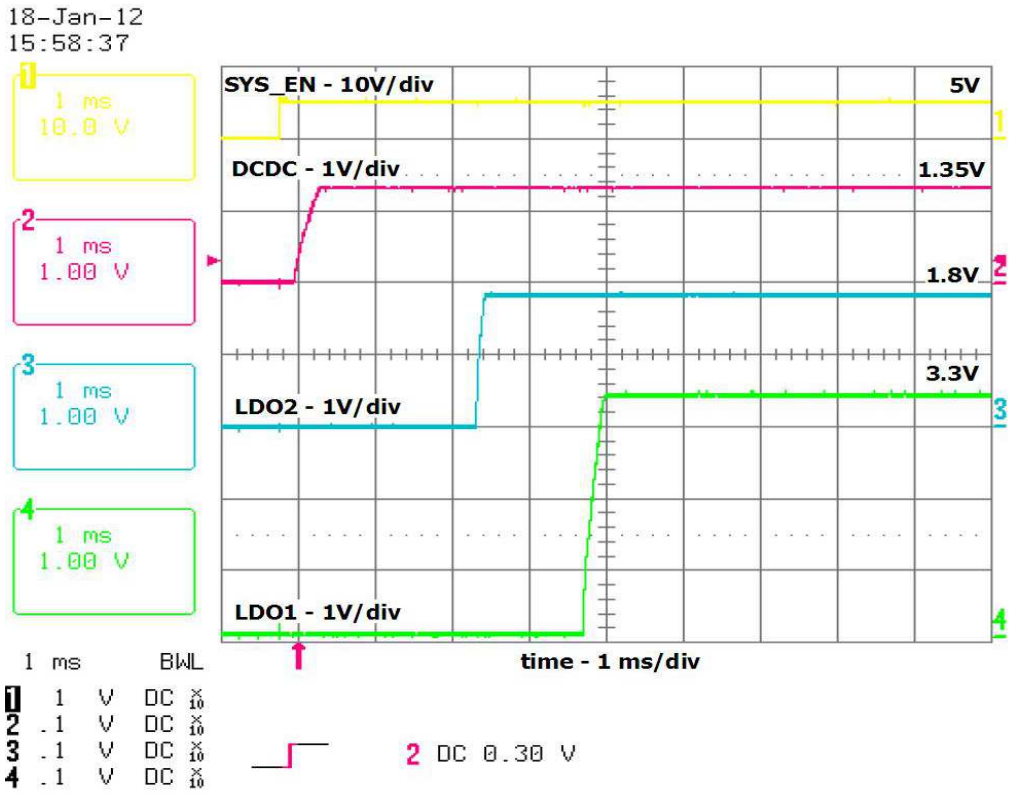

Figure 3. Power-Up Sequence With System Enable HIGH

Figure 4 shows the reset pin, RST, being released after the rails have ramped up and after the reset recovery time, t_{RST}, is exceeded. The measurements were taken under a 1000-mA load on 1.35 V, 125-mA load on 1.8 V, and 146-mA load on 3.3 V.

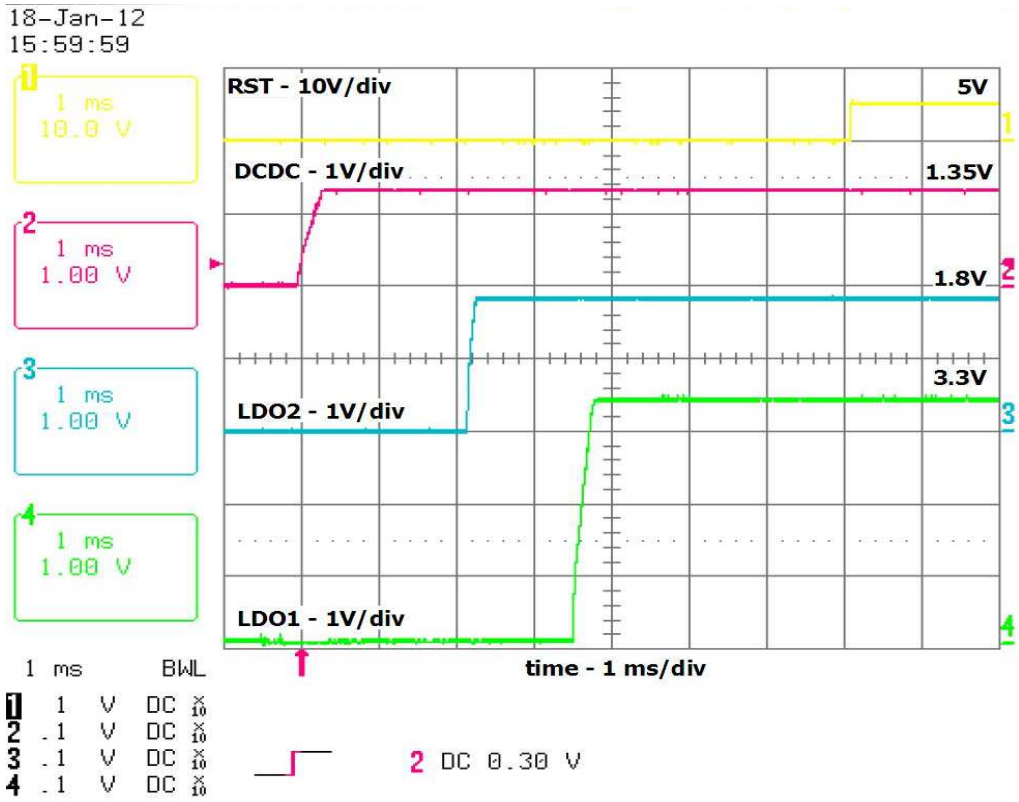

Figure 4. Power-Up Sequence and Reset Release

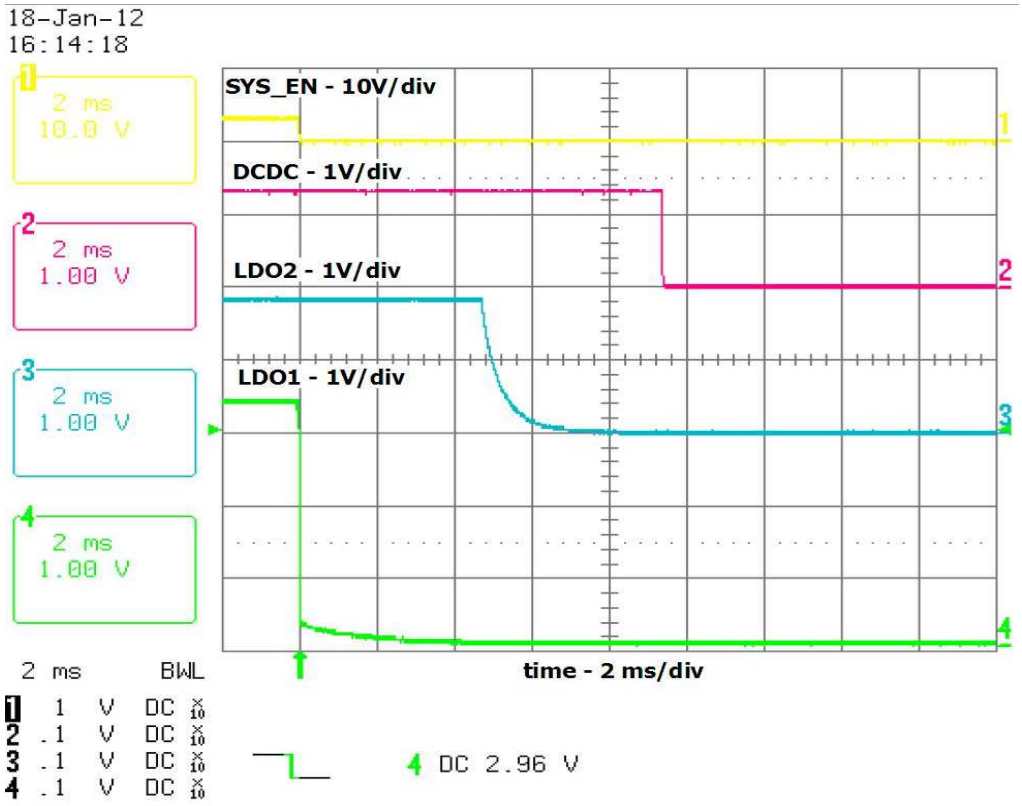

Figure 5. Power-Down Sequence With System Enable LOW

Figure 5 shows the power-down sequence of the 3.3-V, then 1.8-V, and then 1.35-V rails ramping down after system enable SYS_EN is pulled low. Figure 6 shows the reset pin being pulled low during power-off. The measurements were taken under a 1000-mA load at 1.35 V, 125-mA load at 1.8 V, and 146-mA load at 3.3 V.

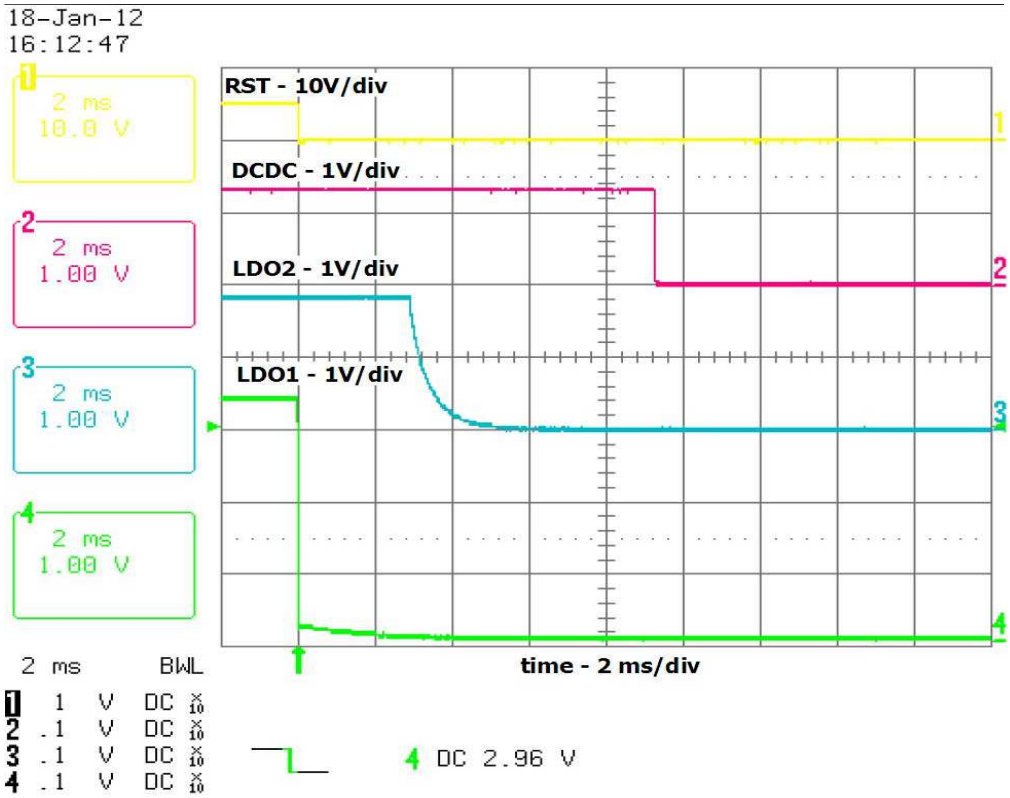

Figure 6. Power-Down Sequence and Reset Pulled LOW

2.3 Bill of Materials

The bill of materials is displayed in Table 2.

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	10 µF	Capacitor, ceramic, 10 V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata
1	C2	2.2 µF	Capacitor, ceramic, 10 V, X5R, 10%	0603	GRM188R61C225KE15D	Murata
1	C3	2.2 µF	Capacitor, ceramic, 10 V, X5R, 10%	0603	GRM188R61C225KE15D	Murata
1	C4	10 nF	Capacitor, ceramic, 16 V, X7R, 10%	0603	Std	Std
1	C6	10 µF	Capacitor, ceramic, 10 V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata
1	C7	22 pF	Capacitor, ceramic, 50 V, C0G, 5%	0603	Std	Std
1	C8	10 µF	Capacitor, ceramic, 10 V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
1	C9	10 µF	Capacitor, ceramic, 10 V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata
1	C10	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	TDK	TDK
1	C11	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	TDK	TDK
1	C12	1 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0805	TDK	TDK
1	D1	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D2	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D3	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	D4	MBR054O	Diode, Schottky, 0.5 A, x0V	SOD-123	MBR054O	MCC Semi
1	L1	2.2 µH	Inductor, SMT, 2.0 A, 110 mΩ	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft
1	R1	5 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R2	47.5 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R3	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R4	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R5	499 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R6	402 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R7	1 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	R8	2 kΩ	Resistor, chip, 1/16W, 5%	0603	Std	Std
1	U1	TPS650061RUK	IC, 2.25-MHz step-down converter with dual LDOs and SVS	QFN	TPS650061RUK	TI

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

3 Conclusion

The TPS650061 provides a low-cost, comprehensive power solution for the 'DM368. A simple logic circuit controls the sequencing for each power rail. A 1.35-V rail (capable of supplying 1 A) is powered on, followed by a 1.8-V rail (300 mA), and then a 3.3-V rail (300 mA). Once all three supplies have reached regulation, $\overline{\text{RESET}}$ goes high (that is, rises to its pullup voltage). For power-down, the 3.3-V rail turns off, then the 1.8-V, and lastly the 1.35-V rail. This meets the power requirements of the 'DM368.

4 References

1. *TMS320DM368, Digital Media System-on-Chip* data sheet (SPRS668)
2. *TPS650061, 2.25 MHz Step Down Converter with Dual LDOs and SVS* data sheet (SLVS810)

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