LMH1297EVM Evaluation Board

The LMH1297EVM is an evaluation module designed for high-speed performance and functional evaluation of the Texas Instruments LMH1297 12G UHD-SDI 75-Ω bidirectional I/O with integrated reclocker. With this kit, users can quickly evaluate the cable reach and output signal integrity supported by the LMH1297. High-performance edge-mount BNC connectors are used at the 75-Ω port for the SDI_IO and SDI_OUT signals, while 100-Ω differential input and output ports are routed to edge-mount SMA connectors. These connectors facilitate connection to lab equipment or user systems for performance evaluation. An onboard MSP430 MCU is included to support an optional SMBus or SPI serial control interface when configuring the LMH1297 operating modes.

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1 Overview

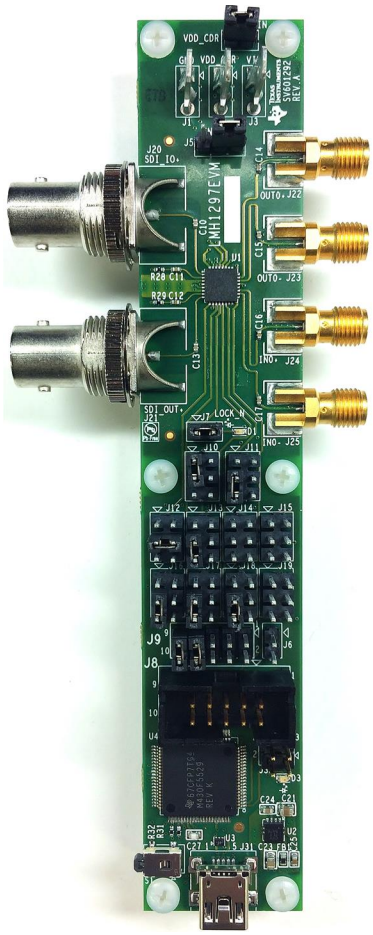

Figure 1. LMH1297EVM

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2 Features

- User-Configurable Adaptive Cable Equalizer or Cable Driver With Integrated Reclocker
- Supports ST-2082-1 (12G), ST-2081-1 (6G), ST-424 (3G), ST-292 (HD), and ST-259 (SD)
- Integrated Reclocker Locks to SMPTE Video Rates of 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps or Divide-by-1.001 Sub-Rates and 270 Mbps
- EQ (Equalizer) Mode:
  - Adaptive Cable Equalizer at 75-Ω Single-Ended Input on SDI_IO
  - 100-Ω Output Driver With De-Emphasis on OUT0
  - Line-Side Reclocked 75-Ω Loop-Through Output on SDI_OUT
- CD (Cable Driver) Mode:
  - PCB Equalizer at 100-Ω Differential Input on IN0
  - Dual Cable Drivers with Integrated Reclocker and Pre-Emphasis on SDI_IO and SDI_OUT
  - Host-Side Reclocked 100-Ω Loop-Back Output on OUT0
- Programmable Through Pins, SPI, or SMBus Interface
- Single-Supply Operation: VDD = 2.5 V ± 5%
- –40°C to +85°C Operation
- High-Speed Signal Flowthrough Pinout Package: 5-mm × 5-mm 32-Pin QFN

3 Applications

- SMPTE-Compatible Serial Digital Interface
- UHDTV/4K/8K/HDTV/SDTV Video
- IP Media Gateway
- Digital Video Processing and Editing

4 Ordering Information

Table 1. LMH1297 Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
LMH1297EVM	LMH1297RTV	QFN (32)

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5 Setup

This section describes the jumpers and connectors on the EVM as well as how to connect, set up, and use the LMH1297EVM. When operating the LMH1297EVM, signal inputs and outputs can be connected as shown in Figure 2.

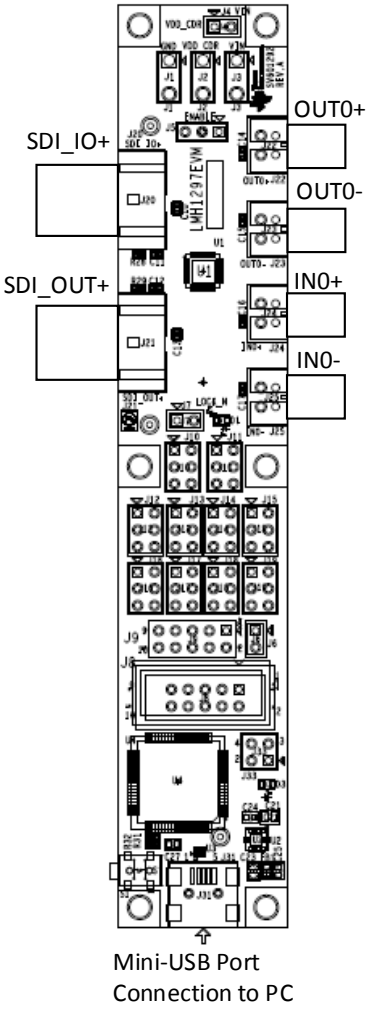

Figure 2. LMH1297EVM Input and Output Pins

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5.1 Modes of Operation

The LMH1297EVM can be used in one of three modes:

1. **Pin Mode (Default)** – Provides general access to the LMH1297 signal integrity and I/O control settings with IC pin-level logic.
2. **SPI Mode** – Provides full access to the LMH1297 signal integrity and control settings with MISO, MOSI, SCK, and SSN pins.
3. **SMBus Mode** – Provides full access to the LMH1297 signal integrity and control settings with SDA, SCL, and GND pins. ADDR0 and ADDR1 pins are used for SMBus address strap.

Using either SPI or SMBus mode, users have full access to all register controls in the LMH1297. For convenience, the LMH1297EVM features an on-chip MSP430 that is configured as a USB2ANY interface between LMH1297 and PC through the mini-USB port header on J31.

NOTE: Currently, the interface from PC to on-board MSP430 can only support SMBus communication.

The external control pins on the LMH1297EVM are used to configure the default device settings. A 4-level input scheme across the control pin interface increases the amount of control levels available to the device with fewer physical pins. The channel settings and controls are configurable in pin mode for the LMH1297 4-logic levels (L, R, F, H). The four logic levels correspond to the following voltages in Table 2.

Table 2. Description of 4-Level Voltage Inputs and Jumper Ties

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1 kΩ to VIN	VIN – 0.04 V
F	Float (Leave Pin Open)	2/3 × VIN
R	Tie 20 kΩ to GND	1/3 × VIN
L	Tie 1kΩ to GND	0.08 V

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VIN
- Internal Threshold between R and F = 0.5 × VIN
- Internal Threshold between F and H = 0.8 × VIN

To set these 4-level voltage inputs, each input is controlled by a group of 6 jumper pins set in Figure 3.

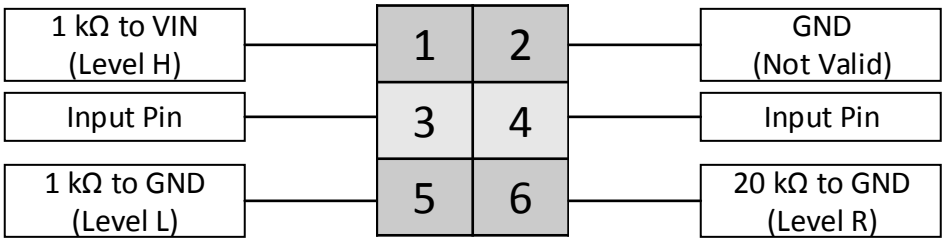

Figure 3. Jumper Orientation for User Configuration

Therefore, the following jumper positions allow access to each of the four logic levels:

LEVEL	JUMPER TIES
H	Pin 1-3
F	Pin 3-4 (or no connect)
R	Pin 4-6
L	Pin 3-5

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The following jumpers have 4-level input control: J10, J11, J12, J13, J14, J15, J16, J17, J18, and J19.

In Pin Mode, EQ/CD_SEL, OUT0_SEL, HOST_EQ0, OUT_CTRL, SDI_VOD, and SDI_OUT_SEL pins control different LMH1297 settings. Using SPI or SMBus, these initial pin control values can be overridden by setting the appropriate override bits through register control. Both SPI and SMBus interfaces allow full control over a wide range of device settings. See Table 3 and Table 4 for jumper descriptions and differences.

Table 3. Description of Connections in SPI Mode (MODE_SEL = Level F)

COMPONENT	NAME	COMMENTS
J1	GND	GND power supply
J2	VDD_CDR	2.5-V VDD_CDR power supply
J3	VIN	2.5-V VIN power supply
J4	VIN_VDD_CDR_Connect	2.5-V power supply. Shunt Pin 1 and 2 to tie VIN and VDD_CDR.
J5	ENABLE	Enable Pin for the LMH1297. Shunt Pin 1 and 2 for proper operation. Refer to LMH1297 data sheet for detailed information.
J6	SPI_MISO	Shunt Pin 1 and 2 to connect MISO signal to J8 for proper SPI mode operation.
J7	LOCK_N	Reclocker lock indicator for the selected input. Shunt Pin 1 and 2 for proper operation. Refer to LMH1297 data sheet for detailed information.
J8	SPI Access	SPI access pins. See datasheet and EVM schematic for detailed pinout information.
J9	SPI Access	For SPI mode, install Pin 1-2, 3-4, and 5-6 for SPI 3.3-V to 2.5-V level shift. Leave Pin 7-10 open. See the data sheet for additional information on SPI operation.
J10	EQ_CD_SEL	EQ_CD_SEL pin selects the I/O direction. See the data sheet and EVM schematic for additional operation information.
J11	OUT0_SEL	OUT0_SEL pin enables or disables the OUT0 100-Ω output. See datasheet and EVM schematic for additional operation information.
J12	HOST_EQ0	HOST_EQ0 pin selects the IN0 100-Ω EQ Adaption Mode settings and OUT0 100-Ω driver output amplitude and de-emphasis level. See the data sheet and EVM schematic for additional operation information.
J13	MODE_SEL	Level F: SPI Mode
J14	OUT_CTRL	OUT_CTRL selects the signal flow from the selected IN port to the enabled outputs. It selects reclocked data, reclocked data and clock, bypass reclocker (equalized data route to output driver), or both equalizer and reclocker bypassed. See the data sheet and EVM schematic for additional operation information.
J15	SDI_VOD	SDI_VOD selects incremental increase or decrease of nominal driver output amplitude applied to the SDI_IO (CD Mode) and SDI_OUT 75-Ω outputs. See the data sheet and EVM schematic for additional operation information.
J16	SS_N	Slave Select. When SS_N is at logic low, it enables SPI access to the LMH1297 slave device.
J17	MISO	MISO is the SPI serial control data output from the LMH1297 slave device. MISO is a 2.5-V LVCMOS output.
J18	SDI_OUT_SEL	SDI_OUT_SEL pin enables or disables the SDI_OUT 75-Ω output. See the data sheet and EVM schematic for additional operation information.
J19	RSV1	Reserved. Do not connect. Leave floating.

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Table 4. Description of Connections in SMBus Mode (MODE_SEL = Level L)

COMPONENT	NAME	COMMENTS
J6	SPI_MISO	Leave Pin 1 and 2 open for proper SMBus operation.
J8	SMBus Access	SMBus access pins. See the data sheet and EVM schematic for detailed pinout information.
J9	SMBus Access	External 2-kΩ pullup resistor to 3.3-V supply. Install shunt jumpers on Pin 7-8 and 9-10 for proper operation. Leave Pins 1-6 open. See the data sheet for additional information on SMBus operation.
J13	MODE_SEL	Level L: SMBus Mode
J16	ADDR0	4-Level strap pins to determine up to 16 unique SMBus address with J17 to create AD[1:0]. See the data sheet for different SMBus address combinations.
J17	ADDR1	4-Level strap pins to determine up to 16 unique SMBus address with J16 to create AD[1:0]. See the data sheet for different SMBus address combinations.

NOTE: Jumpers not listed in Table 4 are identical to the functions mentioned in Table 3.

Table 5. Input and Output Channel Connections

SIGNAL INPUTS AND OUTPUTS	
JUNCTION NUMBERS	**FUNCTION**
J20	SDI_IO+ (BNC Single-Ended)
J21	SDI_OUT+ (BNC Single-Ended)
J22, J23	OUT0+, OUT0– (SMA)
J24, J25	IN0+, IN0– (SMA)

5.2 Software/Hardware Description and Setup

By factory default, the LMH1297EVM is configured in CD Mode to accept a valid SDI signal on IN0 and output the retimed data on OUT0, SDI_IO, and SDI_OUT without programming the LMH1297 beforehand. The LMH1297EVM can also be configured by the user to operate in EQ Mode.

The general procedure for setting up and testing with the LMH1297EVM is as follows. For hardware setup and connections in the steps below, reference the illustrations in Figure 4 and Figure 5.

1. Connect 2.5-V power (0.5-A maximum) to the EVM and install the appropriate shunt jumpers to operate in SMBus Mode:
    1. Connect J3: VIN = 2.5 V and J1: GND.
        1. Install shunt jumper on J4 Pins 1-2.
    2. Set the following jumper settings for appropriate operation:
        1. Install shunt jumper on J5 Pins 1-2.
        2. Install shunt jumper on J7 Pins 1-2.
        3. Install shunt jumpers on J9 Pins 7-8 and Pins 9-10.
        4. Install shunt jumper on J11 Pins 3-5.
        5. Install shunt jumper on J13 Pins 3-5.
        6. Install shunt jumper on J16 Pins 3-5 and J17 Pins 3-5. (SMBus Address = 0x5A)
        7. Install shunt jumper on J18 Pins 3-5.
    3. **CD Mode Only:** Install shunt jumper on J10 Pins 1-3.
    4. **EQ Mode Only:** Install shunt jumper on J10 Pins 3-5.
2. Connect PC to LMH1297EVM with a USB-to-miniUSB cable through the miniUSB port located on J31. The LMH1297's control and signal integrity settings are programmable with SigCon Architect, a GUI which supports full register access through SMBus communication. For more information about SigCon

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Architect, reference the *SigCon Architect: Installation and Starter's Guide*.

3. **CD Mode Only:** Connect the LMH1297EVM to the system under test.
    1. The input signal on J24 and J25 can be connected to a video signal generator over matched 100-Ω differential cables. Either an LMH1219EVM or a second LMH1297EVM in EQ Mode can be used as a 75-Ω single-ended to 100-Ω differential converter before the DUT. In this case, either the LMH1219's 100-Ω OUT0± output or the second LMH1297's 100-Ω OUT0± output can be connected to IN0± on J24 and J25.
    2. The output signal OUT0± on J22 and J23 can be connected with matched 100-Ω differential cables to a high-speed scope to view the output eye diagram. Alternatively, this 100-Ω output can be used as the source for another SDI cable driver.
    3. The output signals on J20 and J21 are dual cable driver outputs. SDI_IO+ on J20 can be connected with 75-Ω coax cable to a video pattern analyzer, while the secondary SDI_OUT+ output on J21 can be used as a duplicate cable driver output.
4. **EQ Mode Only:** Connect the LMH1297EVM to the system under test.
    1. The input signal on J20 can be connected to a video signal generator over a 75-Ω coax cable. Either an LMH1218EVM or a second LMH1297EVM in CD Mode can be used as a 100-Ω differential to 75-Ω single-ended converter before the DUT. In this case, either the LMH1218's 75-Ω OUT0+ output or the second LMH1297's 75-Ω SDI_IO+ output can be connected to SDI_IO+ on J20.
    2. The output signal OUT0± on J22 and J23 can be connected with matched 100-Ω differential cables to a high-speed scope to view the output eye diagram.
    3. The output signal SDI_OUT+ on J21 can be connected with a 75-Ω coax cable to a video pattern analyzer as a loop through output.

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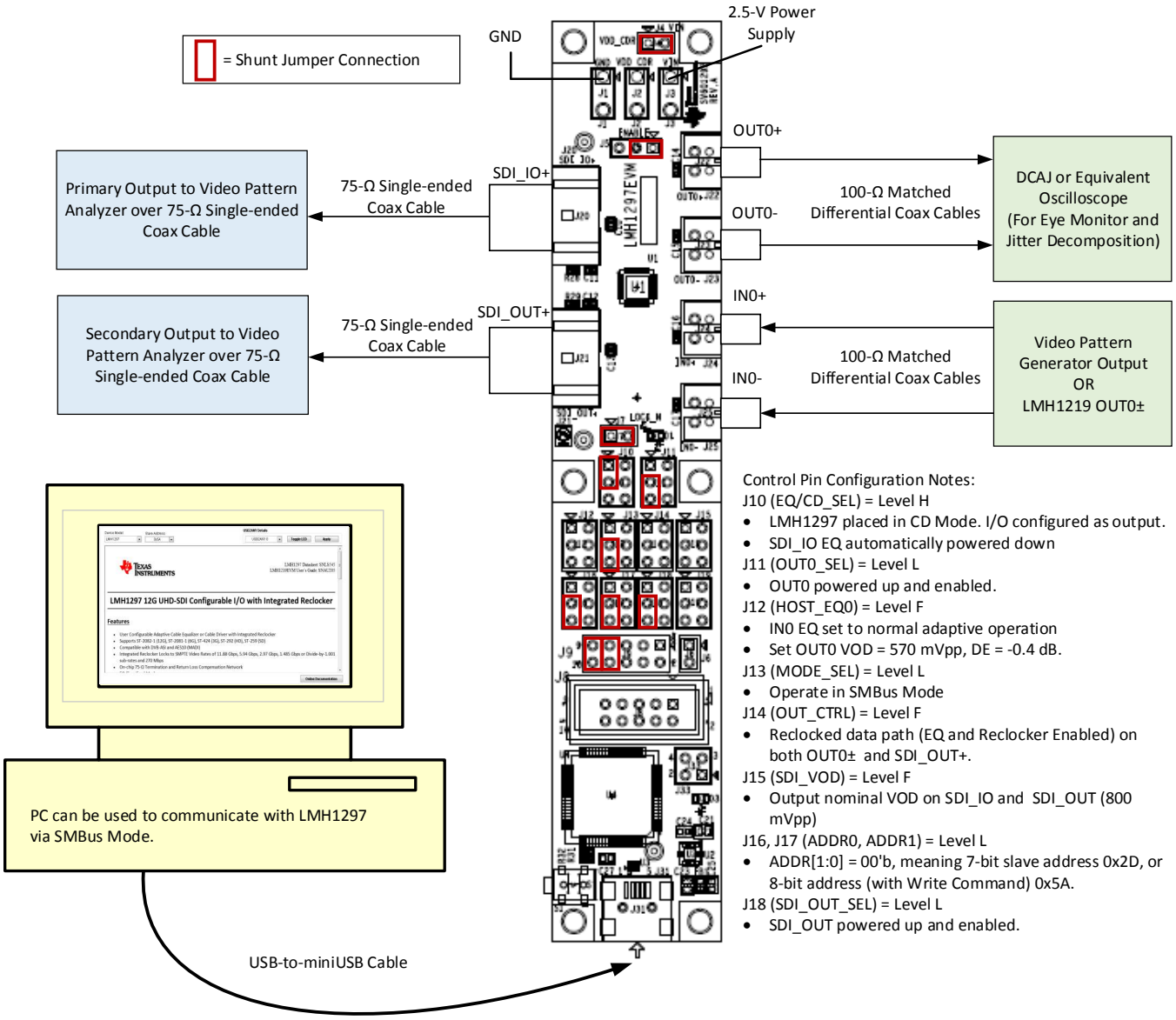

Figure 4. LMH1297EVM CD Mode Default Setup for SMBus Operation With SigCon Architect

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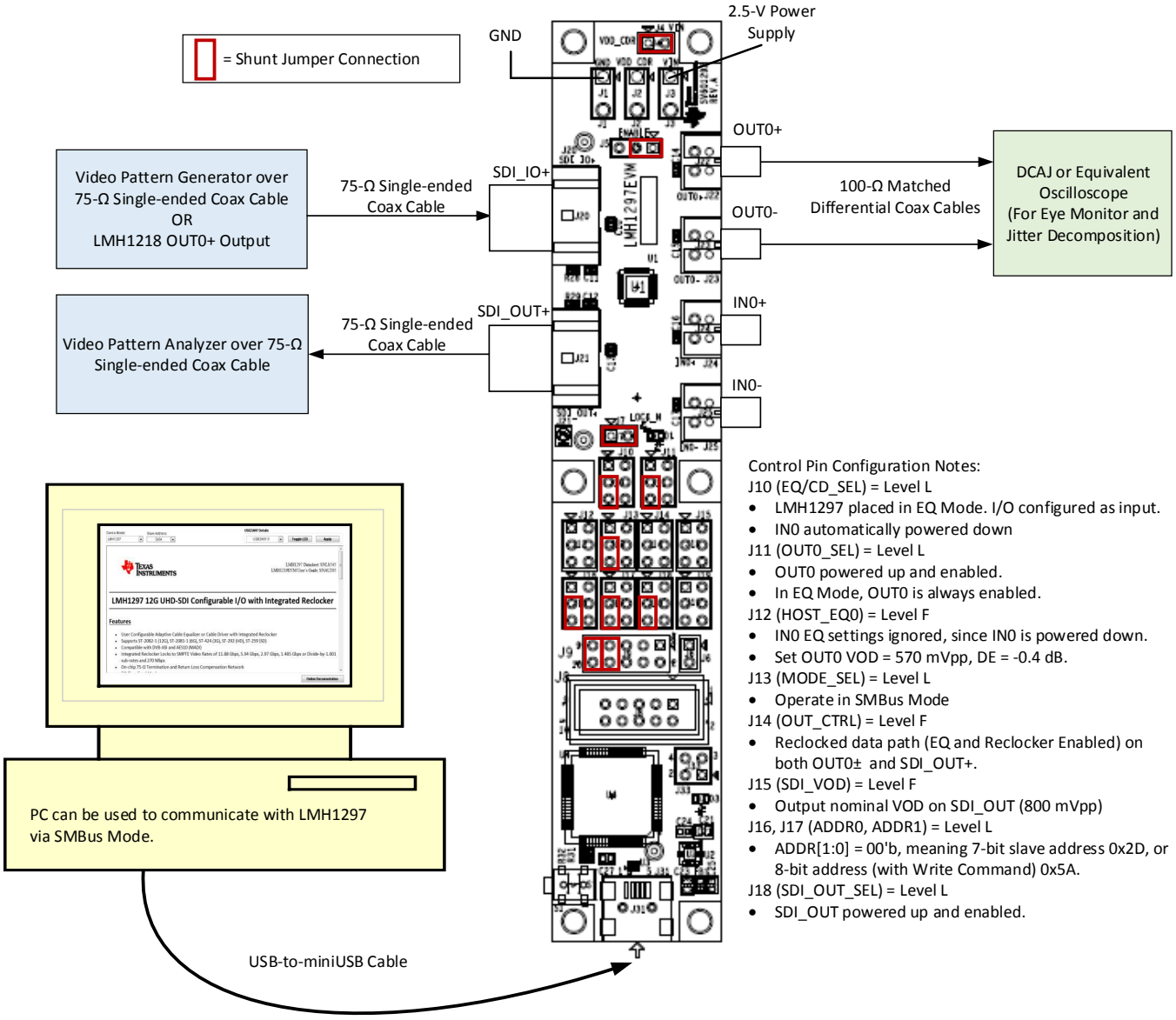

Figure 5. LMH1297EVM EQ Mode Default Setup for SMBus Operation With SigCon Architect

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5.3 Retimed Output at 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, and 270 Mbps

The eye diagrams in the left column of this subsection show the reclocked output eye of SDI_IO+ in CD Mode under the following conditions:

- Input Signal: PRBS-10, 800-mVp-p Launch Amplitude on IN0±
- VIN = 2.5 V, T = 25°C

The eye diagrams in the right column of this subsection show the reclocked output eye of differential OUT0± in EQ Mode under the following conditions:

- Input Signal: PRBS-10, 800-mVp-p Launch Amplitude on SDI_IO+
- VIN = 2.5 V, T = 25°C

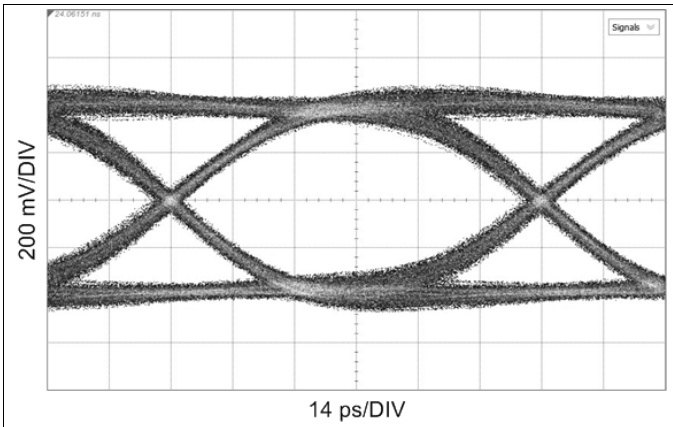

Figure 6. CD Mode at 11.88 Gbps, Measured at SDI_IO+, Reclocked Output

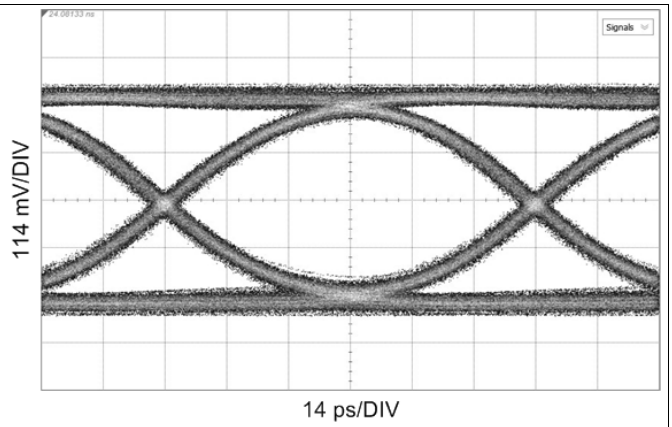

Figure 7. EQ Mode at 11.88 Gbps, Measured at OUT0±, Reclocked Output

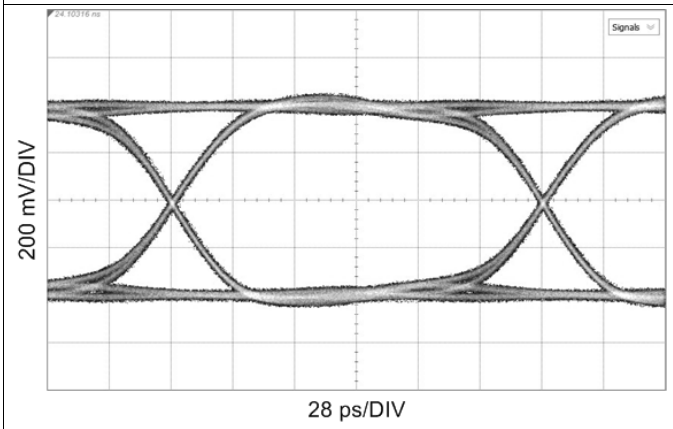

Figure 8. CD Mode at 5.94 Gbps, Measured at SDI_IO+, Reclocked Output

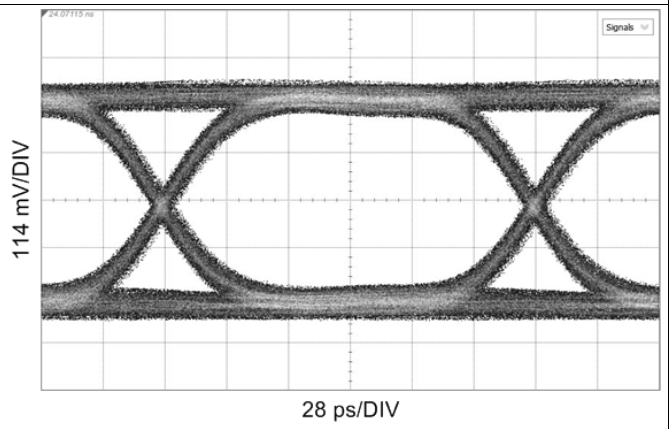

Figure 9. EQ Mode at 5.94 Gbps, Measured at OUT0±, Reclocked Output

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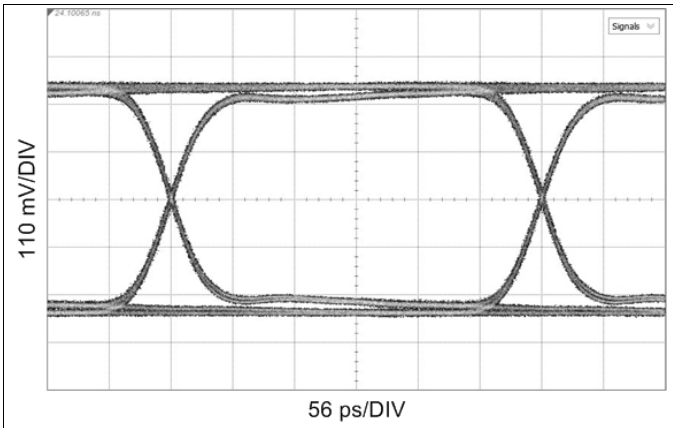

Figure 10. CD Mode at 2.97 Gbps, Measured at SDI_IO+, Reclocked Output

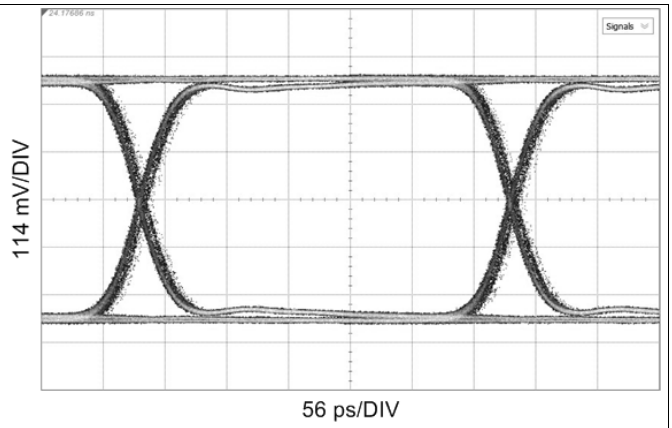

Figure 11. EQ Mode at 2.97 Gbps, Measured at OUT0±, Reclocked Output

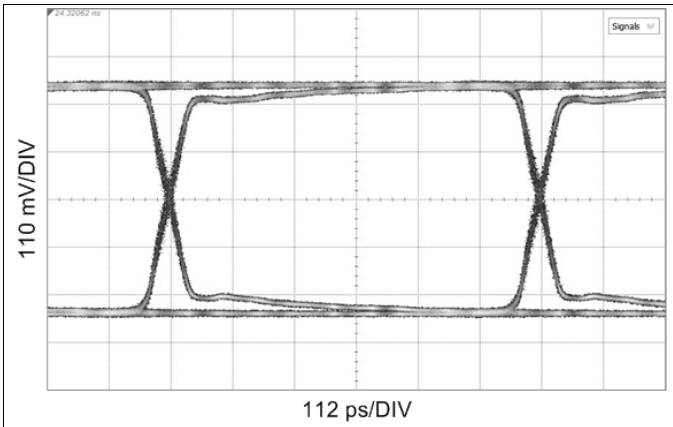

Figure 12. CD Mode at 1.485 Gbps, Measured at SDI_IO+, Reclocked Output

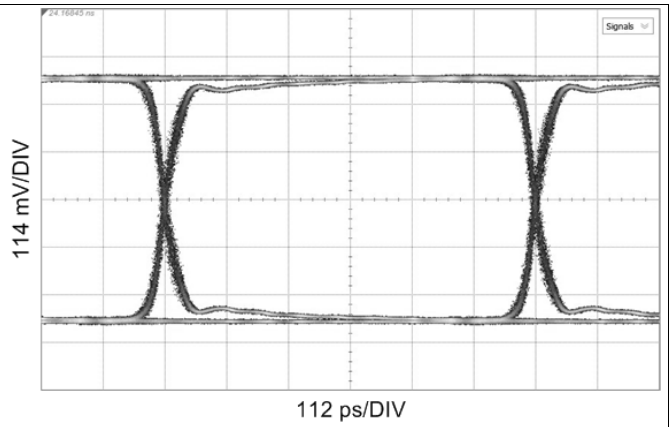

Figure 13. EQ Mode at 1.485 Gbps, Measured at OUT0±, Reclocked Output

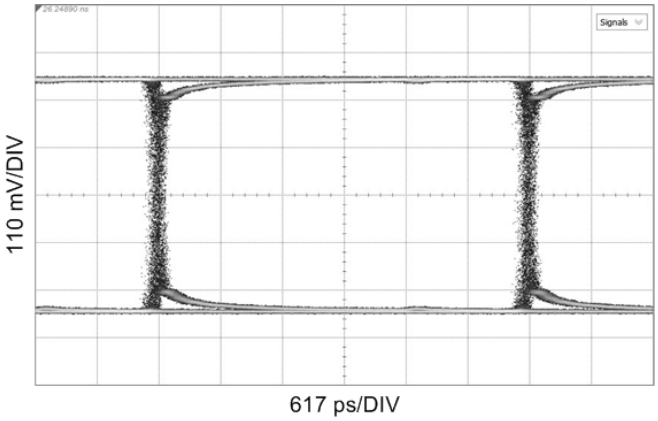

Figure 14. CD Mode at 270 Mbps, Measured at SDI_IO+, Reclocked Output

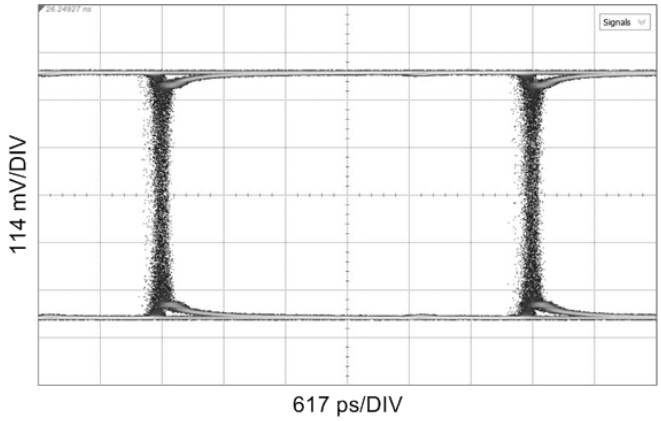

Figure 15. EQ Mode at 270 Mbps, Measured at OUT0±, Reclocked Output

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6 SigCon Architect LMH1297 GUI Profile

SigCon Architect GUI can be used to access the LMH1297 register controls easily. There are four pages associated with the LMH1297 profile:

- *Configuration Page*
- *Low Level Page*
- *High Level Page*
- *Eye Monitor Page*

This section provides a brief overview of the LMH1297 GUI profile.

6.1 Configuration Page

The Configuration Page is the first page of the SigCon Architect LMH12097 GUI. In this page, the user can control the following:

- Change the Slave Address
- Toggle MSP430 LED
- Enable or Disable Demo Mode

Figure 16 shows the Configuration Page.

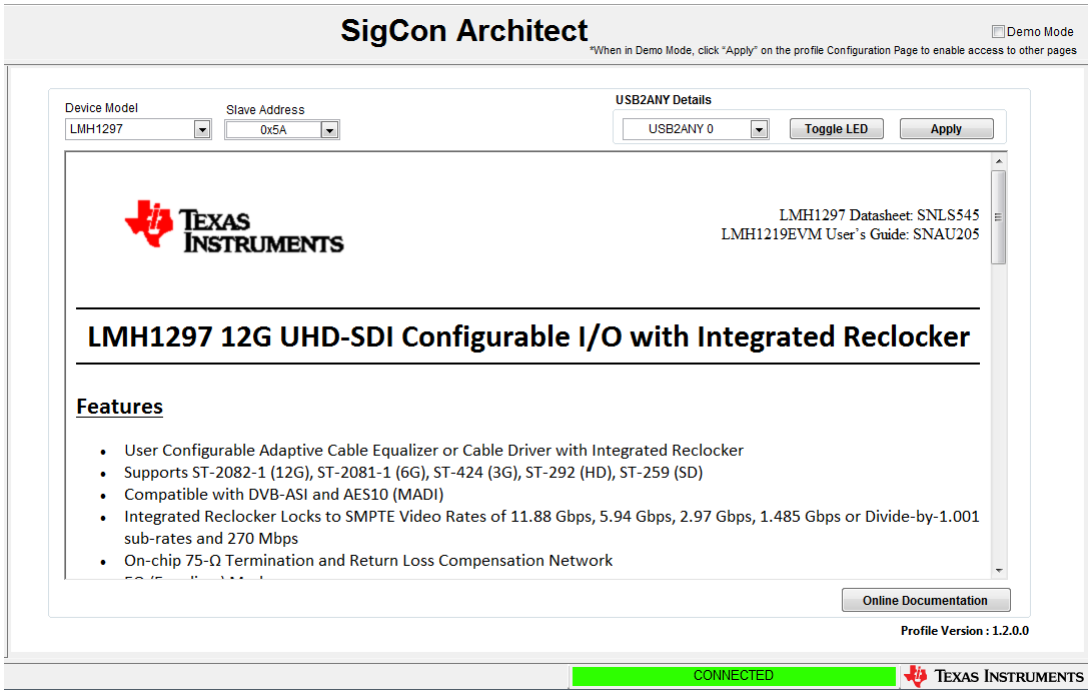

Figure 16. LMH1297EVM Configuration Page

To configure a live LMH1297 using the GUI, the following steps should be taken:

1. Connect the LMH1297EVM through a USB cable to the PC.
2. Select the USB2ANY Device in the *USB2ANY Details* drop-down menu.
3. Select the correct LMH1297 Slave Address (this can be verified and modified with J16 and J17).
4. Uncheck the Demo Mode Checkbox. Click *Apply*.
5. Verify that the status indicator at the bottom right of the GUI turns green and displays *CONNECTED*.

NOTE: In Demo Mode, the *Apply* button must still be clicked to unlock the Low Level, High Level, and Eye Monitor Pages of the GUI.

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6.2 Low Level Page

The Low Level Page allows the user to access the LMH1297 registers individually. This page is described in two main sections:

- *Register Map*
- *Field Description*

Figure 17 shows the Low Level Page.

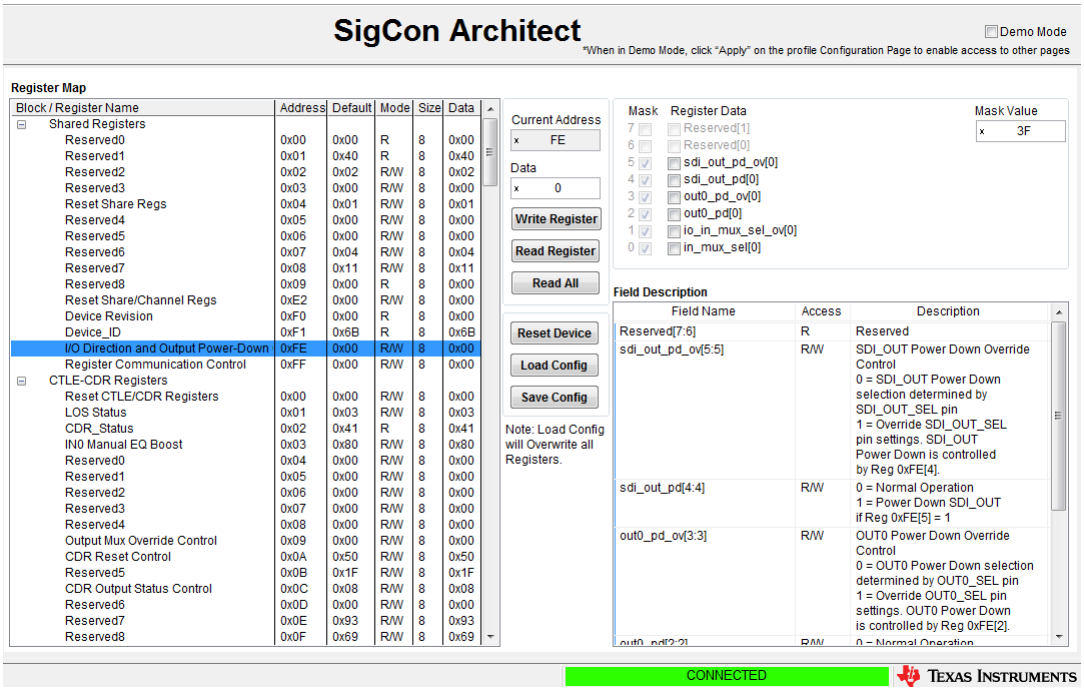

Figure 17. LMH1297EVM Low Level Page

6.2.1 Register Map

The *Register Map* section contains the three main register pages: Shared Registers, CTLE-CDR Registers, and Config IO Registers. Within these register pages, the following can be observed:

- Name of each register
- Each register's address and default value
- Register accessibility as read-only or read/write

The register value can be overwritten by typing the desired value in either the *Data* box or by clicking the appropriate checkboxes in the top right of the Low Level Page. Only bits that are read/write accessible can be modified.

6.2.2 Field Description

The *Field Description* section allows the user to view the detailed name, access type, and description for the register selected from the *Register Map* section.

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6.3 High Level Page

The High Level Page provides an intuitive control interface with a simplified block diagram of the LMH1297. This page is described in two main sections:

- *High Level Interface*
- *Macro Scripting Utility*

Figure 18 shows the High Level Page.

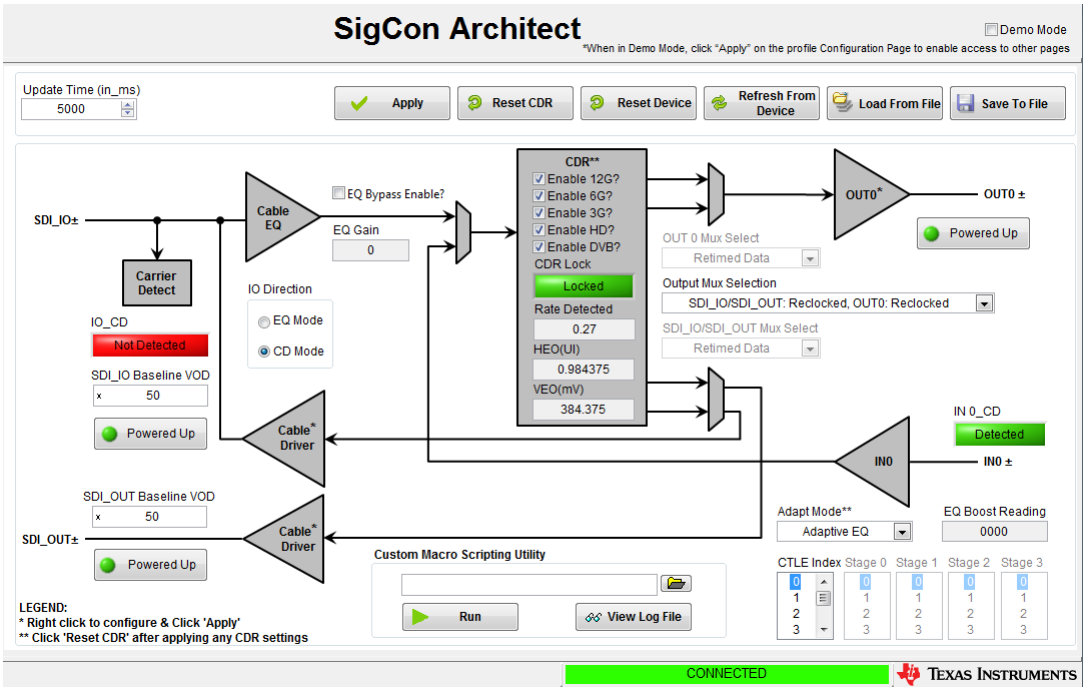

Figure 18. LMH1297EVM High Level Page

6.3.1 High Level Interface

This interface is dynamic and allows the user to view and control a variety of functions in the LMH1297 concurrently. In this page, the user can easily control functions such as the following:

- Configure the LMH1297 as CD or EQ Mode
- Power Up or Down Different Output Channels
- Modify the Signal Output from the Output Mux
- Reset the CDR
- Change the IN0 CTLE Index Boost Value

NOTE: Configuration pins **SDI_OUT_SEL**, **OUT0_SEL**, and **EQ_CD_SEL** will be overwritten with the default values displayed on the High Level Page when first loading SigCon Architect. These configuration pins are also overwritten by the High Level Page values any time the *Apply* button is clicked. By default, SDI_OUT_SEL is powered down, OUT0_SEL is powered up, and EQ_CD_SEL is set low (EQ Mode) by the GUI.

NOTE: Right-clicking the **Cable Driver** and **OUT0** blocks in the High Level Page enables a drop-down menu for the user to select additional output override options such as VOD amplitude, pre-emphasis, or de-emphasis controls.

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6.3.2 Macro Scripting Utility

The Macro Scripting Utility in the High Level Page allows the user to create and upload a text file (.txt extension) with instructions to write to multiple devices and registers simultaneously. After a macro file is uploaded and run, SigCon Architect generates a log file showing the device slave address, register address, data written, and data that is read back after each write. Figure 19 shows the required syntax for the macro scripts.

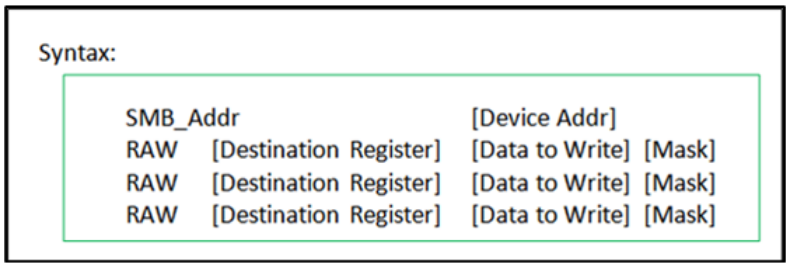

Figure 19. Macro Utility Syntax

NOTE: All parameters on the text file should be separated by a tab in order for the Macro utility to identify and accept the format.

Figure 10 shows an example of a macro script that programs two LMH1297 devices, one with SMBus Address 0x5C and another with SMBus Address 0x5A. After this file is saved as a .txt file, the user can run the macro by entering the appropriate file path in the *Custom Macro Scripting Utility* box. When ready, click *Run* to execute the script.

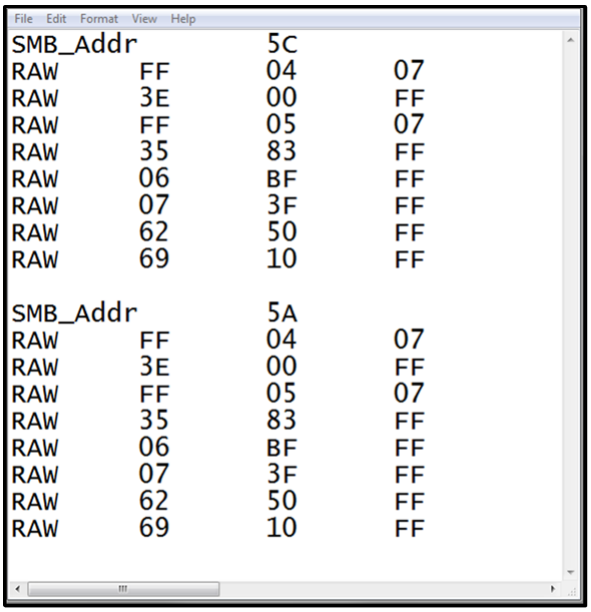

Figure 20. Macro Utility Example

After the script completes, the log file can be accessed by clicking *View Log File* and opening the appropriate log file .txt file. Figure 21 shows an example of a log file based on the macro utility example in Figure 20.

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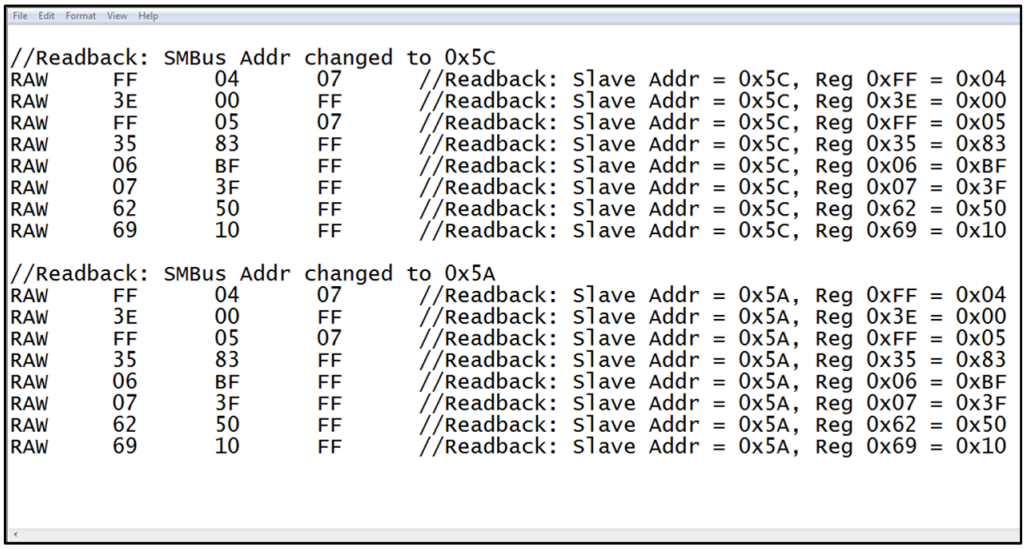

```
File  Edit  Format  View  Help

//Readback: SMBus Addr changed to 0x5C
RAW     FF      04      07      //Readback: Slave Addr = 0x5C, Reg 0xFF = 0x04
RAW     3E      00      FF      //Readback: Slave Addr = 0x5C, Reg 0x3E = 0x00
RAW     FF      05      07      //Readback: Slave Addr = 0x5C, Reg 0xFF = 0x05
RAW     35      83      FF      //Readback: Slave Addr = 0x5C, Reg 0x35 = 0x83
RAW     06      BF      FF      //Readback: Slave Addr = 0x5C, Reg 0x06 = 0xBF
RAW     07      3F      FF      //Readback: Slave Addr = 0x5C, Reg 0x07 = 0x3F
RAW     62      50      FF      //Readback: Slave Addr = 0x5C, Reg 0x62 = 0x50
RAW     69      10      FF      //Readback: Slave Addr = 0x5C, Reg 0x69 = 0x10

//Readback: SMBus Addr changed to 0x5A
RAW     FF      04      07      //Readback: Slave Addr = 0x5A, Reg 0xFF = 0x04
RAW     3E      00      FF      //Readback: Slave Addr = 0x5A, Reg 0x3E = 0x00
RAW     FF      05      07      //Readback: Slave Addr = 0x5A, Reg 0xFF = 0x05
RAW     35      83      FF      //Readback: Slave Addr = 0x5A, Reg 0x35 = 0x83
RAW     06      BF      FF      //Readback: Slave Addr = 0x5A, Reg 0x06 = 0xBF
RAW     07      3F      FF      //Readback: Slave Addr = 0x5A, Reg 0x07 = 0x3F
RAW     62      50      FF      //Readback: Slave Addr = 0x5A, Reg 0x62 = 0x50
RAW     69      10      FF      //Readback: Slave Addr = 0x5A, Reg 0x69 = 0x10
```

Figure 21. Macro Utility Example Log File

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6.4 Eye Monitor Page

The LMH1297 has on-chip eye monitor that can be accessed on the Eye Monitor Page. In this page, the user can control the following:

- Perform a single or continuous capture of the eye diagram
- Measure the HEO (Horizontal Eye Opening) in either time (ps) or unit intervals (UI)
- Measure the VEO (Vertical Eye Opening)
- Read back the detected data rate

Figure 22 shows the Eye Monitor Page.

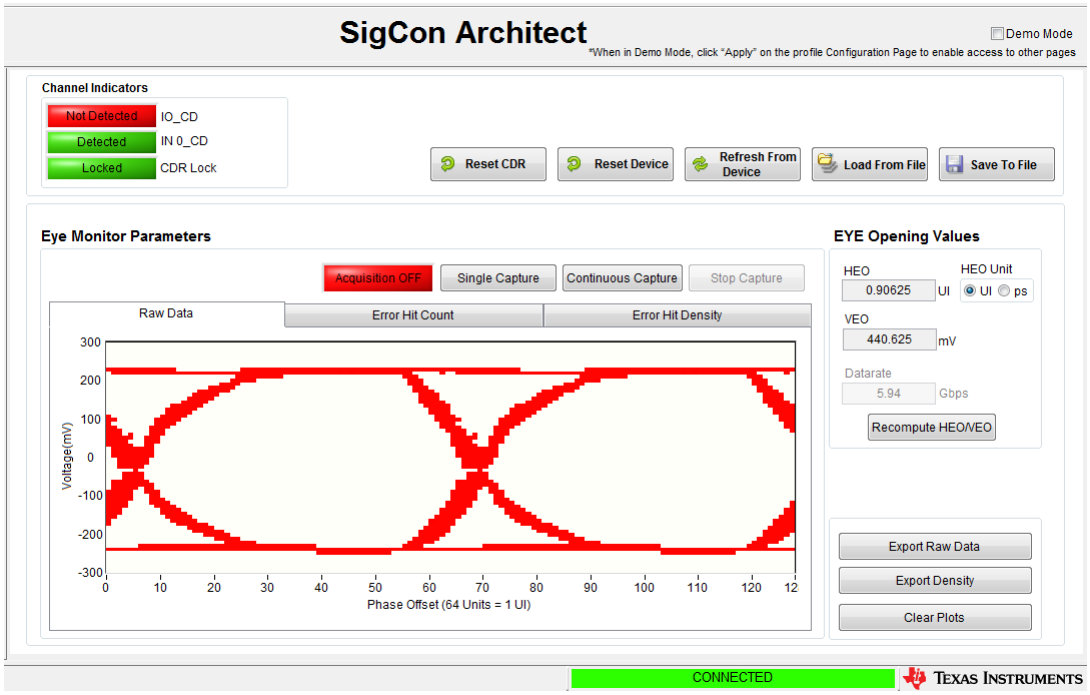

Figure 22. LMH1297EVM Eye Monitor Page

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7 Bill Of Materials

NO.	DESIGNATOR	QUANTITY	DESCRIPTION	MANUFACTURER	PART NUMBER
1	!PCB	1	Printed-Circuit Board	Any	SV601292
2	C1	1	CAP, CERM, 10uF, 16V, +/-20%, X5R, 0805	AVX	0805YD106MAT2A
3	C2, C3, C23	3	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0805, CAP, CERM, 1uF, 16V, +/-10%, X5R, 0805, CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0805	AVX	0805YD105KAT2A
4	C4. C5. C7	3	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X5R, 0402	TDK	C1005X5R0J104K050BA
5	C6	1	CAP, CERM, 1 µF, 6.3 V, +/- 20%, X5R, 0402	TDK	C1005X5R0J105M050BB
6	C10, C11, C12, C13, C14, C15, C16, C17	8	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0402	TDK	C1005X5R1A475K050BC
7	C21	1	CAP, CERM, 2.2uF, 16V, +/-10%, X5R, 0805	AVX	0805YD225KAT2A
8	C22	1	CAP, AL, 22 µF, 10 V, +/- 20%, ohm, SMD	Chemi-Con	EMVE100ADA220ME55G
9	C24	1	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0603	TDK	C1608X7R1H103K080AA
10	C25, C31, C32, C34	4	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
11	C26, C27	2	CAP, CERM, 220pF, 50V, +/-1%, C0G/NP0, 0603	AVX	06035A221FAT2A
12	C28, C29	2	CAP, CERM, 30pF, 100V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D
13	C30	1	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603X222K5RACTU
14	C33	1	CAP, CERM, 0.47uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A474KA61D
15	D1, D3	2	LED, Green, SMD	Lumex	SML-LX0603GW-TR
16	D2	1	Diode, Zener, 7.5 V, 550 mW, SMB	ON Semiconductor	1SMB5922BT3G
17	FB1	1	Ferrite Bead, 60 ohm @ 100 MHz, 0.8 A, 0603	Taiyo Yuden	BK1608HS600-T
18	FID1, FID2, FID3, FID4, FID5, FID6	6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
19	H1, H2, H3, H4, H5, H6	6	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fstener	NY PMS 440 0025 PH
20	H7, H8, H9, H10, H11, H12	6	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C
21	J1, J2, J3	3	Disconnect Terminal, 5.08mm, 2x1, Tin, TH	Keystone	1212-ST
22	J4, J6, J7	3	Header, 100mil, 2x1, Tin, TH	TE Connectivity	5-146278-2
23	J5	1	Header, 100mil, 3x1, Tin, TH	TE Connectivity	5-146278-3
24	J8	1	Header (shrouded), 100mil, 5x2, Gold, TH	TE Connectivity	5103308-1
25	J9	1	Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN
26	J10, J11, J12, J13, J14, J15, J16, J17, J18, J19	10	Header, 100mil, 3x2, Tin, TH	TE Connectivity	5-146254-3
27	J20, J21	2	Connector, BNC Edge Mount, SMD	Samtec	BNC7T-J-P-GN-ST-EM1D
28	J22, J23, J24, J25	4	Connector, TH, End launch SMA 50 ohm	Emerson Network Power	142-0771-821
29	J31	1	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2
30	J33	1	Header, 100mil, 2x2, Gold, TH	Samtec	TSW-102-07-G-D

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NO.	DESIGNATOR	QUANTITY	DESCRIPTION	MANUFACTURER	PART NUMBER
31	Q1	1	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	Fairchild Semiconductor	BSS138
32	R1, R2	2	RES, 2.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04022K00FKED
33	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R41, R42	20	RES, 1.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04021K00FKED
34	R21	1	RES, 220 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402220RJNED
35	R22, R23, R24	3	RES, 3.16k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04023K16FKED
36	R25, R26, R27	3	RES, 9.76k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04029K76FKED
37	R28, R29	2	RES, 75.0 ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040275R0FKED
38	R31, R32	2	RES, 33 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233R0JNED
39	R33	1	RES, 1.5 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED
40	R34, R36	2	RES, 33k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233K0JNED
41	R35	1	RES, 1.2Meg ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031M20JNEA
42	R37	1	RES, 200 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603200RFKEA
43	R43, R44, 445, R46, R47, R48, R49, R50, R51, R52	10	RES, 20.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040220K0FKED
44	S1	1	Switch, Tactile, SPST-NO, SMT	Panasonic	EVQ-PSD02K
45	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13	13	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA
46	U1	1	12G UHD Bidirectional I/O with Integrated Reclocker, RTV0032E	Texas Instruments	LMH1297RTV
47	U2	1	500mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low-Dropout Linear Regulator, DRB0008A	Texas Instruments	TPS73533DRBR
48	U3	1	ESD-Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85 degC, 6-pin SON (DRY), Green (RoHS & no Sb/Br)	Texas Instruments	TPD4E004DRYR
49	U4	1	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	Texas Instruments	MSP430F5529IPN
50	Y1	1	Crystal, 24.000MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR

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8 Schematics

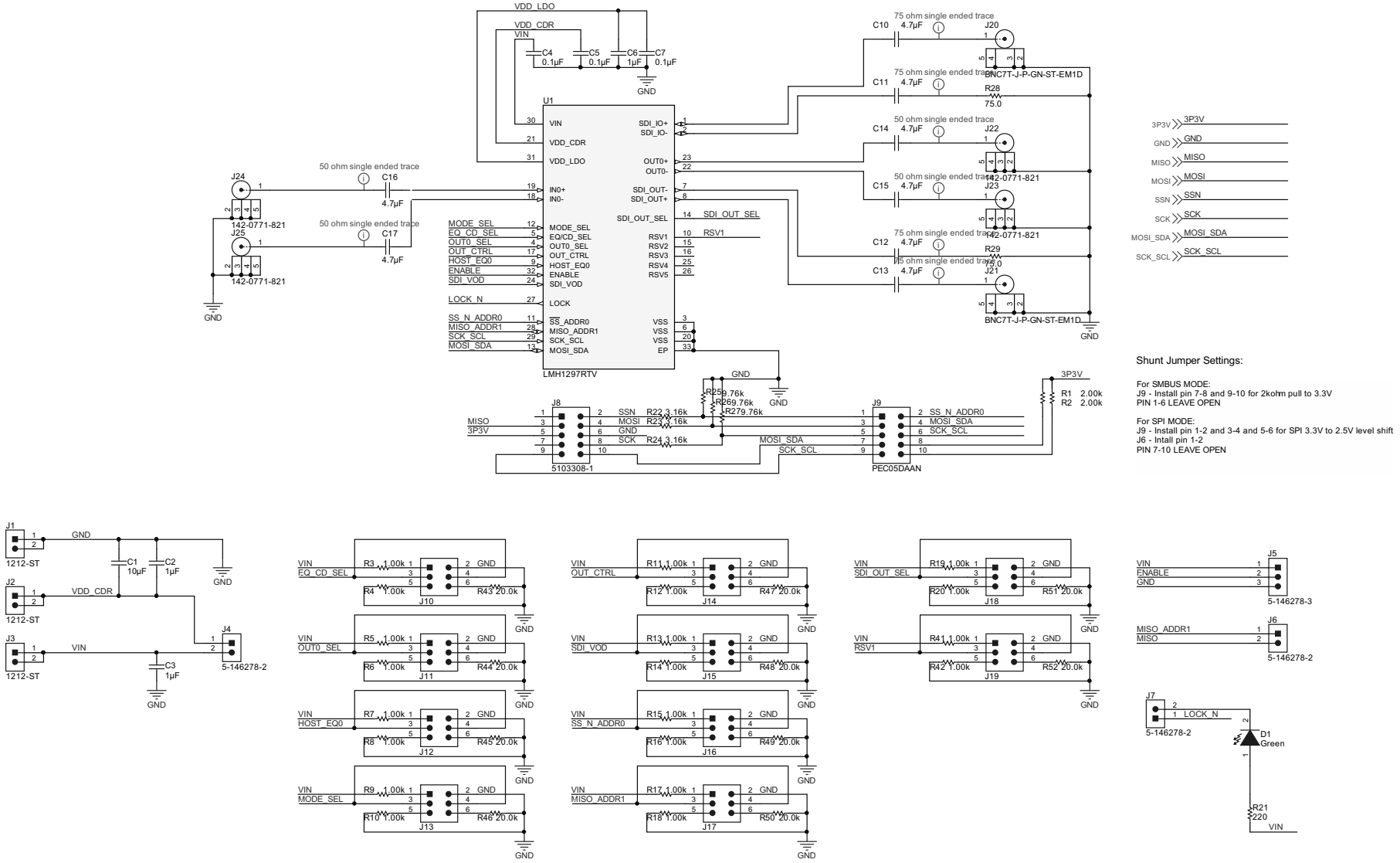

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Figure 23. LMH1297 Schematic Page

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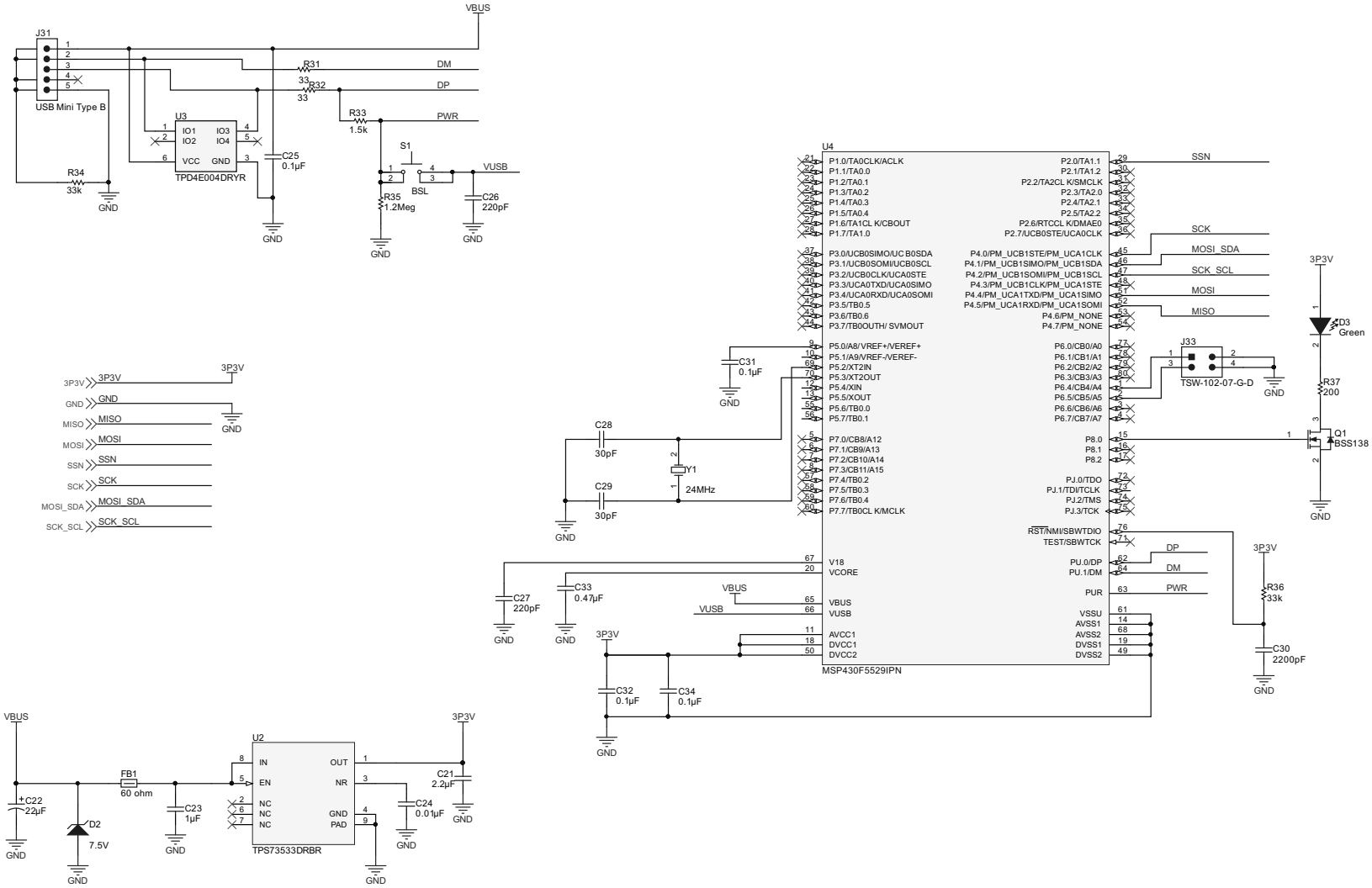

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Figure 24. MSP430 USB2ANY Schematic Page

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9 EVM Layout

The following figures show the LMH1297EVM layout. The evaluation board controls signal integrity control settings through jumper pins.

The LMH1297EVM allows access to all input channels (SDI_IO+ and IN0±) and output channels (SDI_IO+, OUT0±, and SDI_OUT+). It is very compact and low power. The QFN package offers an exposed thermal pad to enhance electrical and thermal performance. This must be soldered to the copper landing on the PWB.

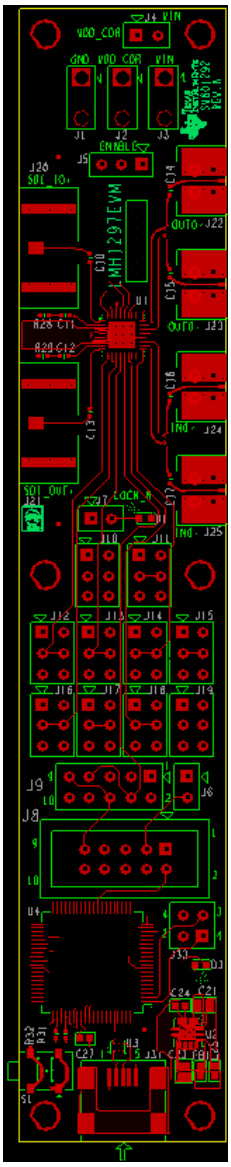

Figure 25. LMH1297EVM Top Layer

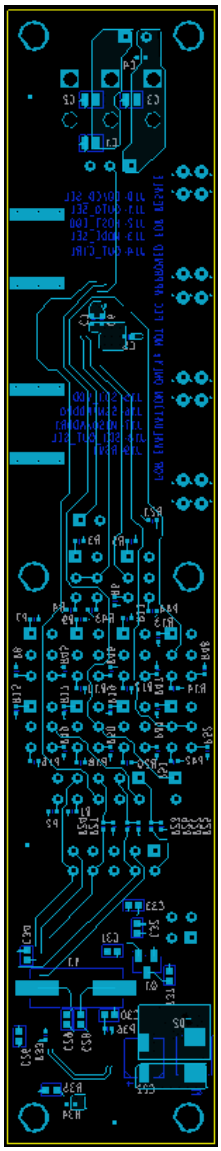

Figure 26. LMH1297EVM Bottom Layer

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2017) to A Revision	Page
• Initial Public Release	3

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