Simple Success with Conducted EMI and Radiated EMI for LMR160X0

Vincent Zhang

ABSTRACT

Electromagnetic Interference (EMI) is an unwanted effect between two electrical systems as a result of either electromagnetic radiation or electromagnetic conduction. EMI is the major adverse effect caused by the application of switch-mode power supplies (SMPS). In switching power supplies, EMI noise is unavoidable due to the switching actions of the semiconductor devices and resulting discontinuous currents. EMI control is one of the more difficult challenges in SMPS design, beyond functional issues, robustness, cost, thermal and space constraints.

First, this application note introduces the overview of LMR160X0 family products and conducted EMI knowledge. Second, step by step differential filter parameters design will be introduced to suppress conducted EMI noise. Third, a reference PCB layout based on LMR160X0 is presented. Finally, both conducted EMI and radiated EMI test with and without input filter were provided and compared to verify the theories. This approach also could be applied to the LMR140X0 family.

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1 LMR16010/20/30 Introduction

The SIMPLE SWITCHER® LMR160X0 non-synchronous buck converter family is an easy to use step-down DC-DC converter capable of delivering up to 3 A of load current from an input of up to 60 V. This family features wide input voltage range, low external component count, low quiescent current, adjustable switching frequency, power good flag, precision enable, adjustable soft-start, PFM at light load, UVLO, over current protection and over temperature protection. It provides flexible and easy to use solutions for a wide range of applications. The devices in this family are available in an SOIC-8 package and are pin-to-pin compatible to each other. The pin configuration is shown in Figure 1.
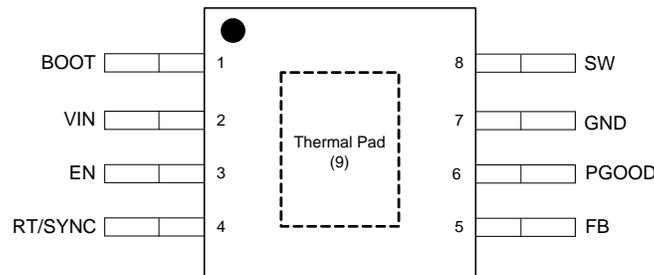
Figure 1. Pin Configuration for LMR160X0

2 Conducted EMI Introduction and Mitigation Technique

Conducted EMI arises from the normal operation of switching circuits. The ON and OFF actions of the power switches generate large discontinuous currents. The discontinuous currents are present at the input side of buck converters, the output side of boost converters and at both input and output ports of flyback and buck-boost topologies. Voltage ripple generated by discontinuous currents can be conducted to other systems via physical contact of the conductors. Without control, excessive input and/or output voltage ripple can compromise operation of the source, load or adjacent system. The discontinuous currents at the input port of a converter need to be filtered by an input filter to smooth out the voltage perturbations leading to the source. Meanwhile, the output side is usually well filtered by the existing output filter of the converter. Proper application of filtering leads to meeting regulatory requirements that allow the end product to be sellable in the marketplace.

Conducted EMI involves the normal operation of DC-DC converters. It does not involve circuit parasitic except input or output capacitor ESR and ESL. PCB layout itself is not going to help reduce conducted EMI. Further, conducted EMI is only related to the current level, not the voltage level at input or output ports. In another words, with the same power level buck converter, lower input voltage means higher input current, thus worse input conducted EMI.

The input port EMI noise comes from voltage ripple generated by the discontinuous current on the input capacitors. The fundamental frequency of the voltage ripple is the switching frequency of the converter. Higher order harmonics of the fundamental frequency also exist in the noise spectrum. Figure 2 represents a typical conducted differential-mode EMI plot of LMR16030 (24 V input 5 V / 3 A output) prior to the addition of the EMI filter. Note that the fundamental switching frequency and several harmonics extend above the regulatory limits. The height of the fundamental above the target limit line establishes the required additional filter attenuation needed in order to comply with the desired limit. Also note that from the standpoint of regulatory test requirements, the measurement frequency span extends from 150 kHz up to 30 MHz. However, there may be system requirements above the frequency range of the regulatory spec that fall into the scope of the SMPS input filter. These system requirements should also be considered and evaluated. It has been observed that keeping the conducted differential EMI performance in check above 30 MHz will assist in meeting the separately tested radiated EMI requirements.
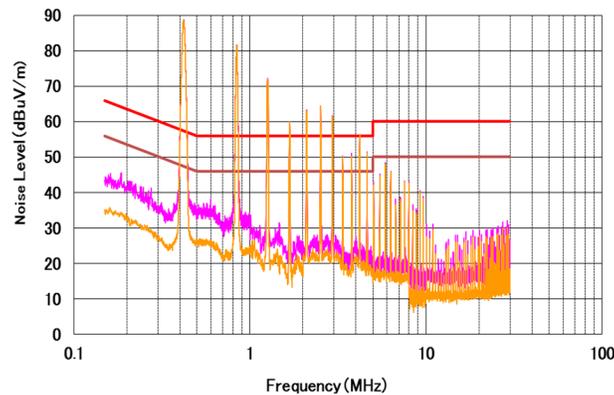
Figure 2. Conducted EMI Measurement Without Filter

Figure 3 shows the conventional circuit configuration with a DC power source, the LC EMI filter and the target SMPS. Note the EMI filter configuration is actually from the right to the left. In other words the filter "ac input" is V_B and the filter "ac output" is V_A. Filter design is accomplished by choosing the inductor L_f and the capacitor C_f.
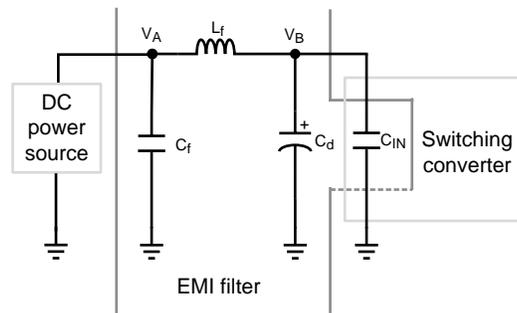
Figure 3. Simplified Schematic For Differential Mode EMI Filter Design

The typical procedure for designing a differential mode input filter for a Buck or Buck-Boost converter is summarized below:

2.1 Calculate the Required Attenuation

Identify noise level at the switching frequency. Figure 2 shows the most significant noise magnitude appearing at the switching frequency. The required attenuation is the difference between the nonfiltered noise level and the governing EMI standard requirement at the switching frequency. The low pass filter provides even greater attenuation for the higher order harmonics of the switching frequency. The switching frequency attenuation is the worst case condition and is the focus of the filter design. The typical procedure is to measure the EMI peak level without added filters under worst case operation (highest input current.) The difference between the noise level at the fundamental switching frequency and the required level defined in the appropriate standard for the target market place.

In this case, in order to pass CISPR 22 Class B requirement, the $|Att|_{dB}$ = 45 dBuV/m.

2.2 Inductor Selection: Lf

The inductor defines the resonant frequency of the EMI filter hence its value (Lf) is usually in the range of 1 µH to 20 µH for low and medium power applications. Choose the highest value in compliance with amperage and physical size requirements. In this case choose 1234AS-H-120M (12 µH, 1 A, 0.19 ohm).

2.3 Calculate Filter Capacitance: Cf

Pick the higher value determined by the following two formulas:

$$C_{fa} = \frac{C_{IN}}{C_{IN}L_f(2\pi f_s/10)^2 - 1}$$

(1)

$$C_{fb} = \frac{1}{L_f}\left(\frac{10^{|Att|_{dB}/40}}{2\pi f_s}\right)^2$$

(2)

Where f_s is the switching frequency of the converter.

The first formula ensures that the resonance frequency of the EMI input filter is at least one decade below the switching frequency. The second formula is derived from an approximation that ensures proper attenuation of the EMI filter. Select the higher value of C_{fa} and C_{fb} because both conditions must be met.

In this case f_s = 420 kHz, C_{IN} = 9.62 µF. C_{fa} = 1.37 µF, C_{fb} = 2.1 µF. Choose C_f = 4.7 µF // 0.22 µF.

2.4 Calculate Damping Capacitance Cd

Addition of an input filter to a switching regulator leads to a modified control-to-output transfer function. The output impedance of the filter must be sufficiently small at point VB so that input filter does not significantly affect the loop gain of the SMPS. The peak of the impedance at the filter's resonance corner frequency is largely dependent on the filter LC parasitic. Added damping is needed when the output impedance is very high at the resonant frequency (that is, Q of filter formed by C_{IN} and L_f is too high).

An electrolytic cap Cd can be used as damping device, with value Cd> = 4 x C_{IN}. In this case, in order to reduce the cost, no electrolytic is used.

2.5 Schematic of LMR160X0 Board and Conducted EMI Test Results

This application note use LMR160X0 reference design board as example to verify the differential EMI filter design. Test Condition is: V_{IN} = 24 V, V_o = 5 V, I_o = 3 A.

Figure 4 and Figure 5 shows detail differential EMI filter and schematic parameters. Figure 6 shows the conducted EMI results with differential EMI Filter. It could be observed that with differential EMI filter, the noise of fundamental frequency and harmonics could be well suppressed.
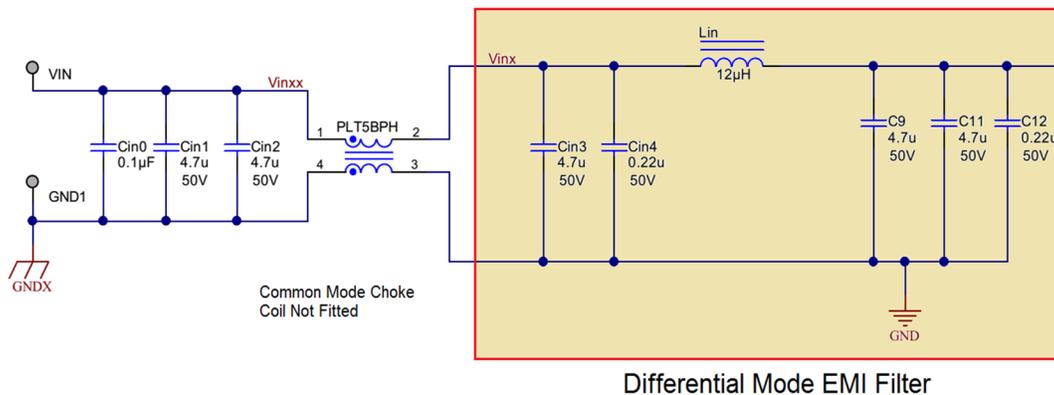
Figure 4. Input EMI Filter Parameters
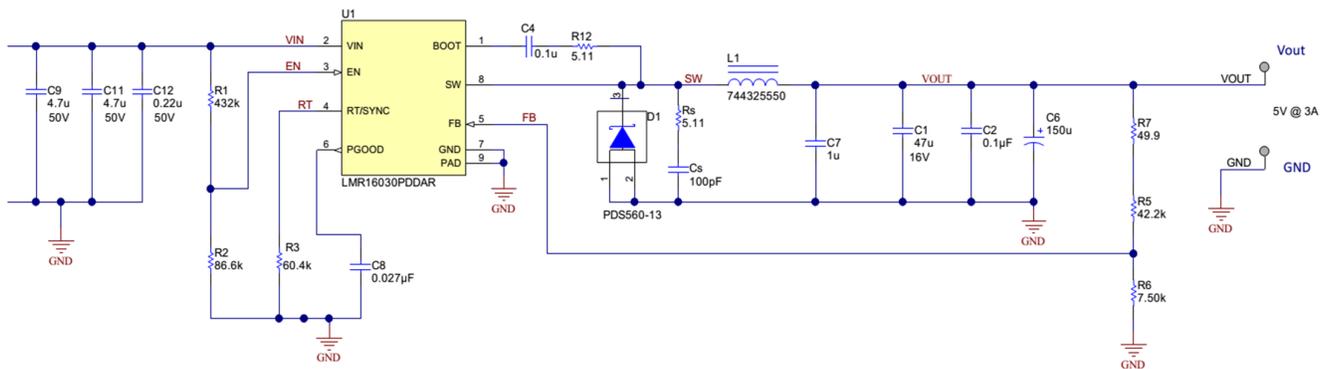
Figure 5. Schematic Parameters for LMR160X0 Board
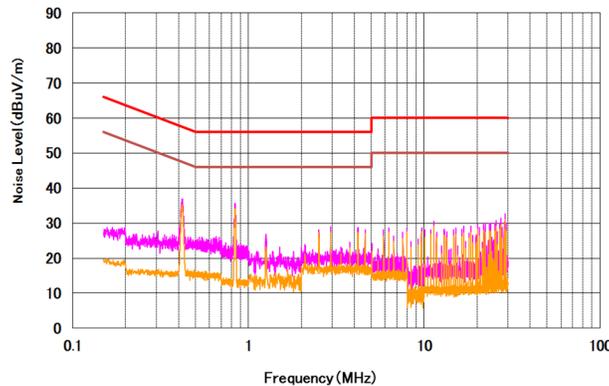
Figure 6. Conducted EMI Measurement With Differential EMI Filter

3   Buck Converter Layout Considerations for Radiated EMI

Board layout is a critical aspect of SMPS design. The performance of an SMPS could be degraded by a poorly designed PCB. Even worse, a bad PCB layout may result in a malfunctioned converter. Due to the switching action in SMPS, large currents with fast transitions exist in the circuit. A current has to circulate through a loop and return to the source. If current transitions exist in a current loop, voltage spikes are going to be generated, $V = L \times (di/dt)$, where L is the self-inductance of the current loop and di/dt is the current transition rate. The self-inductance of a current loop is proportional to the area enclosed by it. The loops containing high di/dt current are the critical paths in SMPS PCB design. To reduce the voltage spikes and switching noises in an SMPS, the critical high di/dt paths should be identified and the area enclosed by them should be minimized.

3.1   Identify Critical Paths

The first step is to identify the critical paths in an SMPS.
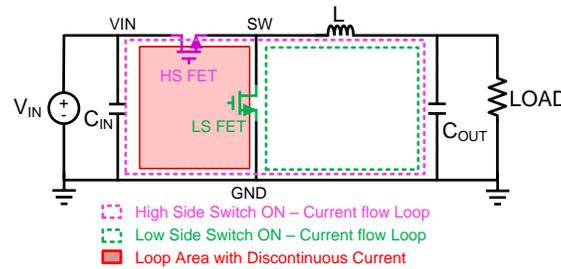
Figure 7. Simplified Buck Converter Schematic

Figure 7 shows a simplified buck converter schematic. The large current high di/dt loop in this topology is formed by the input capacitor, the high side switch and low side switches. This loop can be identified by looking at the current flow when the high side switch (HS FET) or the low side switch (LS FET) is ON. The critical path with high di/dt current is shown in solid red. The area of the red loop should be minimized by component placement and PCB layout. This is the most important high di/dt loop in a buck converter, due to large current level.

3.2 Minimize High Power High di/dt Path Loop Area

Figure 8 shows conceptually how to minimize the critical path loop area in a buck converter.
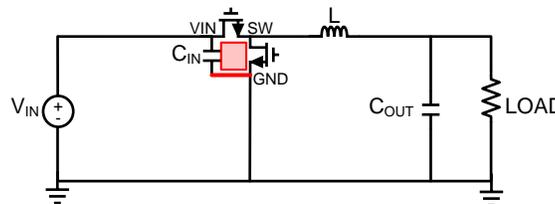
Figure 8. Simplified Buck Converter Schematic illustrating Minimized Loop Area

The high side FET, the low side FET and the input high frequency bypass capacitor should be placed as close as possible to each other. Then, the bypass capacitors should be placed as close as possible to the IC, between the VIN and GND pins. This makes the placement of the input capacitor very easy and results in minimum area of the high di/dt loop. The copper traces connecting to the bypass capacitors contain high di/dt currents. They should be short and wide traces on the same layer as the converter IC, to avoid spreading high frequency noises to other layers or planes. Avoid routing high di/dt current traces through power or ground planes. Avoid using thin and long traces and/or vias in the connecting traces to the bypass capacitors. Parasitic inductances of the traces and vias will make the high frequency bypass ineffective. It is recommended to use short and wide traces. If vias have to be used, place multiple vias in parallel to minimize the added inductance.

3.3 Ground Shielding

Better EMI results can be achieved by adding an unbroken ground plane as a middle layer in the PCB. If the IC is placed on the top layer and the high di/dt paths are routed on the top layer, the ground plane at the mid-layer allows a mirror return current to be formed right underneath a top layer current. The mirror current path minimizes the current loop area and the magnetic field generated by the two opposite direction currents will be almost canceled.

3.4 Layout and Radiated Emission Test Results of the LMR160X0

Figure 9 shows the top layer and mid-layer of LMR160X0 PCB layout. In this case, we make Input GND-HS switch-Diode-Output GND loop as small as possible, also add unbroken ground in the middle layer to improve the EMI performance.

(a) Top Layer   (b) Middle Layer
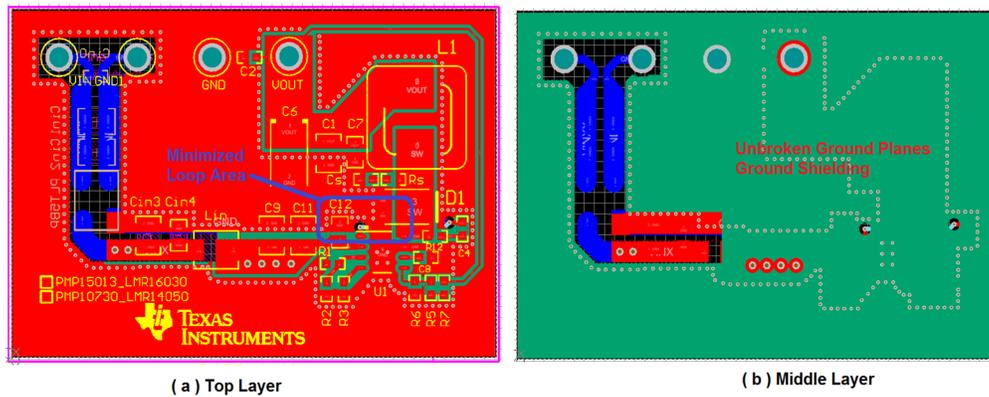
Figure 9. LMR160X0 EMI Reference Design PCB Layout

Figure 10 shows the radiated horizontal and vertical EMI results of LMR160X0. With optimized differential EMI parameters and PCB layout, it could pass CISPR 22 Class B requirement with 10dB margin.
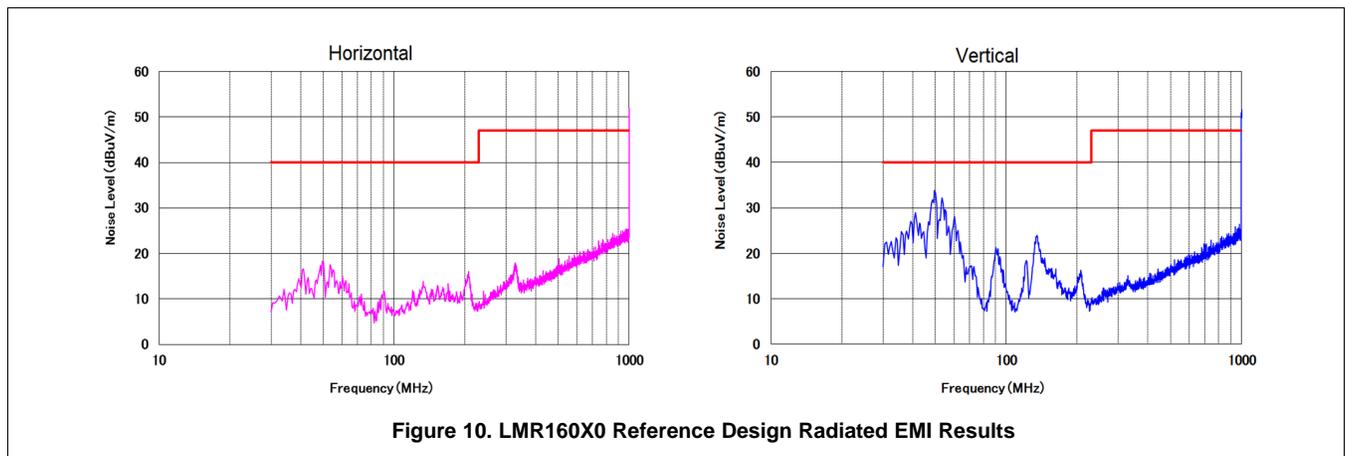
Figure 10. LMR160X0 Reference Design Radiated EMI Results

4 Conclusion

EMI is an unwanted effect between two electrical systems as a result of either electromagnetic radiation or electromagnetic conduction. Adding differential mode EMI filters and optimizing the PCB layout could both improve conducted EMI and radiated EMI performance. This apps note introduces the differential filter design and procedure and minimized loop area PCB layout based on LMR160X0. The conducted and radiated EMI results with and without differential filter verified the theories.

5 References

1. SNVA721 *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*.
1. *AN-2162 Simple Success with Conducted EMI From DC-DC Converters*.

IMPORTANT NOTICE

Products		Applications	
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