Application Report
SPRA941 – August 2003

MPEG-2 Loopback on the DM642 EVM

Video and Imaging Systems

ABSTRACT

The software demonstrates the D1 MPEG-2 encoder and decoder running back-to-back on a DM642 Evaluation Module (EVM). The demonstration encodes the captured frames and then decodes the generated MPEG-2 bitstream to display the decoded frames.

The demonstration uses:

- MPEG-2 encoder library optimized for a DM642 EVM
- MPEG-2 decoder library optimized for a DM642 EVM
- MPEG-2 encoder and decoder library implemented using XDAIS interfaces
- Sample integration of the MPEG-2 encoder and decoder library using RF-5 framework

Contents

Figures

Software Architecture/Data Flow

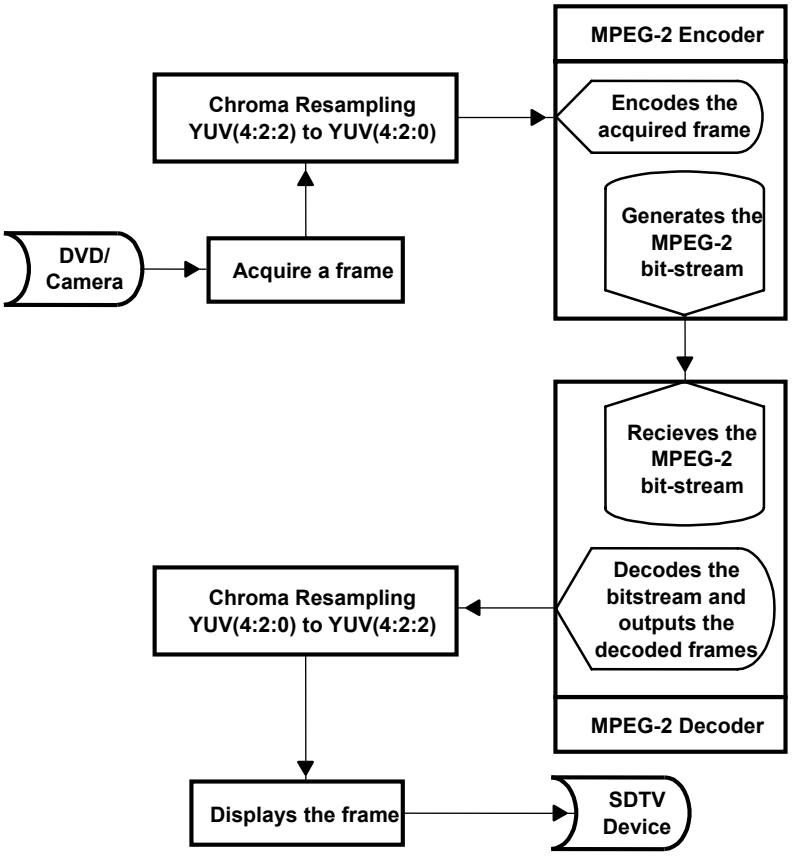

Figure 1. Data Flow Diagram

The data flow in the demonstration follows this sequence:

1. A frame is captured from the input source (DVD/camera), and the acquired frame data, in YUV 4:2:2 format, is resampled to YUV 4:2:0 format.
2. The frame is fed to the MPEG-2 encoder library.
3. The MPEG-2 encoder encodes the input frame and outputs the coded bit-stream.
4. The generated MPEG-2 bit-stream is passed to the MPEG-2 decoder module.
5. The MPEG-2 decoder module decodes the MPEG-2 bit-stream and outputs the decoded frames. The decoded frames received from MPEG-2 decoder module are in YUV 4:2:0 format and are resampled to YUV 4:2:2 format.
6. The frame is then displayed on the output device (SDTV).

Framework Flowchart

This demonstration uses RF-5 framework to integrate the MPEG-2 encoder and decoder library, and it uses a three-task model. Before coming to the DSP BIOS™ task scheduler, the demonstration code initializes various modules used in the system. These include:

- Board and processor
  - The system performs DSP BIOS™ initialization and CSL initialization.
  - The L2 cache mode is set to 64K cache.
  - EMIFA CE0 and EMIF CE1 spaces are enabled for caching.
  - The DMA priority queue lengths are set to maximum.
  - Priority for L2 request is set as high.
- RF- 5 modules
  - The system initializes the channel module of RF-5.
  - The system initializes the ICC and SCOM modules of RF-5 required for intercell communication and messaging.
  - Channel setup is performed with the internal, external, and scratch heap buffers.
- Capture and display channels
  - An instance of capture channel is created and started.
  - An instance of display channel is created and started.
- Algorithm instances
  - The MPEG-2 encoder cell is created and registered in the channel.
  - The MPEG-2 decoder cell is created and registered in the channel.
  - The channel is opened, which leads to creation of the instances of the encoder and decoder cells.

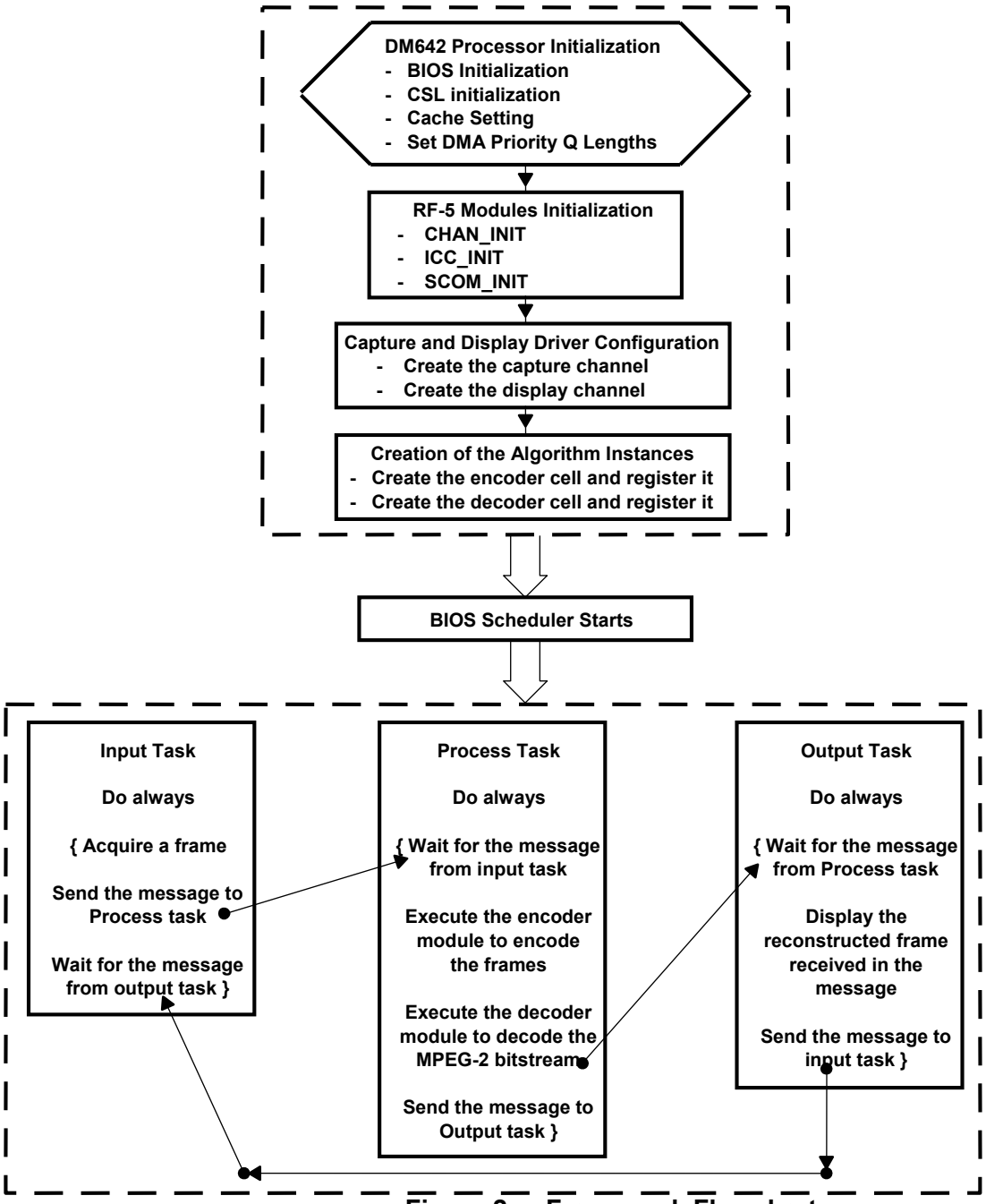

Figure 2. Framework Flowchart

After the initializations, the system enters the three-task system managed by the DSP BIOS™ scheduler. These three tasks use the SCOM module of RF-5 to communicate with each other:

- Input task

  The input task is responsible for acquiring the frames from the NTSC input device. It uses FVID_exchange calls provided by the driver to acquire a frame. The acquired frame is in YUV 4:2:2 format and is resampled to YUV 4:2:0. It then sends the message to the process

task with the frame pointer embedded in the message. The task then waits for the message from the output task to continue.

- Process task

  The process task is responsible for encoding the frame, passing the bitstream to the decoder module, decoding the frame, and then passing in on to the output task. The process task achieves the loopback by executing the RF-5 channel. The RF-5 channel has both encoder and decoder cells registered in it. The ICC module manages the passing of the bitstream generated by the encoder cell to the decoder cell. The task waits until it receives the message, with input frame, from the input task.

  The RF-5 channel in the demonstration code consists of a MPEG-2 encoder cell and a MPEG-2 decoder cell. During the channel execution, first the MPEG-2 encoder cell executes and generates the bitstream. The generated bitstream is passed to the MPEG-2 decoder cell and then the decoder cell executes to produce the decoded frames. It then sends a message to the output task, with the decoded frame pointers embedded in the message. The task then waits for the message from the input task to continue.

- Output task

  The output task is responsible for displaying the frames on the NTSC output device. It uses FVID_exchange calls provided by driver to display a frame. The acquired frame is in YUV 4:2:0 format and is resampled to YUV 4:2:2 format. It then sends the message to the input task to continue. The task then waits for a message from the process task to continue.

System Requirements/Configuration

Software Requirements

- Microsoft Windows NT (SP6)/Microsoft Windows 2000 (SP1 and SP2)
- Code Composer Studio™ Integrated Development Environment (IDE) version 2.20.18
- Driver software (DDK 1.1)

Hardware Requirements

- Pentium machines with 450 MHz, 64MB RAM (minimum)
- DM642 EVM
- NTSC TV for display purposes
- Camera/DVD for NTSC capture purposes
- XDS 510/560 emulator

Hardware Setup

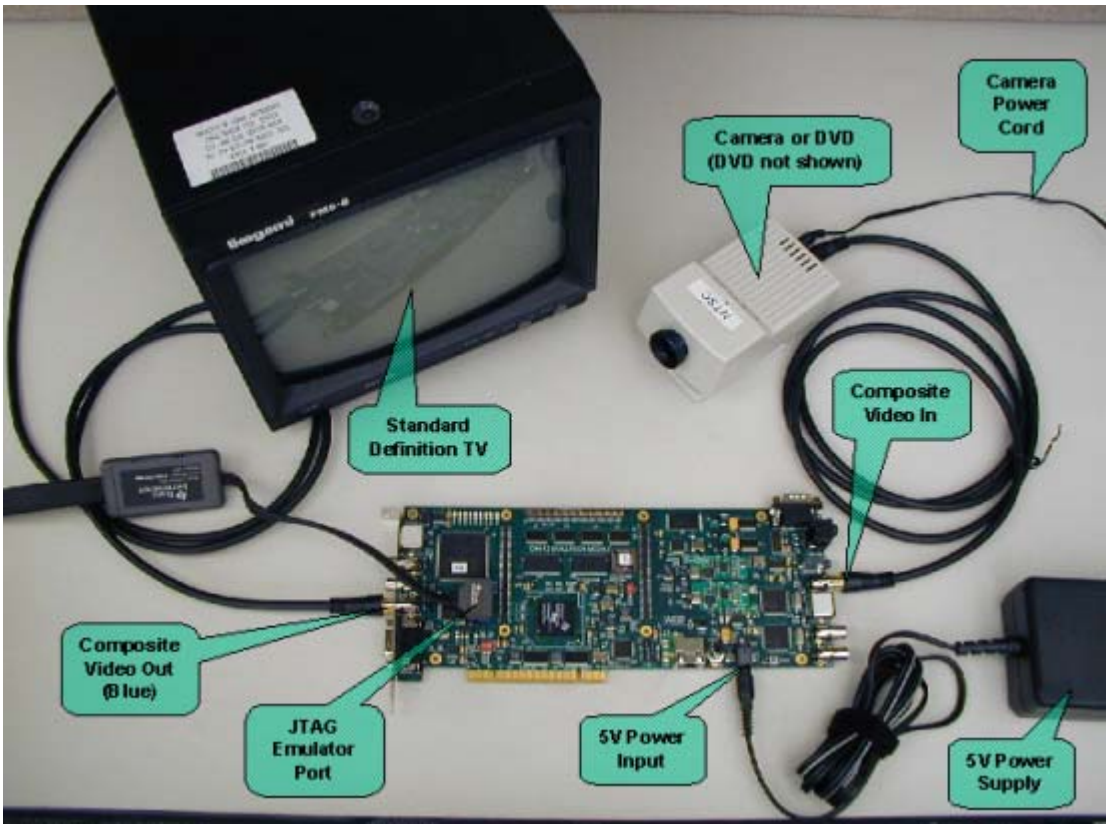

Figure 3. Hardware Setup

To run the demonstration, the hardware must be set up properly, as shown in Figure 3.

- The XDS510/560 emulator must be connected to JTAG pins to download the demonstration code to the board and control it from Code Composer Studio™ IDE.
- The input video port (for composite video) must be connected to the NTSC input source (DVD/camera) using RCA cable.
- The output video port (for composite video) must be connected to the NTSC output device (SDTV) using RCA cable.
- The DM642 EVM must be connected to the appropriate power source.

Demonstration Execution

To run the demonstration:

1. Set up the hardware.
2. Power up the DM642 EVM board.
3. Start Code Composer Studio™ IDE version 2.20.18.

4. Check the color bar on the output device.
5. Go to the bin folder under the MPEG2_loopback directory and load .out.
6. Ensure the presence of the encoder parameter file (test.par) in the same directory as the .out
7. Retain the name of the parameter as test.par, as this is hard-coded in the code. You can make the desired changes inside the parameter file with the restrictions as suggested in the *Known Constraints* section.
8. Once the program is loaded, go to the Debug Menu and press the Run option (F5).
9. On the output screen, watch the output frames from the MPEG-2 encoder/decoder loopback, with the TI logo on the top-right corner of the frames.

Demonstration Code and Build Procedure

The demonstration code for MPEG-2 loopback is located in evmdm642\examples\video\MPEG2_loopback directory.

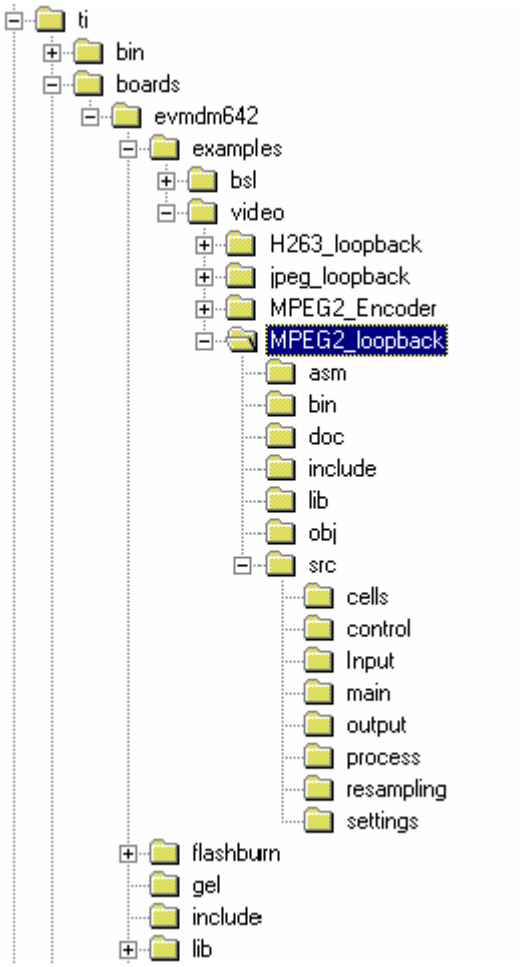

Figure 4. Directory Structure for MPEG2_loopback

Build Procedure

1. Start Code Composer Studio™ IDE version 2.20.18
2. Open the MPEG-2 loopback project (mpeg2loopback_dm642.pjt) from the examples\video\MPEG2_loopback folder.
3. Go to Project->Build Options->Compiler->Preprocessor and define the symbols as required for appropriate demonstration setup.

   Default options: The following must always be defined for proper compilation of the demonstration.

   _NTSC and CHIP_DM642
4. If the C_DIR is not defined or the DDK package has been installed outside the Code Composer Studio™ IDE folder, modify the include paths to point to the appropriate <ccs install dir>\ti\… paths in the project build options. If the C_DIR is defined properly there is no need to modify the include paths.
5. Build the project and load the executable mpeg2loopback_dm642.out build in the examples\video\MPEG2_loopback\ bin directory.
6. Before running the executable, make sure the input (camera/DVD) and output (SDTV) are connected correctly. For all input purposes and for SDTV output purposes, RCA cables must be used.
7. Press F5 to watch the output frames from the MPEG-2 encoder, decoder loopback, with the TI logo on the top-right corner of the frames.

Known Constraints

The MPEG2 libraries in the project have been compiled to work in conformance with the main profile @ main level (MP@ML), as suggested in ISO/IEC document 13818-2:1995.

The encoder parameters in the test.par file can be modified with a few restrictions, as described below.

Options that are highlighted in bold italics can be changed according to the input and computation bandwidth available. All other parameters are either fixed or not fully tested.

```
- /* name of source files. */
- /* name of reconstructed images ("-": don't store) */
- /* name of intra quant matrix file ("-": default matrix) */
- /* name of non intra quant matrix file ("-": default matrix) */
- /* name of statistics file ("-": stdout ) */
1 /* i /* input picture file format: 0=*.Y,*.U,*.V, 1=*.yuv, 2=*.ppm */
1024 /* number of frames */
0 /* number of first frame */
00:00:00:00 /* timecode of first frame */
15 /* N (# of frames in GOP) */
1  /* M (I/P frame distance) */
0 /* ISO/IEC 11172-2 stream */
0 /* 0:frame pictures, 1:field pictures */
720 /* horizontal_size */
480 /* vertical_size */
2 /* aspect_ratio_information 1=square pel, 2=4:3, 3=16:9, 4=2.11:1 */
5 /* frame_rate_code 1=23.976, 2=24, 3=25, 4=29.97, 5=30 frames/sec. */
8000000.0 /* bit_rate (bits/s) */
112 /* vbv_buffer_size (in multiples of 16 kbit) */
0 /* low_delay */
0 /* constrained_parameters_flag */
4 /* Profile ID: Simple = 5, Main = 4, SNR = 3, Spatial = 2, High = 1 */
8 /* Level ID: Low = 10, Main = 8, High 1440 = 6, High = 4 */
0 /* progressive_sequence */
1 /* chroma_format: 1=4:2:0, 2=4:2:2, 3=4:4:4 */
2 /* video_format: 0=comp., 1=PAL, 2=NTSC, 3=SECAM, 4=MAC, 5=unspec */
5 /* color_primaries */
5 /* transfer_characteristics */
4 /* matrix_coefficients */
720 /* display_horizontal_size */
480 /* display_vertical_size */
0 /* intra_dc_precision (0: 8 bit, 1: 9 bit, 2: 10 bit, 3: 11 bit */
1 /* top_field_first */
0 0 0 /* frame_pred_frame_dct (I P B) */
0 0 0 /* concealment_motion_vectors (I P B) */
1 1 1 /* q_scale_type (I P B) */
1 0 0 /* intra_vlc_format (I P B)*/
0 0 0 /* alternate_scan (I P B) */
0 /* repeat_first_field */
0 /* progressive_frame */
0 /* P distance between complete intra slice refresh */
0 /* rate control: r (reaction parameter) */
0 /* rate control: avg_act (initial average activity) */
0 /* rate control: Xi (initial I frame global complexity measure) */
0 /* rate control: Xp (initial P frame global complexity measure) */
0 /* rate control: Xb (initial B frame global complexity measure) */
0 /* rate control: d0i (initial I frame virtual buffer fullness) */
0 /* rate control: d0p (initial P frame virtual buffer fullness) */
0 /* rate control: d0b (initial B frame virtual buffer fullness) */
6 5 63 63 /* P: forw_hor_f_code forw_vert_f_code search_width/height */
4 4 15 15 /* B1: forw_hor_f_code forw_vert_f_code search_width/height */
5 5 31 31 /* B1: back_hor_f_code back_vert_f_code search_width/height */
5 5 31 31 /* B2: forw_hor_f_code forw_vert_f_code search_width/height */
4 4 15 15 /* B2: back_hor_f_code back_vert_f_code search_width/height */
```

Figure 5. MPEG-2 Encoder Parameter File

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