# Interfacing an LCD Controller to a DM642 Video Port

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**ABSTRACT**

There is an increasing demand to bring video and image processing capabilities to devices like video IP phones, cellular phones, and personal data assistants (PDAs). The images are brought to the user on liquid crystal displays that usually use thin film transistor (TFT) technology. These LCD devices require very specific timings and row/column formatting that can make them difficult to directly interface. For this reason, we recommend that you use an LCD controller. Most LCD controllers require little more input than raw RGB data. Some require horizontal and vertical sync signals, while others remove even that need. LCD controllers take care of any timing requirements and row/column formatting.

With their ability to output raw RGB data and horizontal/vertical sync signals, the DM642's video ports have the necessary functionality to seamlessly interface to TFT LCD controllers. Therefore, we have decided to show how to interface the DM642's video ports to an LCD controller, instead of directly to an LCD module. This application report details how to program the DM642's video ports to meet LCD controller requirements.

Specific examples will be provided using the ***NEC S1L50282F23K100*** LCD controller interfacing to the ***NEC NL2432HC22-22A*** LCD module. Hardware schematics and software driver collateral is also included. Project collateral discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SPRA975.

**Contents**



**List of Figures**

**List of Tables**



# 1 Introduction

This application report describes how to connect an LCD controller to a DM642 video port. The design consists of an NEC S1L50282F23K100 LCD controller. We also use an NEC NL2432HC22-22A LCD module that interfaces to the controller only, not the DM642. The S1L50282F23K100 has an 18-bit digital RGB interface which can provide a target resolution in landscape or portrait of 240x320 or 320x240, respectively. The NL2432HC22-22A is an amorphous silicon transflective TFT LCD display which supports 262,144 colors at a resolution of 320x240.

# 2 Design Specifications

The architecture used to interface the video port and the S1L50282F23K100 is shown in the diagram below. We have added the NL2432HC22-22A into the diagram as well for completeness.

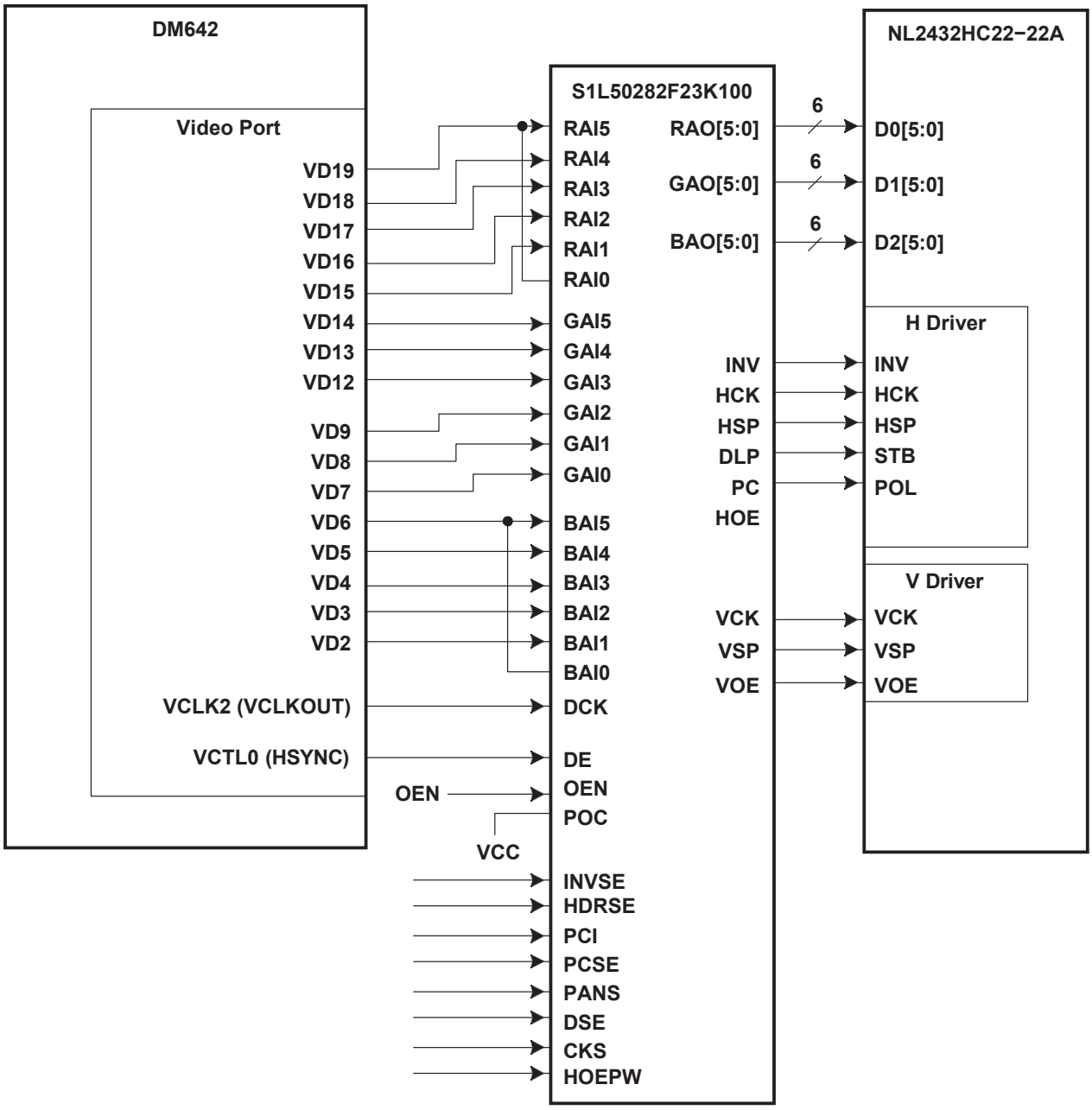



**Figure 1. General System Architecture**

## 2.1 DM642 Video Port

The video port peripheral is an 8/10/16/20-bit parallel video capture or video display interface. Each video port has a channel A and channel B. Either both channels must be inputs or both must be outputs. When configured for 8/10-bit BT.656 mode, the capture can input two separate channels on A and B. The channels can be used together to create a single 16/20-bit input/output. For example, the A display port can be used to output 16/20-bit raw RGB data. It is this raw data output capability which we are going to take advantage of in this application report.

In addition to being able to receive and transmit a variety of data formats, the video port peripheral has a separate clock for each channel and can supply a range of control signals like active video, horizontal and vertical sync, and composite sync, to name a few.

For more information on control signals, supported standards, and general video port operation, please see the *TMS320C64x DSP Video Port/VCXO Interpolated Control (VIC) Port Reference Guide* (SPRU629).

**Table 1. Video Port Signals**

| Signal Name | Description |
|---|---|
| VD[19:12] | Upper bits of Video Data Out |
| VD[9:2] | Lower bits of Video Data Out |
| VCLK2 (VCLKOUT) | Video Port output clock |
| VCTL0 (AVID) | Active Video |

NOTE: This is only a list of video port pins used in this design. For a complete listing, please see SPRU629. Also, VD[11:10, 1:0] are only used in 10/20-bit mode. They allow for fractional values used in BT.656 operation. When in 8/16-bit mode, they are ignored.

## 2.2 NEC S1L50282F23K100

The NEC S1L50282F23K100 is an LCD controller used to interface to QVGA/HVGA LCD modules. This controller, like other LCD controllers, is used to drive the horizontal and vertical gates on an LCD module, adjusting the row/column formatting as is necessary. While doing this, it is also used to control the distinct timing required between data and control signals. The input and output data format is 6-bit x 3 (RGB) parallel.

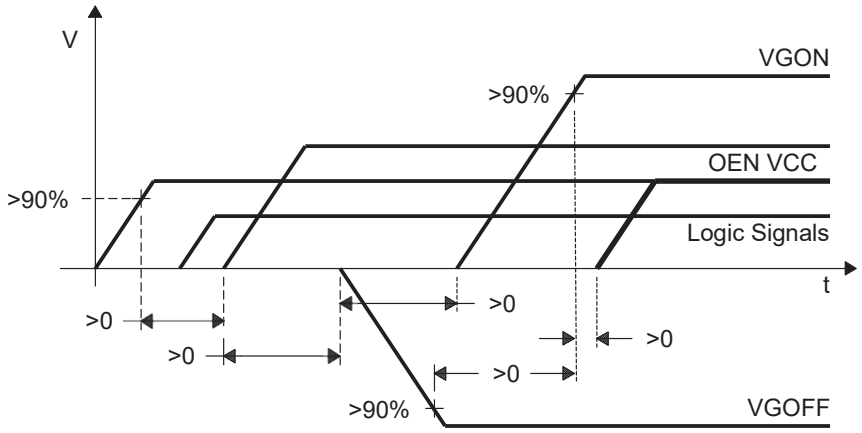
This particular controller was used because of the low number of input signals required for operation. The input and output signals are described in Table 2.

**Table 2. NEC S1L50282F23K100 Input and Output Signal Descriptions**

| Signal Name | I/O | Description |
|---|---|---|
| RAI[5:0] | I | 6-bit red value, 2.5MHz |
| GAI[5:0] | I | 6-bit green value, 2.5MHz |
| BAI[5:0] | I | 6-bit blue value, 2.5MHz |
| DCK | I | Clock, 5MHz |
| DE | I | Data Enable, 18.75kHz − Used to signify when data is enabled for every horizontal line |
| OEN | I | Output Enable, DC – Enable the horizontal and vertical gate driver output |
| POC | I | Power on Clear – Enables or disables device reset (0: reset; 1: reset off) |
| RAO[5:0] | O | 6-bit red value |
| GAO[5:0] | O | 6-bit green value |
| BAO[5:0] | O | 6-bit blue value |
| INV | O | Output data inversion signal, 2.5MHz – Allows you to invert the data going to the LCD module |
| HCK | O | Clock for horizontal gate driver |
| HSP | O | Horizontal driver start pulse |
| DLP | O | Horizontal driver latch pulse |
| PC | O | Polarity Change |
| HOE | O | Source-driver output enable |
| VCK | O | Vertical driver clock |
| VSP | O | Vertical driver start pulse |
| VOE | O | Vertical driver output enable |
| INVSE | I | Not used here, please see the product data sheet. |
| HDRES | I | Not used here, please see the product data sheet. |
| PCI | I | Not used here, please see the product data sheet. |
| PCSE | I | Not used here, please see the product data sheet. |
| PANS | I | Not used here, please see the product data sheet. |
| DSE | I | Not used here, please see the product data sheet. |
| CKS | I | Not used here, please see the product data sheet. |
| HOEPW | I | Not used here, please see the product data sheet. |

### 2.2.1 Power-ON Sequencing

The following supply voltage timings should be met for the LCD controller and module. Their voltages are interdependent; therefore, the signals below are specific to either the controller or the module. See Figure 2 to find out which signal applies to which part.




| Signal | Value | Description− Module |
|---|---|---|
| VGON | +15 V | V driver (+) supply voltage − Module |
| VGOFF | −15 V | V driver (−) supply voltage − Module |
| VDD | +4.5 V | H driver supply voltage − Module |
| VCC | +3.0 V | Logic supply voltage − Controller and Module |
| OEN | +3.0 V | Output enable signal − Controller |

**Figure 2. LCD Controller and Module Power-ON Sequencing Requirement**

## 2.3 Video Port to S1L50282F23K100 Interface Details

We will now address some of the details involving the output signals from the DM642 video port to the input of the S1L50282F23K100.

### 2.3.1 Data Interface

The S1L50282F23K100 requires a 18-bit input (R:G:B → 6:6:6). TI has developed Y:Cr:Cb to RGB conversion algorithms; however, these algorithms convert to a 16-bit, 5:6:5 RGB format. To lessen the amount of software development for algorithm modification, appropriate bit-packing, etc., we decided to use the existing RGB conversion algorithm. To accommodate the difference in data widths, we tie together the most and least significant bits on the R and B data lines, as is shown in Figure 1. This is a commonly used scheme in systems where you need to convert a 16-bit output to 18-bits.

### 2.3.2 Control Interface

**DCK:**

The *DCK* input is used to specify the clock for the controller.

## DCK Implementation

The video port can generate a clock signal on its VCLK2 pin. We use this signal to provide the controller a 5MHz clock.

**DE:**

The *DE* signal is used to generate an internal horizontal and vertical sync. This sort of scheme is referred to as virtual timing. It does not require the CPU to provide timing information to the LCD Controller; but only to provide an active data signal with a few timing constraints. These constraints are defined in Figure 3.

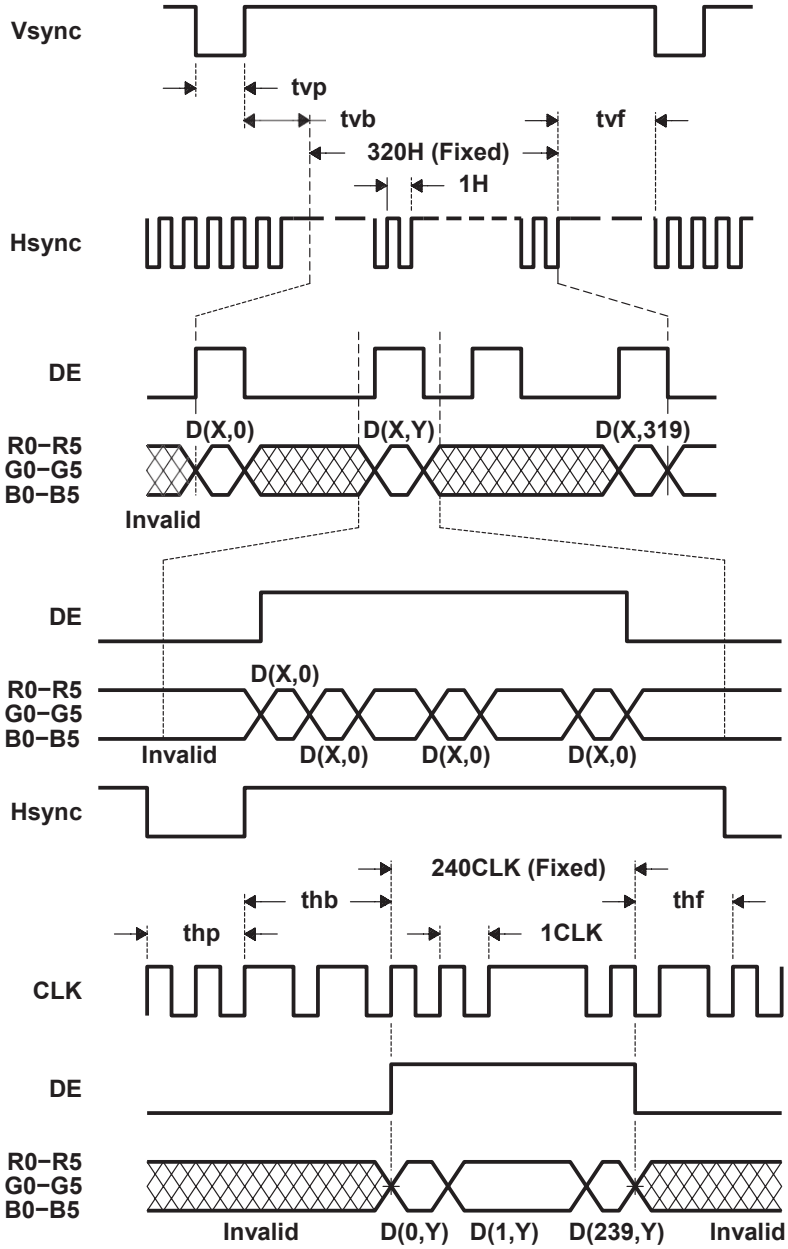



**Figure 3. Data Enable Signal Timing Requirements**

The above series of timing diagrams can be summarized using the following picture:

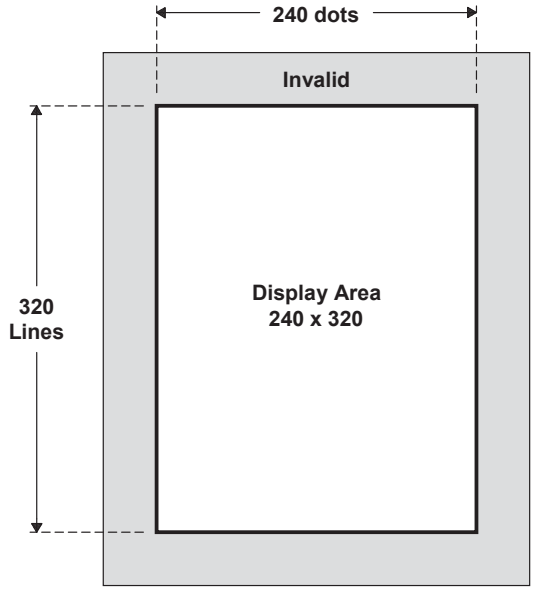



**Figure 4. Display Area with DE Signal**

While the data for the display area is being outputted, the data enable (DE) signal should be high.

**DE Implementation**

The DM642 video ports can output an active video control signal on pin VCTL0. This signal is high while the video port is outputting data for the current frame. This corresponds exactly to the definition of what the DE signal should be as described above.

**OEN:**

The OEN input is used to enable the output of the horizontal and veritcal gate drivers to the LCD module. In our design, we want the output to be enabled at all times, so we simply tie this signal high.

**OEN Implementation**

There is one consideration with this signal and that is its timing requirement with the rest of the power supply voltages. The *OEN* signal nees to be the last driven voltage in a sequence. The idea behind this is that you want the LCD module to be up and running before the controller starts sending it data. To achieve this, you use the *TPS3801−01*. The design can be seen in Appendix A.

**POC:**

The *POC* input specifies device reset.

**POC Implementation:**

For our purposes, the device will come out of reset on power up, but it will always be ready subsequently; therefore, we also tie this signal high.

## 2.4 Achieving Higher Resolutions

The DM642 video ports have the ability to interface to much higher resolution LCDs like SVGA (800 x 600) and XVGA (1024 x 768). This is done simply by changing the values in the video port display registers to reflect a larger viewing area and appropriately modified SYNC and blanking intervals. It should be noted however, that with this particular NEC LCD controller, the highest achievable resolution is HVGA (640 x 240). To achieve the higher resolutions on larger LCD modules, you would need a different LCD timing controller. In fact for the larger LCD modules, the timing controller is usually built into the device; therefore, the DM642 video port would interface directly to the LCD module.

# 3 Video System Hardware Design Guidelines

To achieve good performance within the video system, some general guidelines have been listed below. These guidelines are given in a checklist format for ease of implementation. These techniques provide a starting point for creating a low-noise video system. Signal integrity analysis should be done using IBIS modeling in order to help obtain optimum signal integrity and performance.

**Table 3. DM642 Video Port to THS8200 Hardware Design Checklist**

| Completed | Description |
|---|---|
| | **Power Supplies** |
| ☐ | Analog and digital power supplies should be separated. |
| ☐ | The power supplies should have a high power supply rejection ratio (PSRR). |
| ☐ | Multiple connections between the separate ground planes generate current loops, which must be avoided. |
| | **Decoupling/Bypass Capacitance** |
| ☐ | Multiple decoupling capacitors should be located as close as possible to all digital ICs, especially the video DAC and DSP. |
| ☐ | As many 0.1-μF capacitors with low ESL/ESR should be placed near the ICs as feasible. |
| ☐ | Bulk capacitors, on the order of 10-μF, should also be used to help filter power supply fluctuations. |
| | **Signal Integrity** |
| ☐ | Serial termination may be necessary on all data busses, address busses, and/or control/clock signals. Longer traces (>1.5 in.) generally require serial termination. Shorter traces may not require termination, but |
| ☐ | IBIS analysis can provide insight as to proper sizing and placement of termination resistors. |
| ☐ | High speed interfaces should be kept within a reasonable length. Buses and control signals should not vary greatly in length. |
| ☐ | Clock lines have proper termination and do not branch off several times on a given net. |

# 4 Conclusion

This application report demonstrates a glueless interface between a DM642 video port and an LCD controller. The proper selection of LCD module will allow a glueless interface from the controller to the module, as well. This design and the schematics in Appendix A have been tested with hardware and attached software. It should be noted that this design is very specific to the chosen NEC LCD controller and module. While the control signals reuired for most modules will allow for DM642 video ports to be a glueless interface, so modules might require a particular combination of control signals that could make the connection more difficult. A future application report will contain a working example application with software.

# 5 References


1. *TMS320DM642 Data Manual* (SPRS200)
2. *TMS320C64x DSP Video Port/VCXO Interpolated Control (VIC) Port Reference Guide* (SPRU629)
3. *LCD Controller Type: S1L50282F23K100* (DOD-N-0195)
4. *TFT Color LCD Module Type: NL2432HC22-22A* (DOD-PD-0073)
5. *TPS2034 Power-Distribution Switch* (SLVS190)
6. *Low Power DC/DC Boost Converter* (SLVS413)
7. *Constant Current LED Driver* (SLVS441)
8. *TPS77601, Fast-Transient-Response 500-mA LDO Voltage Regulator* (SLVS232)

# Appendix A S1L50282F23K100 Daughtercard Schematics for DM642 EVM

Appendix A contains preliminary schematics for the S1L50282F23K100 LCD Controller daughtercard for the DM642EVM. These schematics have yet to be tested, and they should only be used as an example of how to interface a DM642 video port to an LCD controller. While we have chosen the S1L50282F23K100 in our design, the general scheme is applicable to a variety of devices.

The schematics are also inclued in PDF format within the attached .zip file.

# S1L50282F23K100 LCD Controller Daughter Card for the DM642 Evaluation Module

Table of Contents



Revision History

| Rev.# | Description | Date | Approved |
|---|---|---|---|
| 0.1 | Preliminary Schematics Completed | 10/20/2003 | AAS |
| 0.2 | Changed R57 Value, Added R61 and R62, Deleted L1 | 11/25/2003 | AAS |
| 0.3 | Assigned part numbers to diodes in power supply design. | 12/01/2003 | AAS |
| 0.4 | Switched labeling of pins 4 and 5 on TPS76301, connected pin 2 on TPS61040 to ground, changed C15 to be a polar Cap. | 02/27/2004 | AAS |

Notes:

1) RESISTANCE VALUES ARE IN OHMS
2) CAPACITANCE VALUES ARE IN MICROFARADS
3) BOARD PROPERTIES
   A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE PARTS SHALL NOT USE THERMAL RELIEFS
   B. 50 OHM MATCHED IMPEDANCE FOR DIGITAL LINES. 75 OHM MATCHED IMPEDANCE FOR ANALOG LINES
   C. OUTER LAYERS 0.5 OZ CU & 0.5 OZ AU PLATING
   D. INNER LAYERS 1.0 OZ CU
   E. FR4 BOARD MATERIAL
   F. MINIMUM TRACE WIDTH/SPACING 4 MILS
   G. MINIMUM VIA SIZE 10/19 MILS
   H. APPROXIMATE BOARD SIZE 5.125 x 3.125 INCHES
   I. U13 HAS A PowerPAD THAT IS CONNECTED THROUGH PIN 21
   J. THERMAL RELIEFS SHOULD NOT BE USED

| TI | |
|---|---|
| Title: | **LCD Daughtercard for DM642 EVM** |
| Description: | Title |
| Doc. #: | SPRA975 |
| Rev.: | 0.4 Page: 1 of 7 |
| Date: | Tuesday, April 20, 2004 |

**Figure A−1. Schematic Title Page**

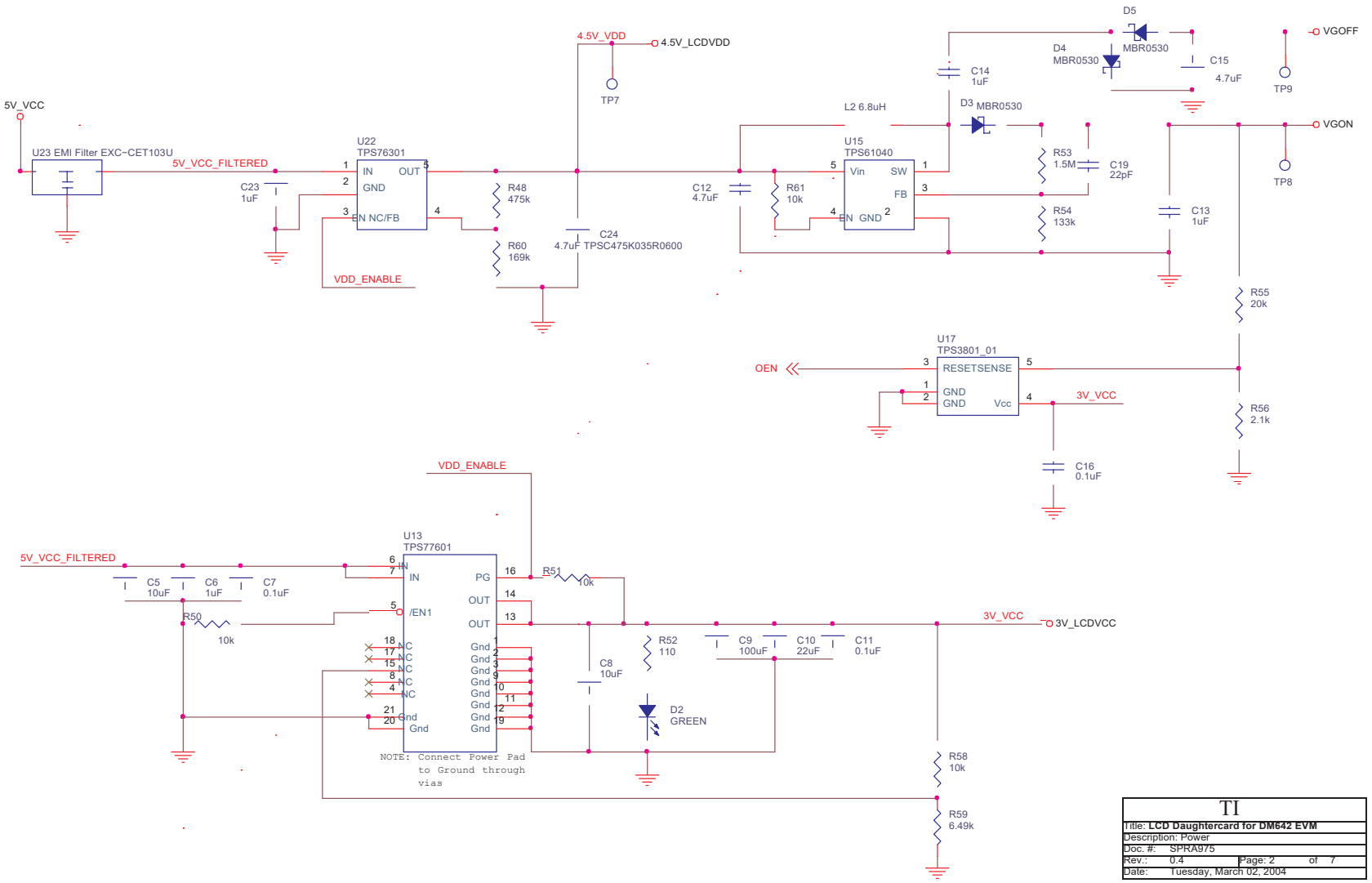



**Figure A−2. Power Supply Design**

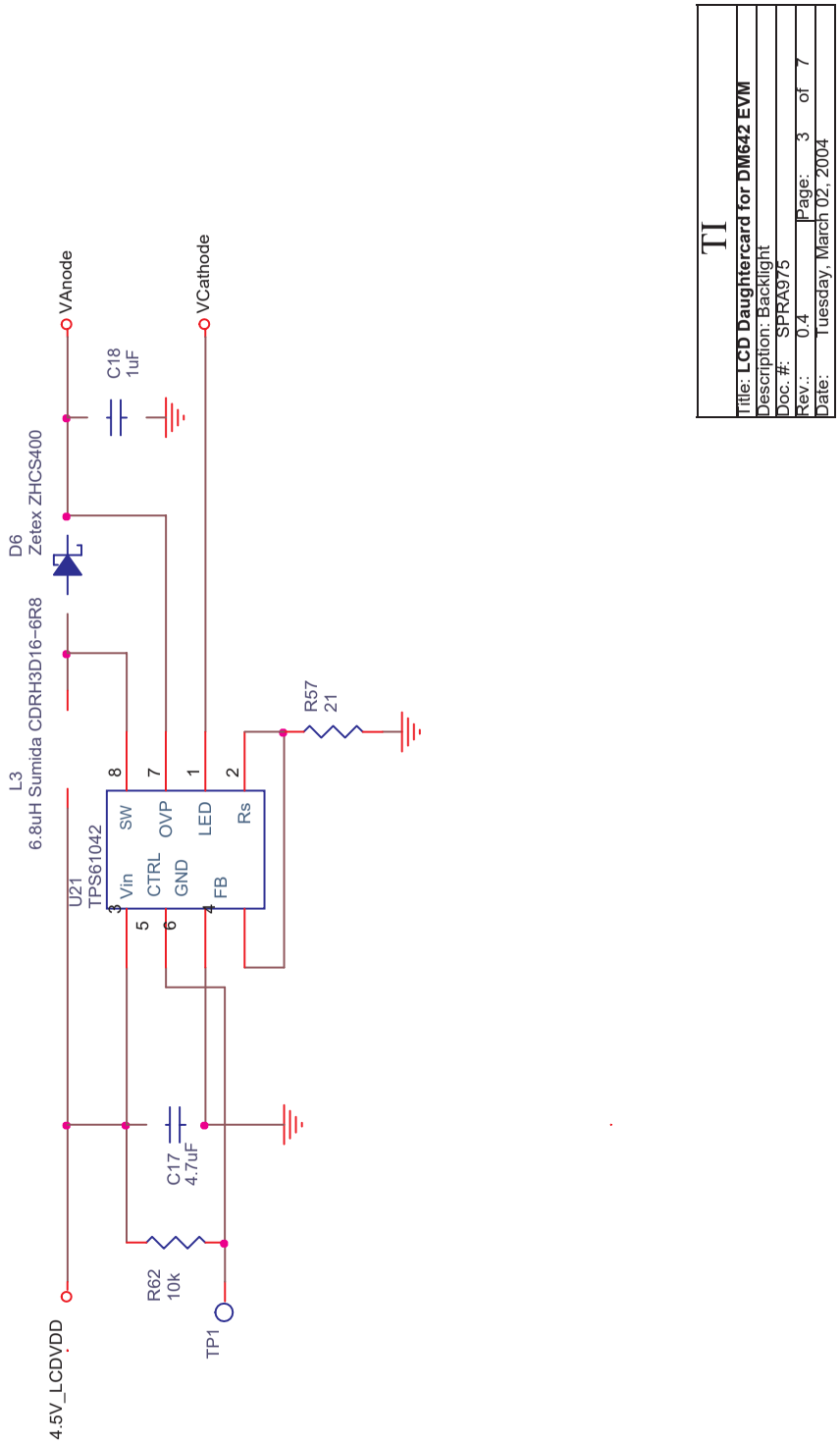



**Figure A–3. LCD Backlight Circuit**

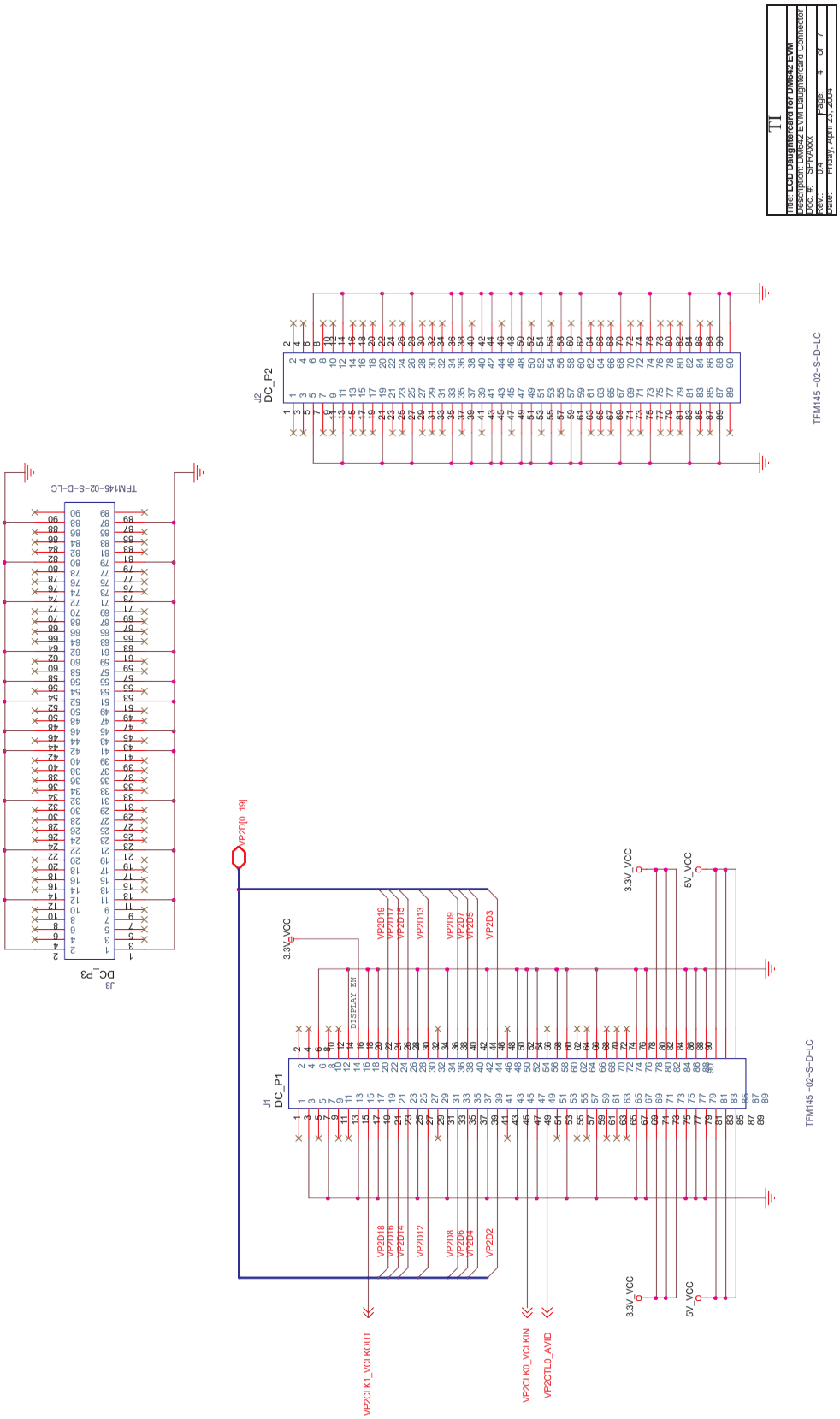



**Figure A–4. DM642 EVM Daughter Card Connectors**

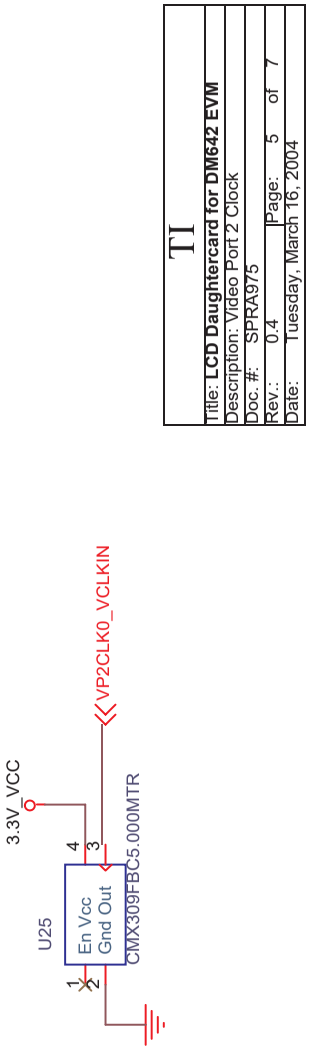



**Figure A–5. Video Port Clock**

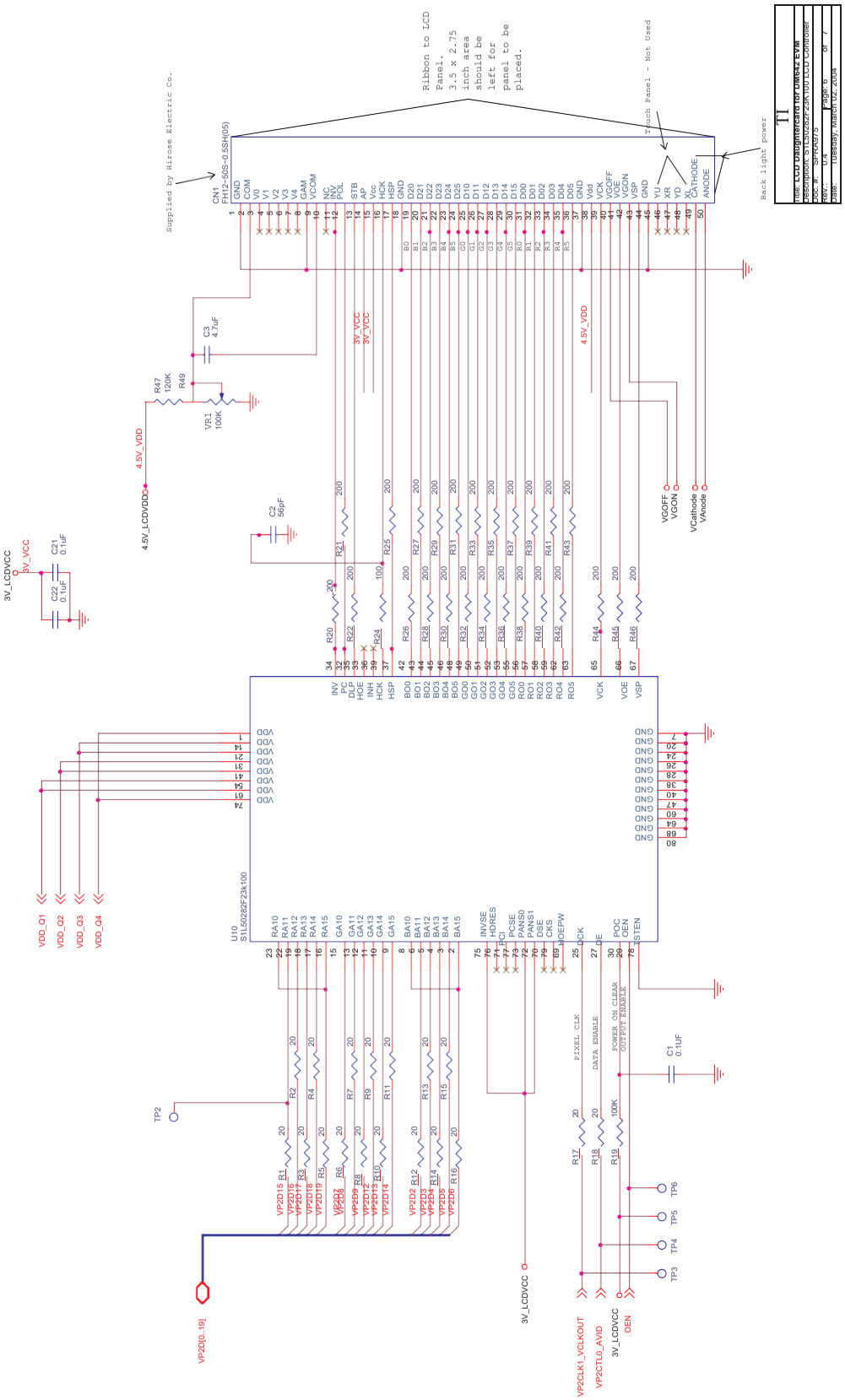



**Figure A–6. S1L50282F23K100**

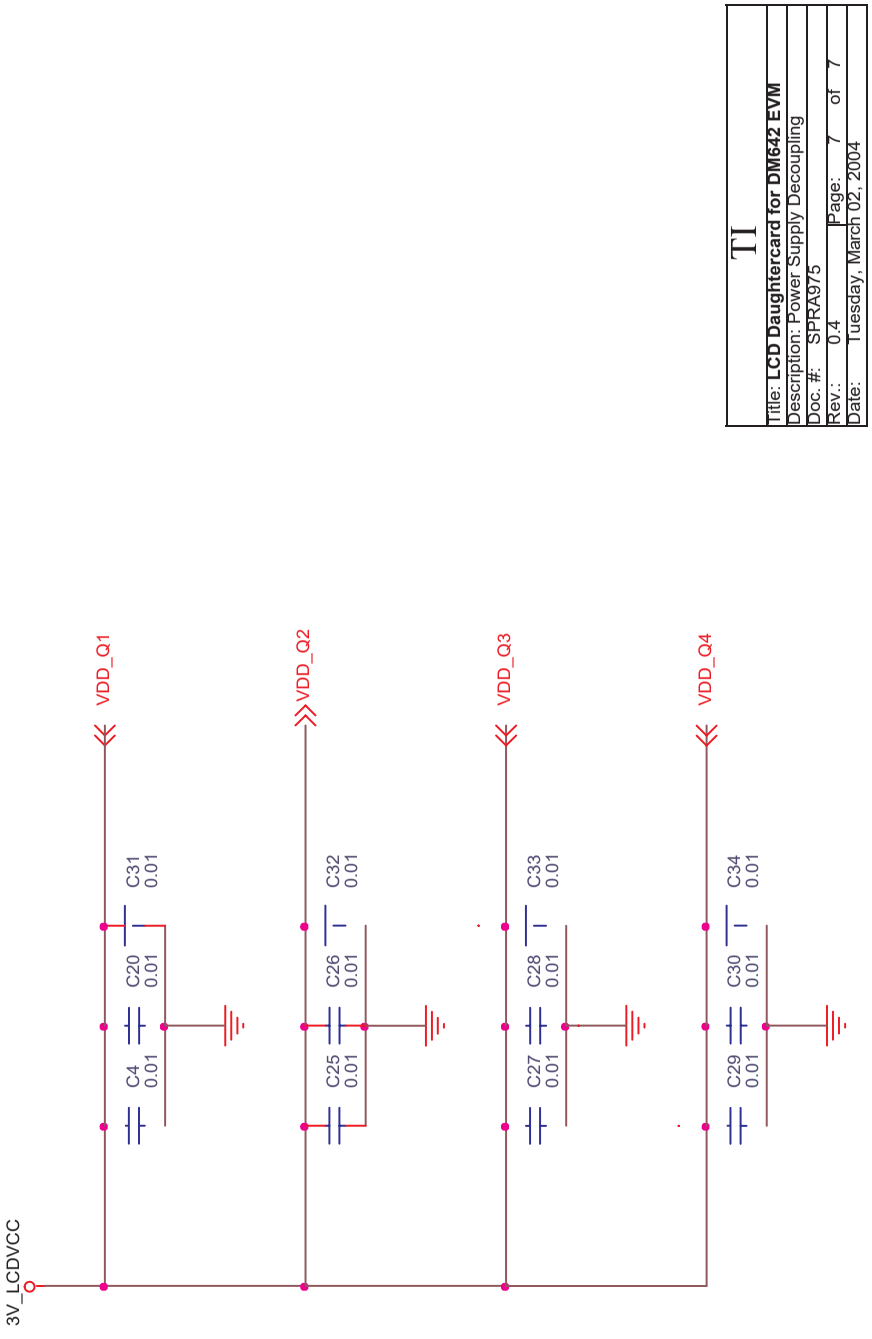



**Figure A–7. Power Supply Decoupling**

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