Application Report
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Crosspoint Switch with TS3USB30 Device

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ABSTRACT

Cross-point switches are particularly helpful in simplifying layouts when traces have to cross and also are helpful in USB Type-C applications switching the top and bottom signals of the reversible connector. This document introduces how to use two TS3USB30 devices to provide 2 : 2 Cross-point switch with only one GPIO to control the Mux.

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Trademarks

1 Introduction

The TS3USB30 is a high-bandwidth 1:2 switch specially designed for the switching and isolating of high-speed USB 2.0 signals in systems with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs or from two different hosts to one corresponding output. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The TS3USB30 integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.8 mm x 1.4 mm) .

Cross-point switches are particularly helpful in simplifying layouts when traces have to cross and also are helpful in USB Type-C applications switching the top and bottom signals of the reversible connector.

There are some switch devices on the market for cross-point switches, but either they need more GPIOs to control the Mux or with large package size.

Here we are going to introduce a 2:2 Mux using two TS3USB30 devices. With only one GPIO, it can be either 2:2 cross-point switch or just 2:2 fan out.

(1)

2 Functional Block Diagram

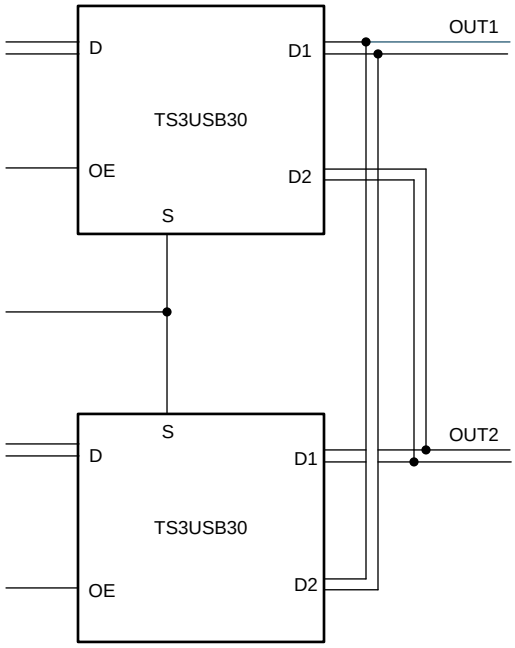

Figure 1. Function Block Diagram

3 Device Functional Mode

It can be configured to be either cross-point switch or just fan out based on the layout requirement controlled by GPIO pin FLIP. It should be available from any PD controller.

The device functional modes are shown in Table 1. Inputs signal USB2 or I2C can be routed to OUT1 or OUT2.

Table 1. Differential MUX Function Table

CONTROL SETTING		SIGNAL ROUTING	
FLIP	OE	OUT1	OUT2
L	L	USB2	I2C
H	L	I2C	USB2

4 Application Information

4.1 2:2 Differential Cross-point Switch

It can be configured to be cross-point switch if FLIP control pin is high and OE pin is low. USB2 signal will be routed to OUT2 and I2C signal to OUT1.

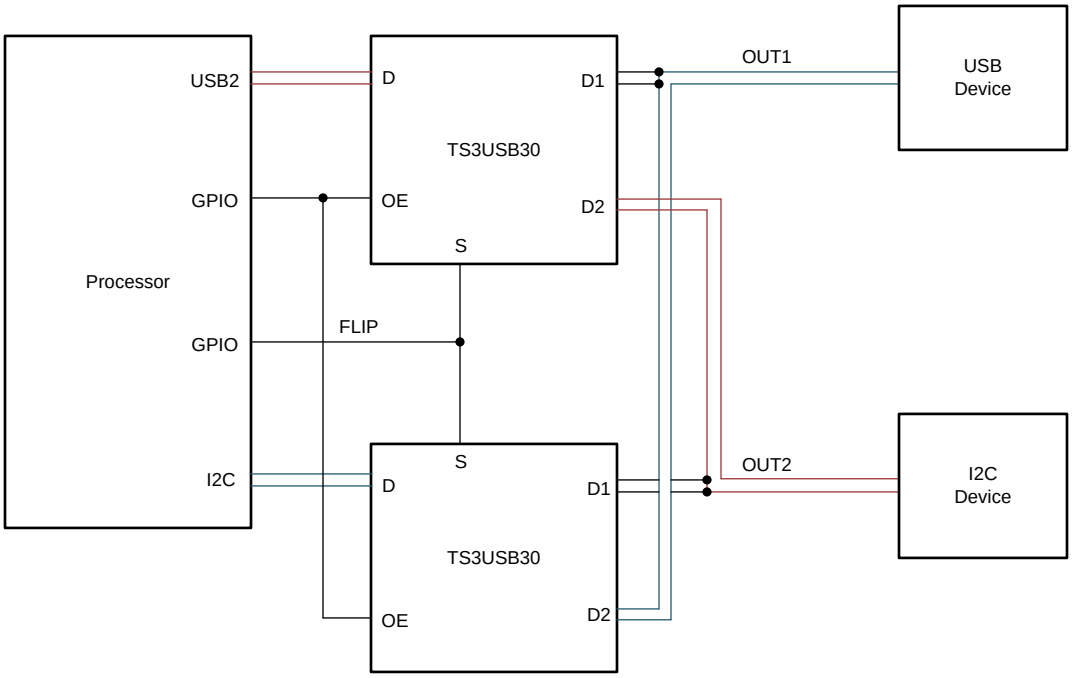

Figure 2. 2:2 Differential Cross-point Switch Schematic

4.2 2:2 Differential Fan out

It also can be configured to be 2:2 fan out if FLIP control pin is low and OE pin is low. USB2 signal will be routed to OUT1 and I2C signal to OUT2.

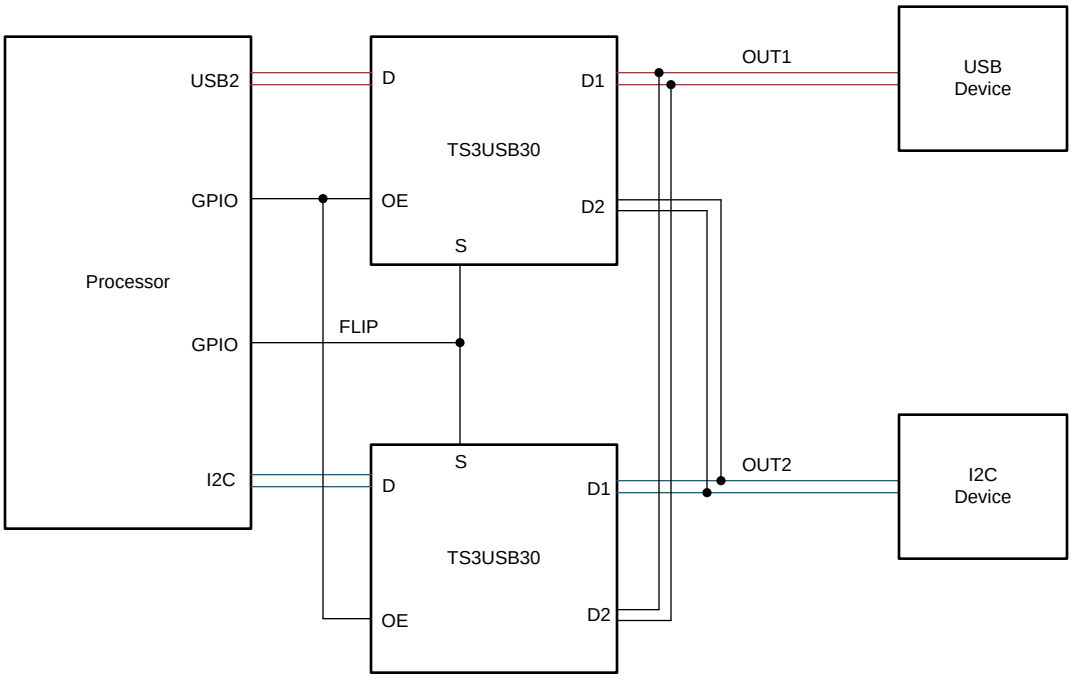

Figure 3. 2:2 Differential Fan Out Switch Schematic

5 Power Supply Recommendations

Power to the device is supplied through the VCC pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

6 Layout

6.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see High Speed Layout Guidelines (SCAA082) and USB 2.0 Board Design and Layout Guidelines (SPRAAR7).

6.2 Layout Example

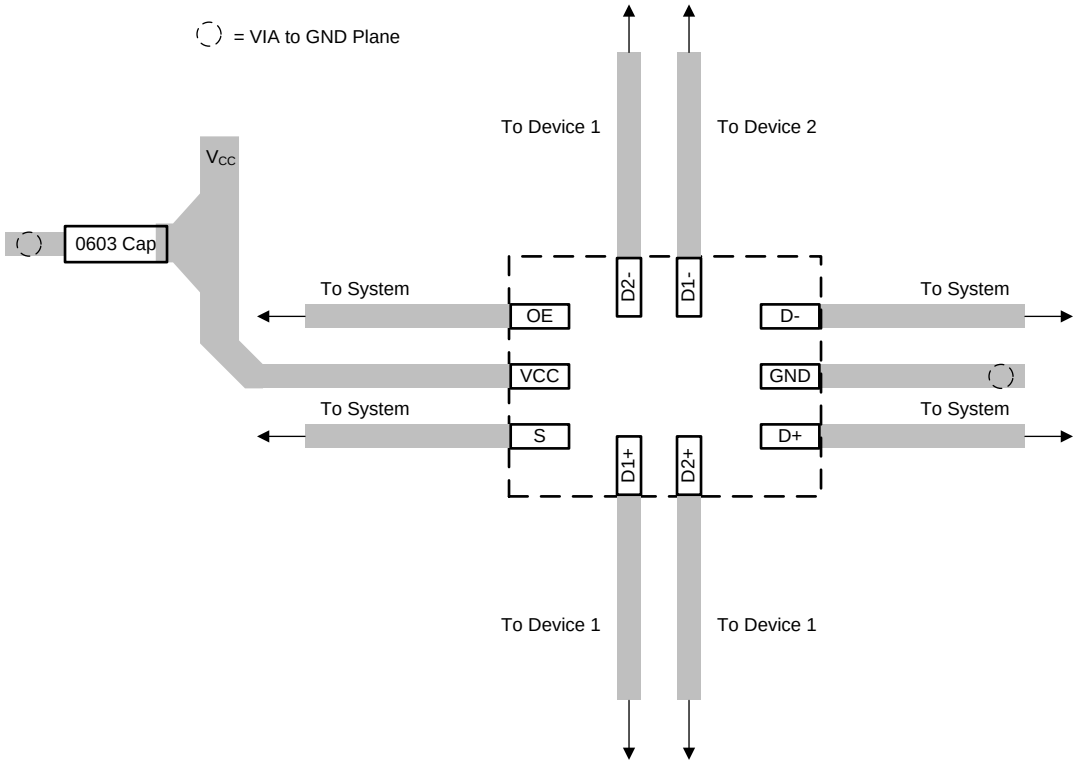

Figure 4. Layout Recommendation

7 References

• Datasheet: TS3USB30 High-Speed USB 2.0 (480-MBPS) 1:2 Multiplexer/Demultiplexer Switch With Single Enable SCDS237F

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