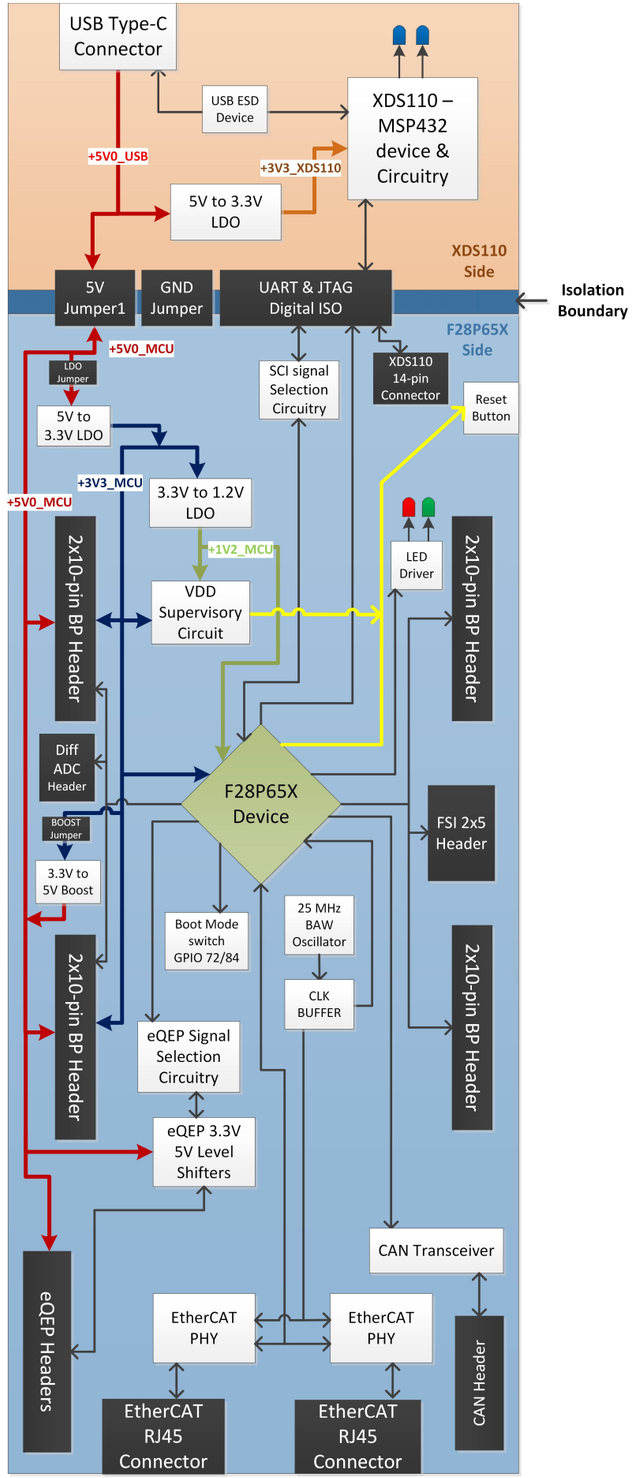
1) ETHERCAT Differential pairs - 100 Ohm
(A) TD_P and TD_N
(B) RD_P and RD_N

2) USB Differential Pairs - 90 Ohm
(A) USB_D_P and USB_D_N

3) ADC Differential pair Impedance Matching - 50 Ohm
(A) ADCINB8B9_P and ADCINB8B9_N
(B) ADCINC8C9_P and ADCINC8C9_N
(C) MCU_B8B9_P and MCU_B8B9_N
(D) MCU_C8C9_P and MCU_C8C9_N

4) CLK Paths - 50 Ohm
(A) X1
(B) PHY0_25MHZ_CLK and PHY1_25MHZ_CLK



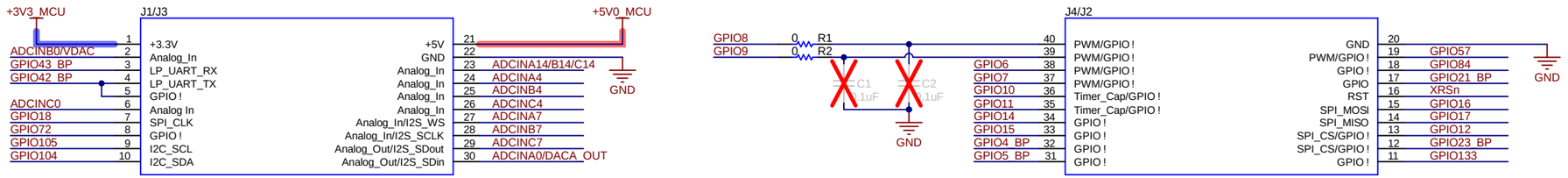
Revision History

Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	April 12, 2023	PL	Original engineering release.
A	N/A	June 7, 2023	PL	Cosmetic changes to PCB silkscreen.

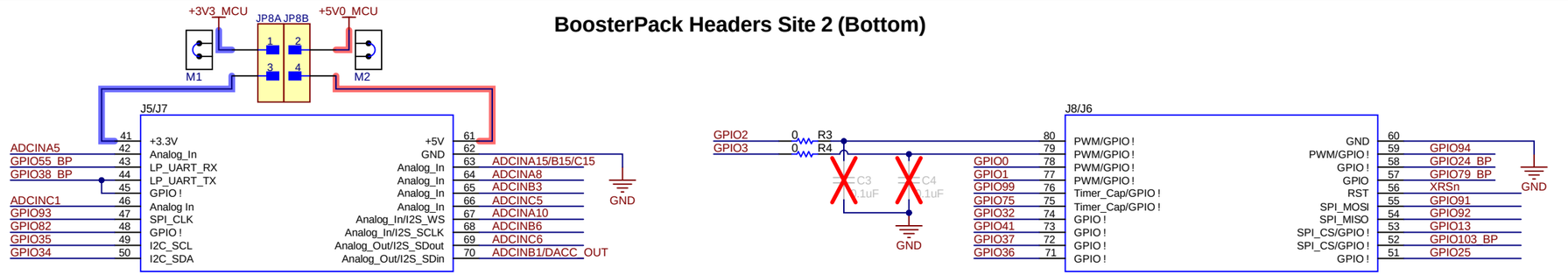
Orderable: LAUNCHXL-F28P65X	Designed for: Public Release	Mod. Date: 8/8/2023	
TID #: N/A	Project Title: LAUNCHXL-F28P65X		
Number: MCU117 Rev: A	Sheet Title:		
SVN Rev: f32bee2f24060b802f8157a[redacted]001		Sheet: 1 of 9	
Drawn By: Peter Luong	File: MCU117A_Block_Diagram.SchDoc	Size: B	
Engineer: Peter Luong	Contact: http://www.ti.com/support		

TEXAS INSTRUMENTS
http://www.ti.com

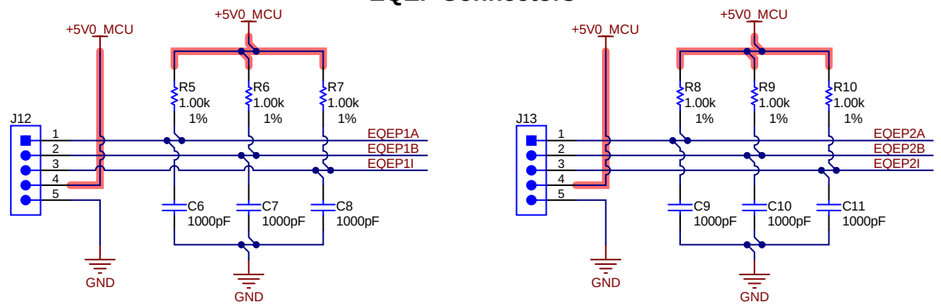
BoosterPack Headers Site 1 (Top)



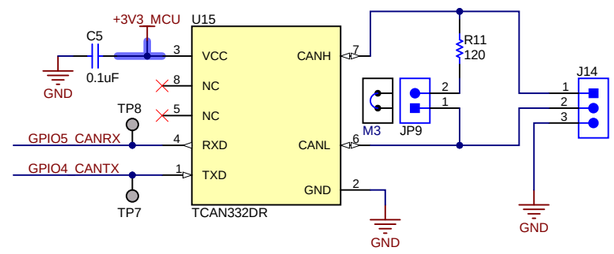
BoosterPack Headers Site 2 (Bottom)



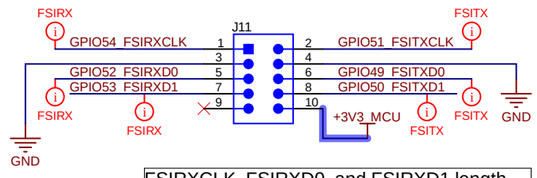
EQEP Connectors



CAN Transceiver & Connector

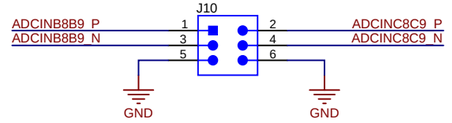


FSI Connector



FSIRXCLK, FSIRXD0, and FSIRXD1 length matched to each other with 25mil tolerance.
FSITXCLK, FSITXD0, and FSITXD1 length matched to each other with 25mil tolerance.

Differential ADC Connector



Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A		Project Title: LAUNCHXL-F28P65X	
Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf090[illegible]: 001			Sheet: 2 of 9
Drawn By: Peter Luong		File: MCU117A_Connectors.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

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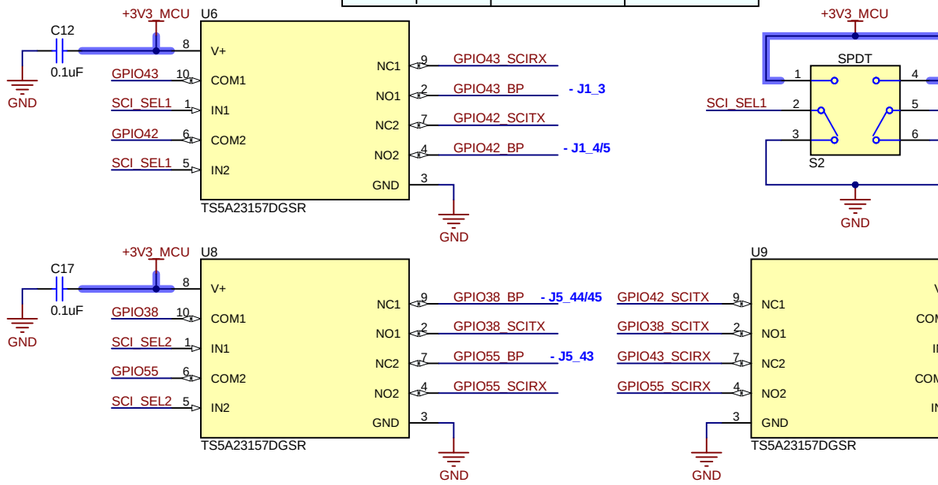
http://www.ti.com

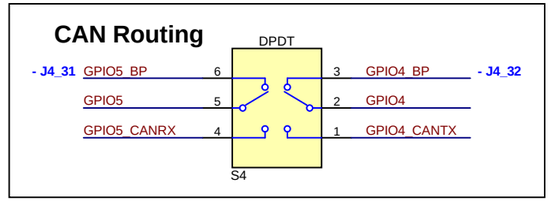
UART Routing

SCI_SEL1	SCI_SEL2	GPIO42/43 Route	GPIO38/55 Route
0	0	XDS110 COM Port	BP
0	1	XDS110 COM Port	NC
1	0	BP	BP
1	1	BP	XDS110 COM Port

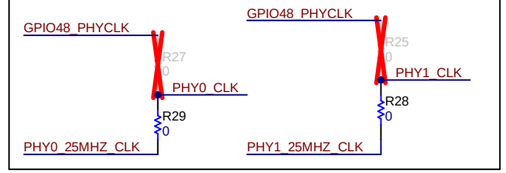
- DEFAULT



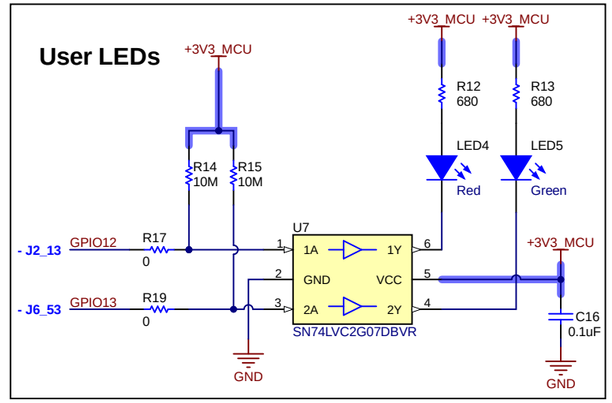
CAN Routing



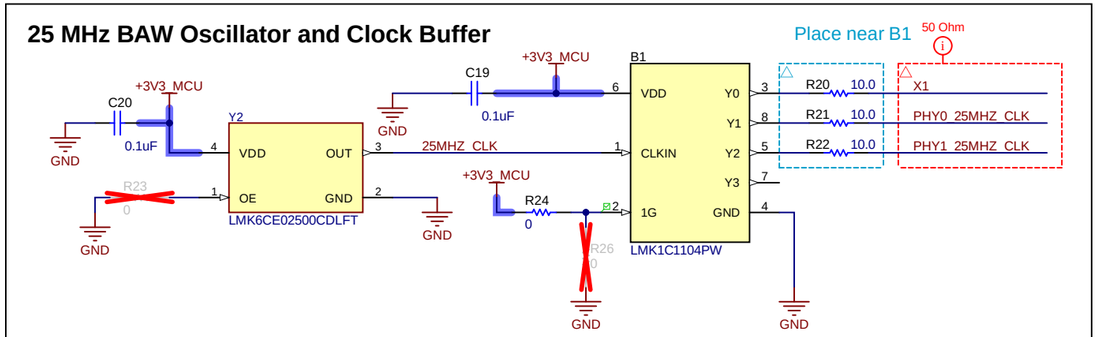
Clock Source Selection



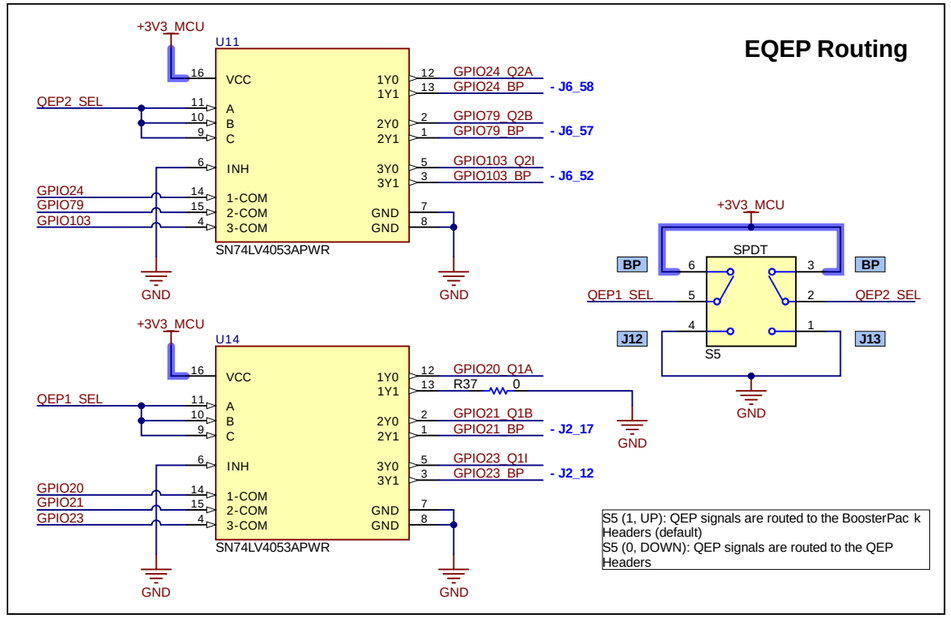
User LEDs



25 MHz BAW Oscillator and Clock Buffer

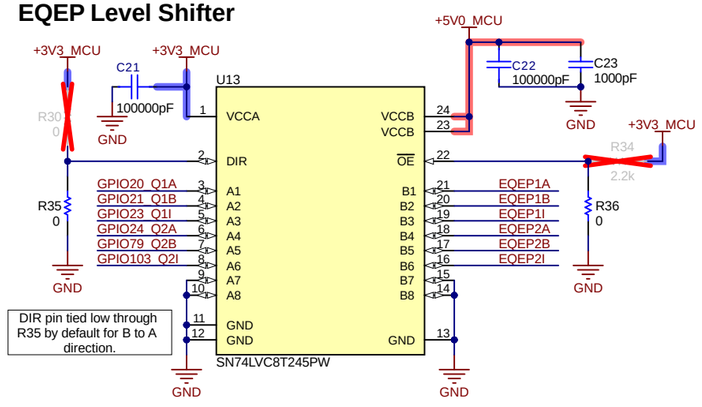


EQEP Routing



S5 (1, UP): QEP signals are routed to the BoosterPac k Headers (default)
S5 (0, DOWN): QEP signals are routed to the QEP Headers

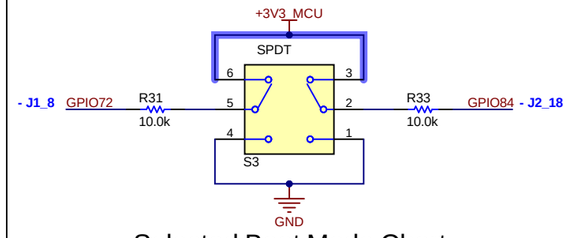
EQEP Level Shifter



DIR pin tied low through R35 by default for B to A direction.

To disable the Level Shifter:
1. De-populate R36
2. Place a 2.2k ohm resistor on R34 to pull-up OE

Boot Mode Select

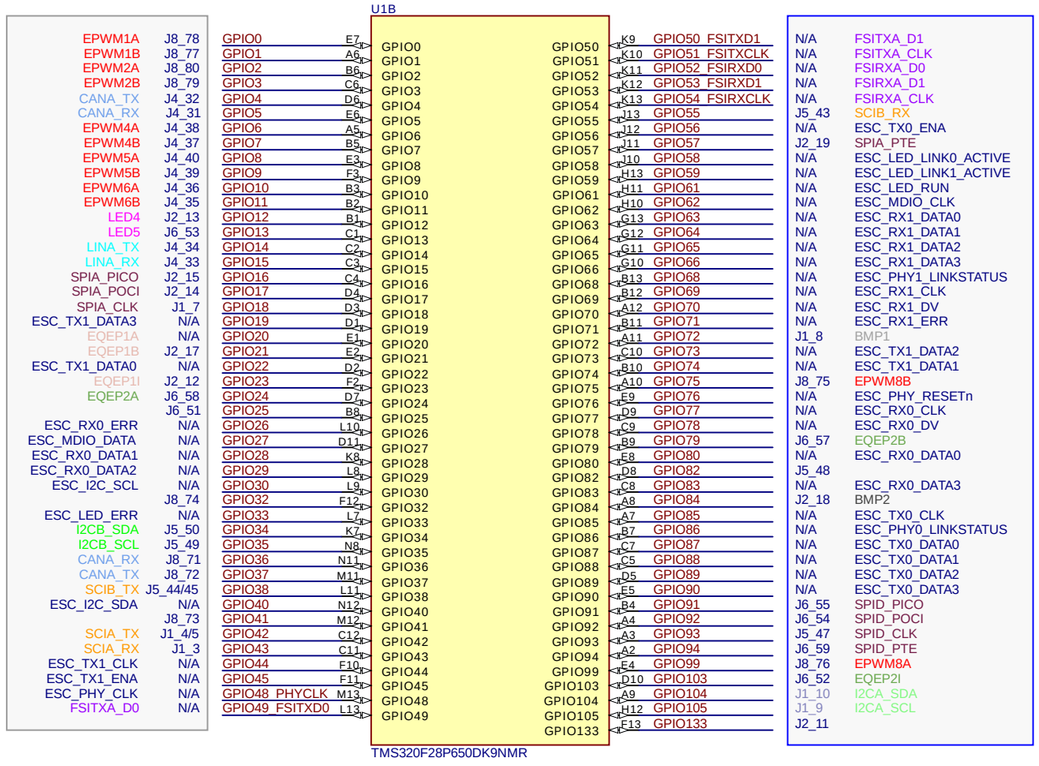


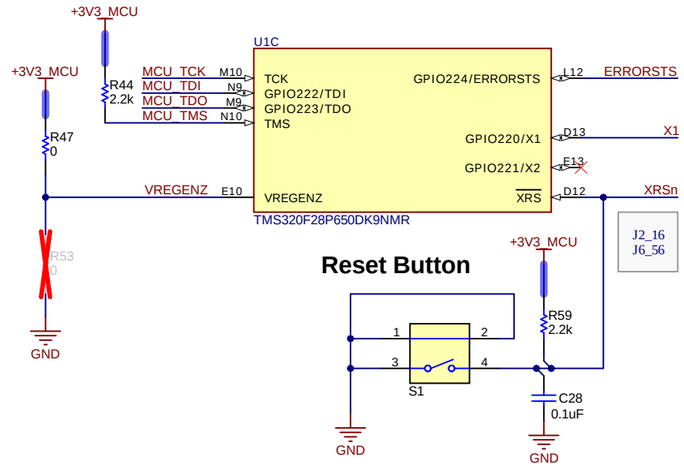
Selected Boot Mode Chart

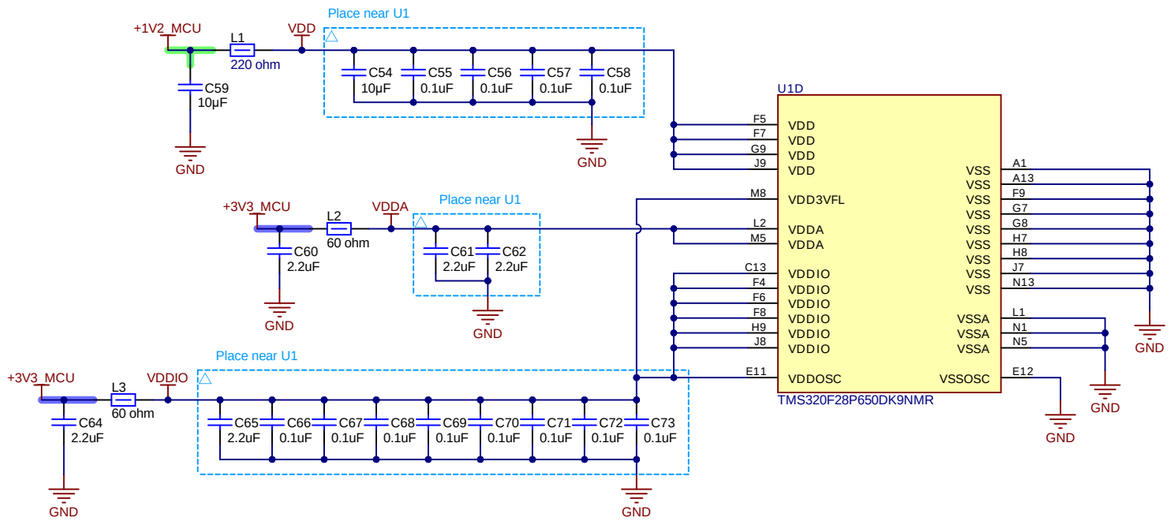
Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A		Project Title: LAUNCHXL-F28P65X	
Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf09043ed42c3497f2ff		File: 001	Sheet: 3 of 9
Drawn By: Peter Luong		File: MCU117A_AltRouting_Misc.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	http://www.ti.com

F28P65x Device



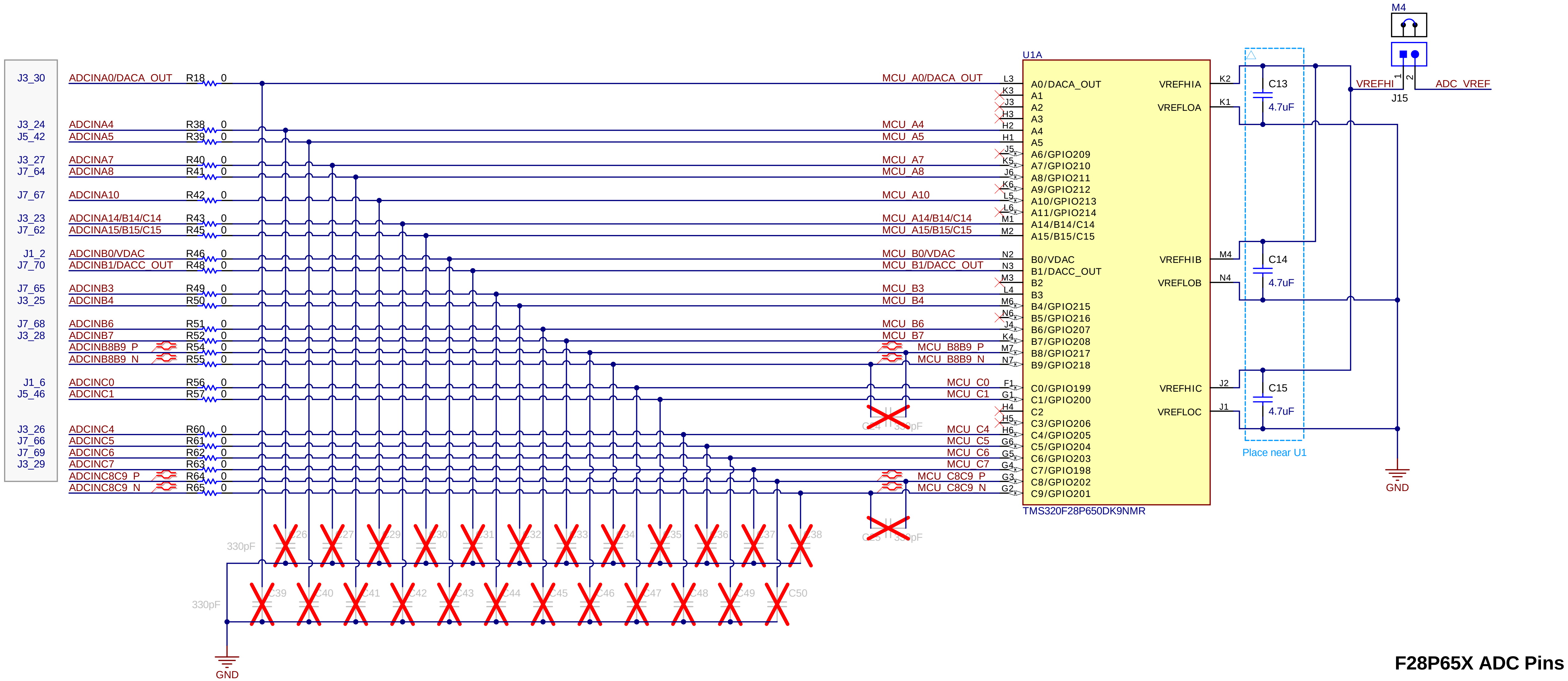




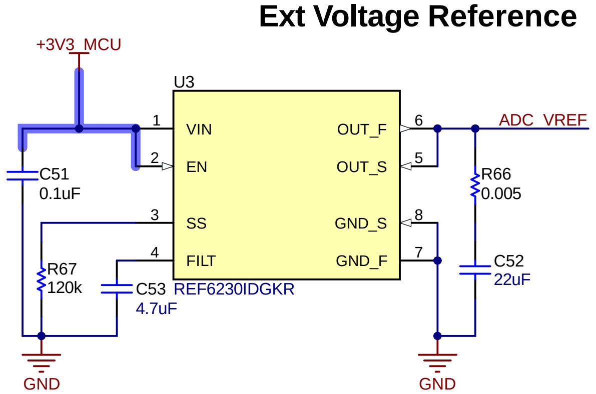
Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A		Project Title: LAUNCHXL-F28P65X	
Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf090[illegible]		Sheet: 4 of 9	
Drawn By: Peter Luong		File: MCU117A_F28P65X_Device.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

http://www.ti.com

F28P65X ADC Pins



Ext Voltage Reference



The on-board REF6230 supports all 12-bit ADC modes and does not guarantee datasheet-specified performance in 16-bit mode. This REF6230 is not a recommended reference for designs requiring 16-bit ADC operation. Instead, please refer to TMDSCNCD28P65X for recommended ADC reference circuit.

Orderable: LAUNCHXL-F28P65X | Designed for: Public Release | Mod. Date: 8/8/2023
TID #: N/A | Project Title: LAUNCHXL-F28P65X
Number: MCU117 | Rev: A | Sheet Title:
SVN Rev: f3f0c28fbfb7c50f7254bf09047ae4d42c349208 | Assembly Variant: 001 | Sheet: 5 of 9
Drawn By: Peter Luong | File: MCU117A_ADC.SchDoc | Size: B
Engineer: Peter Luong | Contact: http://www.ti.com/support
Texas Instruments
http://www.ti.com

EtherCAT EEPROM

U12 (NC, NC, NC, VSS, VCC, WP, SCL, SDA) — +3V3_MCU, C86 0.1uF, R105 4.7k, R106 4.7k, GPIO30, GPIO40, GND

EtherCAT PHY0

U17 DP83826ERHB

Pin	Signal
33	PAD
21	PowerDown/Interrupt
10	RBias
9	XI/50Mhz In
8	XO
19	RX_CLK/50MHZ_RMII
18	RX_DV/CRS_DV/Strap10
15	Strap9/RX_D1
14	Strap8/RX_D2
13	Strap7/RX_D3
20	RX_ER/Strap6
22	TX_CLK/Strap5
28	COL/LED_2/GPIOStrap4
29	CRS/Strap3
30	LED0/Strap2
31	CLKOUT/LED_1/Strap1
16	Strap0/RX_D0
1	ModeSelect
32	RST_N
12	MDC
11	MDIO
2	CEXT
23	TX_EN
27	TX_D3
26	TX_D2
25	TX_D1
24	TX_D0
6	TD_M
7	TD_P
4	RD_M
5	RD_P
17	VDDIO
3	VDDA3.3

+3V3_MCU, R108 4.7k, R109 6.49k, PHY0_CLK, GND, Place near P0

PHY0 Address selection: R88 2.49k, R89 2.49k, R111 2.49k, R123 2.20k, R124 2.20k, R125 2.20k, R112 2.49k, R113 2.49k, R127 2.49k, R128 2.49k — PHY0_ADDR=0x0

GPIO77, GPIO78, GPIO28, GPIO29, GPIO83, GPIO26, GPIO85, GPIO80 — R114 33.2, R115 33.2, R116 33.2, R117 33.2, R118 33.2, R119 33.2, R120 33.2, R121 33.2, R122 33.2, R126 33.2

R129 2.49k, GPIO86

R58 0 GPIO56, R83 0 GPIO90, R84 0 GPIO89, R86 0 GPIO88, R87 0 GPIO87

R32 4.7k, GPIO76, GPIO62, GPIO27, R107 2.20k, +3V3_MCU

C89 2.2uF, C90 0.1uF, C91 4.7pF, C92 4.7pF, C93 4.7pF, C94 4.7pF

PHY0_TD_N, PHY0_TD_P, PHY0_RD_N, PHY0_RD_P

U19 TPD4E05U06DQAR (D1+, D1-, GND, D2+, D2-, NC, NC, NC, NC, GND, GND, NC, NC)

R131, R134, C97 22uF, C98 0.1uF, C99 47uF, C100 0.1uF

RJ1 7498010210A (TD+, TCT, TD-, RD+, RCT, RD-, NC, CHS GND, Shield, Shield)

Place near RJ1: C87 0.1uF, C88 1uF; C95 0.1uF, C96 1uF; C101 0.01uF, R136 1.00M

J1, J2, J3, J6, J4, J5, J7, J8

GPIO58, R132 470, GPIO86, R135 470

ETH1_EARTH

Run and Error LEDs

U18A, U18B, U18C

GPIO33 Error LED — Red D11 — R137 1.27k

GPIO61 Run LED — Bright Green D12 — R138 680

R139 1.5M, R140 1.5M, C103 0.1uF, +3V3_MCU, GND

EtherCAT PHY1

U20 DP83826ERHB

Pin	Signal
33	PAD
21	PowerDown/Interrupt
10	RBias
9	XI/50Mhz In
8	XO
19	RX_CLK/50MHZ_RMII
18	RX_DV/CRS_DV/Strap10
15	Strap9/RX_D1
14	Strap8/RX_D2
13	Strap7/RX_D3
20	RX_ER/Strap6
22	TX_CLK/Strap5
28	COL/LED_2/GPIOStrap4
29	CRS/Strap3
30	LED0/Strap2
31	CLKOUT/LED_1/Strap1
16	Strap0/RX_D0
1	ModeSelect
32	RST_N
12	MDC
11	MDIO
2	CEXT
23	TX_EN
27	TX_D3
26	TX_D2
25	TX_D1
24	TX_D0
6	TD_M
7	TD_P
4	RD_M
5	RD_P
17	VDDIO
3	VDDA3.3

+3V3_MCU, R142 4.7k, R143 6.49k, PHY1_CLK, GND, Place near P1

PHY1 Address selection: R130 2.49k, R133 2.49k, R145 2.49k, R151 2.20k, R159 2.20k, R160 2.20k, R146 2.49k, R147 2.49k, R161 2.49k, R162 2.49k — PHY1_ADDR=0x1

GPIO69, GPIO70, GPIO64, GPIO65, GPIO66, GPIO71, GPIO44, GPIO63 — R148 33.2, R149 33.2, R150 33.2, R152 33.2, R153 33.2, R154 33.2, R155 33.2, R156 33.2, R157 33.2, R158 33.2

R163 2.49k, GPIO68

R141 4.7k, GPIO76, GPIO62, GPIO27

R91 0 GPIO45, R92 0 GPIO19, R110 0 GPIO73, R144 0 GPIO74, R203 0 GPIO22

C105 2.2uF, C106 0.1uF, C107 4.7pF, C108 4.7pF, C109 4.7pF, C110 4.7pF

PHY1_TD_N, PHY1_TD_P, PHY1_RD_N, PHY1_RD_P

U21 TPD4E05U06DQAR (D1+, D1-, GND, D2+, D2-, NC, NC, NC, NC, GND, GND, NC, NC)

R166, R168, C113 22uF, C114 0.1uF, C115 47uF, C116 0.1uF

RJ2 7498010210A (TD+, TCT, TD-, RD+, RCT, RD-, NC, CHS GND, Shield, Shield)

Place near RJ2: C102 0.1uF, C104 1uF; C111 0.1uF, C112 1uF; C117 0.01uF, R170 1.00M

J1, J2, J3, J6, J4, J5, J7, J8

GPIO59, R167 470, GPIO68, R169 470

ETH1_EARTH

Refer Application Notes for PHY boot strapping configuration:
https://www.ti.com/lit/snla344

Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A		Project Title: LAUNCHXL-F28P65X	
Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf09043e9d42c349720f		Doc No.: 001	Sheet: 6 of 9
Drawn By: Peter Luong		File: MCU117A_EtherCAT.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

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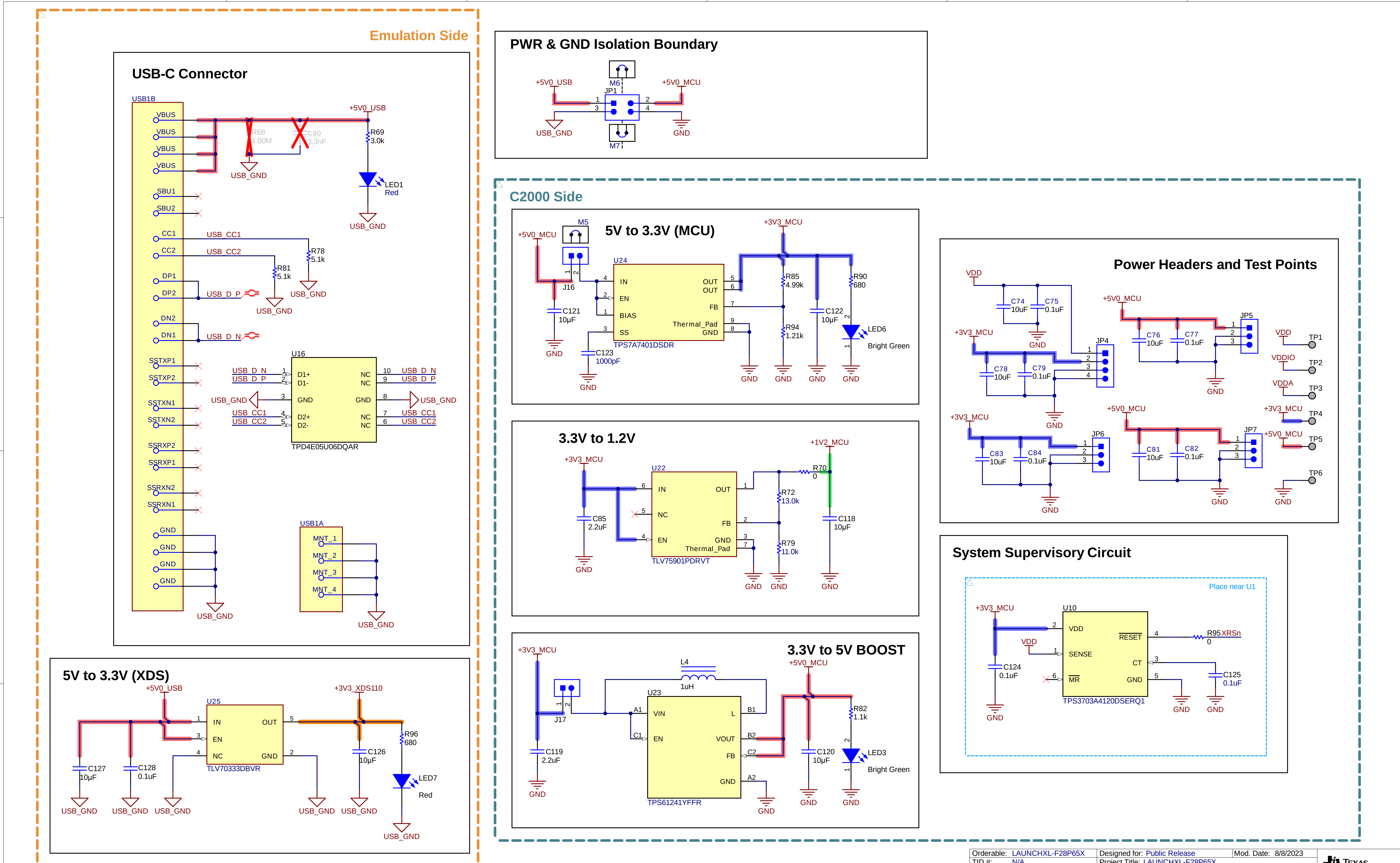

Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A		Project Title: LAUNCHXL-F28P65X	
Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf090		Assembly Variant: 001	Sheet: 7 of 9
Drawn By: Peter Luong		File: MCU117A_USB_and_Power.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

Texas Instruments

http://www.ti.com

XDS110 Device

+3V3_XDS110
R16 3.3k
XDS_RXD
XDS_TXD
XDS_TCK_SWDCLK
XDS_TMS_SWDIO
XDS_TDO_SWO
XDS_TDI
XDS_RESET_OUT
+5V0_USB
R164 100
C131 10000pF
USB_GND
U2A
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5
PC0/TCK/SWCLK
PC1/TMS/SWDIO
PC2/TDI
PC3/TDO/SWO
PC4 PC5 PC6 PC7
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
PK0 PK1 PK2 PK3 PK4 PK5 PK6 PK7
PJ0 PJ1
PH0 PH1 PH2 PH3
PG0 PG1
PF0 PF1 PF2 PF3 PF4
PE0 PE1 PE2 PE3 PE4 PE5
MSP432E401YTPDT
R101 1.00k
R102 1.00k
R103 1.00k
R104 1.00k
DEBUG_ID4
DEBUG_ID5
DEBUG_ID6
DEBUG_ID7
U2B
PL0 PL1 PL2 PL3 PL4 PL5 PL6 PL7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
PP0 PP1 PP2 PP3 PP4 PP5
USB_D_P
USB_D_N
MSP432E401YTPDT
R172 470
R173 470
LED8 Blue
LED9 Blue
U2D
VDD
GND
GNDA
VDDA
VDDC
VREFA+
VBAT
C134 10000pF
C135 10000pF
C136 10000pF
C137 100000pF
C138 100000pF
C139 1uF
C140 1uF
C141 10000pF
C142 1uF
C143 100000pF
C144 1uF
R177 51
C145 100000pF
U2C
WAKE
RST
EN0RXIN
EN0RXIP
EN0TXON
EN0TXOP
HIB
RBIAS
XOSC0
XOSC1
OSC0
OSC1
R174 10k
R175 10k
R176 4.87k
Y1
C147 12pF
C146 12pF

JTAG & UART Digital Isolation

+3V3_XDS110
+3V3_ISO_JTAG
+3V3_MCU
U26
ISO7741DWR
VCC1 VCC2 INA INB INC OUTD EN1 GND1 GND2 OUTA OUTB OUTC IND EN2
XDS_TMS_SWDIO
XDS_TCK_SWDCLK
XDS_TDI
XDS_TDO_SWO
MCU_TMS_INT
MCU_TCK_INT
MCU_TDI_INT
MCU_TDO_INT
C129 0.1uF
C130 0.1uF
R74 0
R97 0 MCU_TMS
R98 0 MCU_TCK
R99 0 MCU_TDI
R100 0 MCU_TDO
U27
ISO7731DWR
VCC1 VCC2 INA INB OUTC EN1 NC GND1 GND2 OUTA OUTB INC EN2 NC GND2
XDS_RESET_OUT
XDS_TXD
XDS_RXD
XDS_RESET_INT
MCU_RXD_INT
MCU_TXD_INT
C132 0.1uF
C133 0.1uF
R76 0
R165 0 MCU_RXD
R171 0 MCU_TXD
USB_GND
GND

Disconnect 0 ohm resistors when connecting to external target.

XDS110 Target Interface

J101A J101B
U4
TPD4E004DRYR
U5
TPD4E004DRYR
IO1 IO2 IO3 IO4 VCC GND

Orderable: LAUNCHXL-F28P65X		Designed for: Public Release	Mod. Date: 8/8/2023
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Number: MCU117	Rev: A	Sheet Title:	
SVN Rev: f3f0c28fbfb7c50f7254bf090		Assembly Variant: 001	Sheet: 8 of 9
Drawn By: Peter Luong		File: MCU117A_XDS110_MCU.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com

FID1 FID2 FID3

FID4 FID5 FID6

MH1 MH2

MH3 MH4

PCB Number: MCU117
PCB Rev: A

Logo1
PCB
LOGO
Texas Instruments

CE Logo1

Logo3
PCB
LOGO
FCC disclaimer

Logo4
PCB
LOGO
WEEE logo

Logo5
PCB
LOGO
Texas Instruments

Logo6
PCB
LOGO
ETHERCAT LABEL

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: LAUNCHXL-F28P65X	Designed for: Public Release	Mod. Date: 8/8/2023
TID #: N/A	Project Title: LAUNCHXL-F28P65X	
Number: MCU117 Rev: A	Sheet Title:	
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