TMS320DM35x Digital Media System-on-Chip (DMSoC) Real Time Out (RTO) Controller

Reference Guide

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Preface: Read Me First

This document describes the Real Time Out (RTO) controller on the DM35x Digital System-on-Chip (DMSoC) .

TMS320DM355 Digital Media System-on-Chip (DMSoC)

Related Documentation From Texas Instruments

The following documents describe the TMS320DM355 Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com. Contact your TI representative for Extranet access.

SPRS463— *TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual* This document describes the overall TMS320DM355 system, including device architecture and features, memory map, pin descriptions, timing characteristics and requirements, device mechanicals, etc.

SPRZ264— TMS320DM355 DMSoC Silicon Errata Describes the known exceptions to the functional specifications for the TMS320DM355 DMSoC.

SPRUFB3— *TMS320DM355 ARM Subsystem Reference Guide* This document describes the ARM Subsystem in the TMS320DM355 Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUED1— *TMS320DM35x DMSoC Asynchronous External Memory Interface (EMIF) Reference Guide* This document describes the asynchronous external memory interface (EMIF) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUED2— *TMS320DM35x DMSoC Universal Serial Bus (USB) Controller Reference Guide* This document describes the universal serial bus (USB) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUED3— *TMS320DM35x DMSoC Audio Serial Port (ASP) Reference Guide* This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

SPRUED4— *TMS320DM35x DMSoC Serial Peripheral Interface (SPI) Reference Guide* This document describes the serial peripheral interface (SPI) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUED9— *TMS320DM35x DMSoC Universal Asynchronous Receiver/Transmitter (UART) Reference Guide* This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUEE0— *TMS320DM35x DMSoC Inter-Integrated Circuit (I2C) Peripheral Reference Guide* This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEE2— *TMS320DM35x DMSoC Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide* This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUEE4— *TMS320DM35x DMSoC Enhanced Direct Memory Access (EDMA) Controller Reference Guide* This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUEE5— *TMS320DM35x DMSoC 64-bit Timer Reference Guide* This document describes the operation of the software-programmable 64-bit timers in the TMS320DM35x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUEE6— *TMS320DM35x DMSoC General-Purpose Input/Output (GPIO) Reference Guide* This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUEE7— *TMS320DM35x DMSoC Pulse-Width Modulator (PWM) Reference Guide* This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUEH7— *TMS320DM35x DMSoC DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide* This document describes the DDR2 / mobile DDR memory controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The DDR2 / mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUF71— TMS320DM35x DMSoC Video Processing Front End (VPFE) Users Guide This document describes the Video Processing Front End (VPFE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF72— TMS320DM35x DMSoC Video Processing Back End (VPBE) Users Guide This document describes the Video Processing Back End (VPBE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF74— TMS320DM35x DMSoC Real Time Out (RTO) Controller Reference Guide This document describes the Real Time Out (RTO) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

The following documents describe TMS320DM35x Digital Media System-on-Chip (DMSoC) that are not available by literature number. Copies of these documents are available (by title only) on the internet at www.ti.com. Contact your TI representative for Extranet access.

— ***TMS320DM35x DDR2 / mDDR Board Design Application Note*** This provides board design recommendations and guidelines for DDR2 and mobile DDR.

— ***TMS320DM35x USB Board Design and Layout Guidelines Application Note*** This provides board design recommendations and guidelines for high speed USB.

Real Time Out (RTO) Controller

1 Introduction

The Real Time Out (RTO) controller works in conjunction with Timer 3 to provide signals to control external components, such as motors.

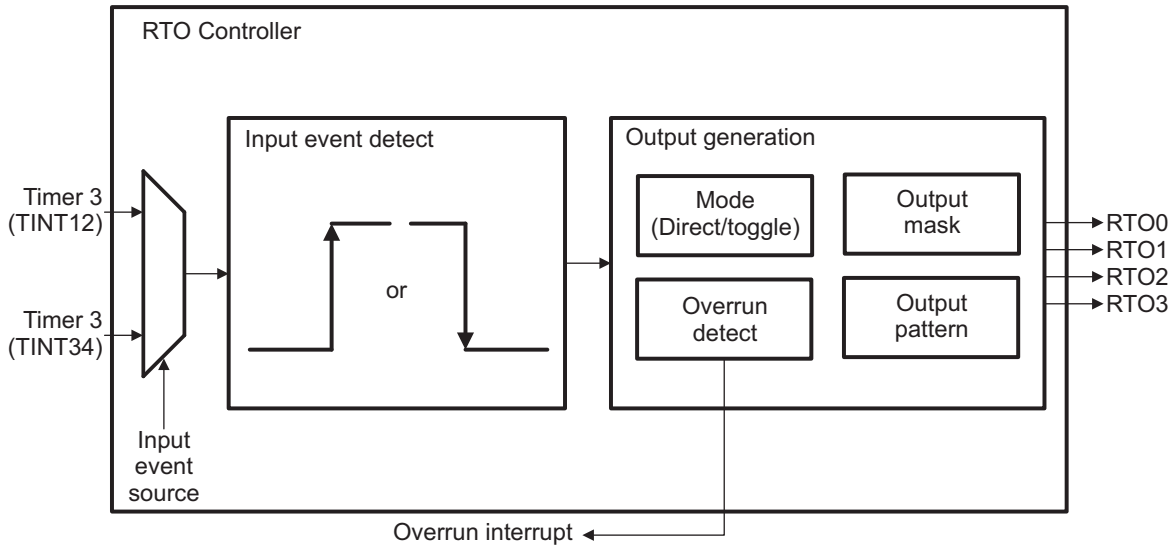
2 Features

The DM35x RTO controller supports the following:

- Trigger on Timer 3 events
- Four separate output signals

3 Functional Block Diagram

The RTO controller takes input from the Timer 3 module and generates output signals on the RTO pins (RTO[3:0]). You can select the input from Timer 3 to be either the signal generated by the Timer 1:2 side or the TImer 3:4 side of Timer 3. The Timer signals are generated when the timer times-out. See *TMS320DM35x DMSoC Timer/Watchdog Timer User's Guide* (literature number SPRUEE5) for additional information on the Timer 3 module.



6 Industry Standard(s) Compliance Statement

The RTO controller does not conform to any recognized industry standards.

Peripheral Architecture

1 Clock Control

The RTO controller is driven by the auxiliary clock of the PLL controller. The frequency of the auxiliary clock is equal to the input reference clock of the PLL controller, and therefore is not affected by the multiplier and divider values of the PLL controller. For more information on device clocking, refer to the *TMS320DM355 DMSoC ARM Subsystem Reference Guide* (literature number SPRUFB3).

2 Signal Descriptions

The RTO controller generates signals on four separate pins: RTO[3:0]. Refer to the *TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual* (literature number SPRS463) for more information on these pins.

3 RTO Output Generation

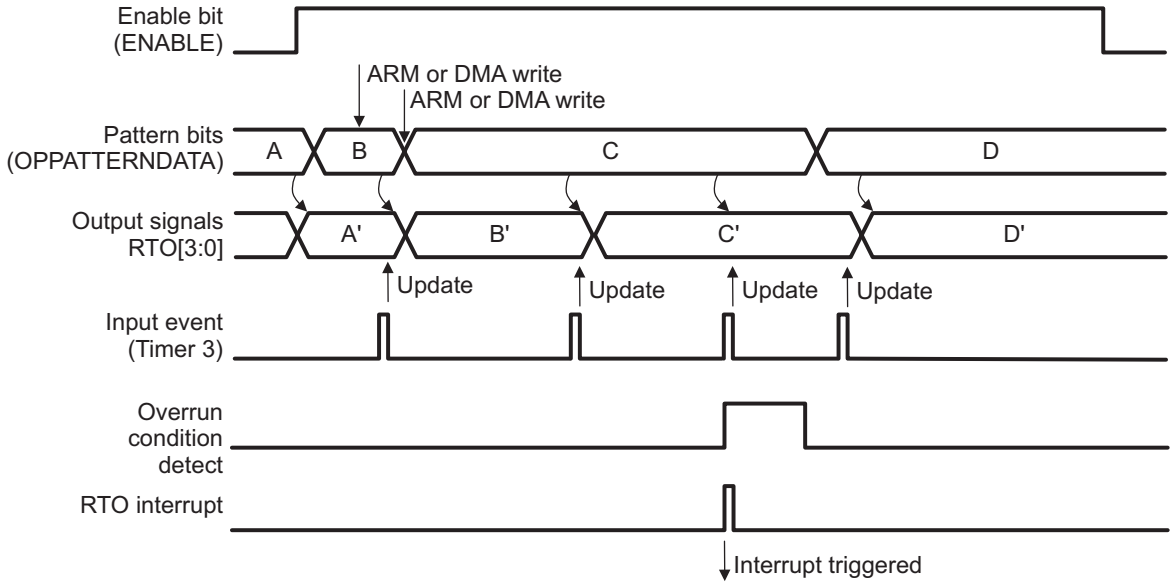
As shown in Section 4, the RTO controller takes input from the Timer 3 module and generates output signals on the RTO pins: RTO[3:0]. Using the select input event source bit (SELECTBIT) in the control and status register (CTRL_STATUS), you can select the input from Timer 3 to be either the signal generated by the Timer 1:2 side or the Timer 3:4 side of Timer 3. The Timer signals are generated when the timer times-out. Using the event condition detect bit (DETECTBIT) in the control and status register (CTRL_STATUS), you can configure the RTO controller to detect the timer events. When these events are detected the RTO controller will change the state of RTO[3:0] depending on the output mode bits (OUTPUTMODE), the output mask bits (OPMASKDATA), and the output pattern bits (OPPATTERNDATA).

The output mode bits (OUTPUTMODE), select the output mode of which there are two options: Direct Out mode and Toggle mode. The output mask bits (OPMASKDATA) determine which RTO output pins (RTO[3:0]) are masked. If a pin is masked, it's state is not changed the next time an input event is detected. The output pattern bits (OPPATTERNDATA) specify the next output pattern on RTO[3:0]. The relationship between these bits and the output pattern on RTO[3:0] is shown in the state table and diagram: Table 1 and Section 4.

The RTO controller generates an interrupt when the output pattern bit field (OPPATTERNDATA) in the control and status register (CTRL_STATUS) is not written prior to receiving the next input event (see Section 4). The status of this interrupt is reflected in the overrun condition bit (OVERRUN) in the control and status register (CTRL_STATUS).

Table 1. RTO Outputs State Table

Mode (OUTPUTMODE)	Mask Bits (OPMASKDATA)	Data Pattern Bits (OPPATTERNDATA)	Previous Pin State (RTO[3:0])	Next Pin State (RTO[3:0])	Description
Direct Out Mode	Masked	x	0	0	No state change when masked
			1	1	
	No mask	0	x	0	Next state forced to 0
	No mask	1	x	1	Next state forced to 1
Toggle Mode	Masked	x	0	0	No state change when masked
			1	1	
	No mask	0	0	0	Next state does not toggle
			1	1	Next state does not toggle
	No mask	1	0	1	Next state toggles
			1	0	Next state toggles



5 Reset Considerations

5.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) causes the RTO controller registers to return to their default state after reset.

5.2 Hardware Reset Considerations

A hardware reset of the processor causes the RTO controller registers to return to their default values after reset.

6 Initialization

To initialize the RTO controller, execute the following steps:

1. Select the input event source polarity (SOURCEPOLARITY): Not inverted or Inverted
2. Select the input event source (SELECTBIT): TINT12 or TINT34
3. Select the input event condition (DETECTBIT): Falling edge. It is recommended to set DETECTBIT to 2h.
4. Select the output mode (OUTPUTMODE): Direct Out Mode or Toggle Mode
5. Configure the output mask (OPMASKDATA)
6. Enable the RTO controller (ENABLE)

7 Interrupt Support

7.1 Interrupt Events and Requests

The RTO controller generates an interrupt when the output pattern bit field (OPPATTERNDATA) in the control and status register (CTRL_STATUS) is not written prior to receiving an input event. The status of this interrupt is reflected in the overrun condition bit (OVERRUN) in the control and status register (CTRL_STATUS).

7.2 Interrupt Multiplexing

The RTO controller is supported by the ARM Interrupt Controller (AINTC) module. The register ARM_INTMUX in the System Control Module must be used to select the interrupt source for multiplexed interrupts. In particular, the RTO interrupt is multiplexed with other interrupts. Refer to the *TMS320DM355 ARM Subsystem Reference Guide* (literature number SPRUFB3) for more information on the System Control Module and ARM Interrupt Controller.

8 EDMA Event Support

The EDMA module has access to the registers of the RTO controller, therefore the EDMA may program the RTO registers. Also, the RTO controller generates an EDMA synchronization event at the same time that it generates an ARM interrupt. For EDMA synchronization events assignment, see the *TMS320DM355 DMSoC ARM Subsystem Reference Guide* (literature number SPRUFB3).

9 Power Management

The RTO controller can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the RTO controller is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM355 DMSoC ARM Subsystem Reference Guide* (literature number SPRUFB3).

10 Emulation Considerations

The RTO controller is not affected by emulation halt events (such as breakpoints). The interface will continue to operate, even if an emulation halt event occurs.

Registers

The RTO controller registers are listed in and described throughout this section.

1 RTO Controller Revision ID Register (REVID)

The RTO controller Revision ID register is shown in Figure 1 and described in Table 2.

Figure 1. RTO Controller Revision ID Register (REVID)

31 30	29 28	27 16
SCHEME	RESERVED	FUNC
R - 1	R - 0	R - 0x4D0

15 11	10 8	7 6	5 0
RTL	MAJOR	CUSTOM	MINOR
R - 0	R - 0	R - 0	R - 3

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2. RTO Controller Revision ID Register (REVID) Field Descriptions

Bit	Field	Value	Description
31 - 30	SCHEME		Scheme value
29 - 28	RESERVED		Reserved
27 - 16	FUNC		Function
15 - 11	RTL		RTL revision
10 - 8	MAJOR		Major number
7 - 6	CUSTOM		Custom
5 - 0	MINOR		Minor Number

2 RTO Controller Control and Status Register (CTRL_STATUS)

The RTO controller Control and Status Register (CTRL_STATUS) is shown in Figure 2 and described in Table 3.

Figure 2. RTO Controller Control and Status Register (CTRL_STATUS)

31	22	21	18	17	16
RESERVED		OUTSTATE		SOURCE POLARITY	OVERRUN
R - 0		R - 0		R/W - 0	R/W - 0

15	12	11	8	7	6	5	4	0
OPMASKDATA		OPPATTERNDATA		OUTPUT MODE	DETECTBIT		SELECTBIT	ENABLE
R/W - 0		R/W - 0		R/W - 0	R/W - 0		R/W - 0	R/W - 0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. RTO Controller Control and Status Register (CTRL_STATUS) Field Descriptions

Bit	Field	Value	Description
31 - 22	RESERVED		Reserved
21 - 18	OUTSTATE		Output signal status. Reflects the actual state of the output pins. The bits in this field [3:0] may to RTO outputs [3:0].
17	SOURCEPOLARITY		Event source bit. Shows the source of the event.
		0	Event source signal is active high
		1	Event source signal is active low
16	OVERRUN		Overrun condition bit. Shows the status of overrun condition.
		0	Overrun condition has not occurred. This bit is cleared by writing 0
		1	Overrun condition has occurred. Writing 1 to this bit has no effect.
15 - 12	OPMASKDATA		Output mask. The bits in this field [3:0] map to RTO outputs [3:0].
		0	Do not change state of output pin.
		1	Change state of output pin depending on output pattern and output mode.
11 - 8	OPPATTERNDATA		Output pattern. The bits in this field [3:0] map to RTO outputs [3:0].
		0	State of '0' on output pin in Direct Out mode. No state change on output pin in Toggle mode. Use bit OUTPUTMODE to select Direct Out mode or Toggle mode.
		1	State of '1' on output pin in Direct Out mode. State is toggled on output pin in Toggle mode. Use bit OUTPUTMODE to select Direct Out mode or Toggle mode.
7	OUTPUTMODE		Output Mode.
		0	Select Direct Out mode
		1	Select Toggle mode
6 - 5	DETECTBIT		Input event condition detect. Select the condition on which the input event will trigger RTO output.
		00	Detect no events
		01	Detect rising edge
		10	Detect falling edge
		11	Detect both rising and falling edge
4 - 1	SELECTBIT		Select input event source:
		0000	Select Timer 1:2 side of Timer 3 to be the input event
		0001	Select Timer 3:4 side of Timer 3 to be the input event
		Others	Reserved
0	ENABLE		RTO Enable
		0	Disable RTO
		1	Enable RTO

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