Technical Article

A Smart Solution to Sequence and Monitor Multiple Power Rails in a System

Yihe

Electronic systems that include a central processing unit (CPU), digital signal processor (DSP), microcontroller (MCU), field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC) can have multiple voltage rails and require certain power on/off sequences in order to function correctly. TI's UCD9090A power-supply sequencer and monitor with Advanced Configuration and Power Interface (ACPI) support can control up to 10 voltage rails, ensures correct power sequences during both normal and fault conditions, and includes a dedicated fault pin to easily cascade multiple devices.

The UCD9090A is an upgrade to the former UCD9090 (listed as not recommended for new designs [NRND]). In this post, I will explain the differences between the two devices, including their operation and features, and how to migrate from the UCD9090 to the UCD9090A. Table 1 lists the features included with the new UCD9090A.

Table 1. Comparison of Features of the UCD9090 and UCD9090A

Features	UCD9090A	UCD9090
Fault pin (enables single to cascading multiple UCD9090A devices)	Yes	No
General Purpose Input (GPI) fault response	Yes	No
GPI debugging	Yes	No
Rail state	Yes	No
Fault/peak logging disable	Yes	No
Logic General Purpose Output (LGPO) sequence on/off dependency	Yes	No
Non-volatile (NV) fault log	26	30
Rail sequence on/off timeout	140m	32s
Cold boot mode	Yes	No

What Is a Fault Pin?

The fault pin is a new feature that enables you to cascade multiple TI UCD9090A devices with fault-pin capability. The fault pin is a bidirectional signal connected to a fault bus. The fault bus is pulled up to 3.3V by a 10K resistor. When no fault exists on a particular UCD9090A device, the fault pin is a digital input pin that listens to the fault bus. When one or multiple UCD9090A devices detect a rail fault, the corresponding fault pin turns to the active driven low state, pulling down the fault bus and informing all other UCD9090A devices of the corresponding fault. This way, coordinated action can occur across multiple devices. After the fault is cleared, the state of the fault pin turns back to an input pin. A diagram showing use of a fault pin is show in Figure 1.

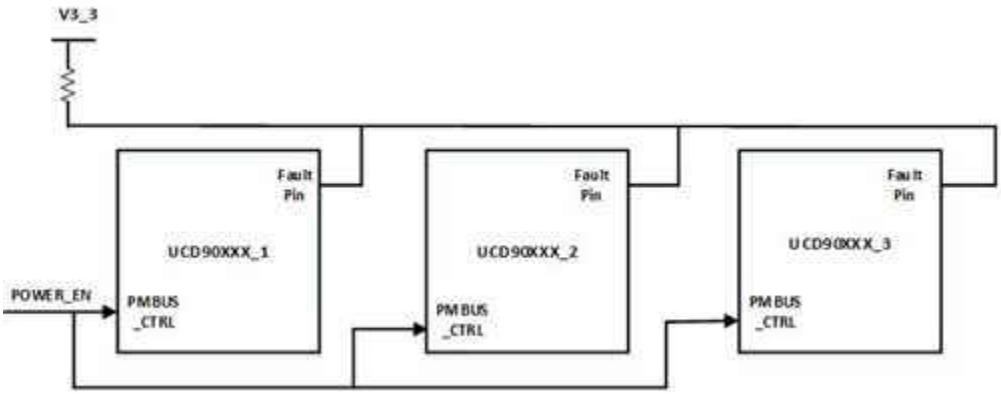

Figure 1. Example Using a Typical Fault Pin

What Is the GPI Fault Response?

This feature solves the issue of limited Analog Monitor (AMON) pins. For example, in the UCD9090, when all 10 rails are assigned to a voltage monitor; the system does not have the capability to monitor one more external event (e.g., OVER_TEMP) or one more rail. With the GPI fault response feature in place, the external event or POWER_GOOD of the point of load (POL) could connect to the assigned GPI. When the signal changes to de-asserted, the UCD9090A can help shut down the rails and retry and re-sequence the system based on how the GPI fault-response is configured.

What Is GPI Debugging?

To avoid triggering the PMBus alert, response fault or continue system watchdog during board-level debug or programming, a GPI pin can be assigned to perform a GPI debugging function on the UCD9090A. When asserting the assigned GPI, the device is under the GPI debug mode. The device will not activate the PMBus alert pin for any faults/warnings nor respond to any fault response. It will not log any faults, will suspend system watchdog and ignore the sequencing dependencies for rails.

What Is the LGPO Sequencing On/off Dependency?

The UCD9090 only supports sequencing dependencies over rail and GPI. If users want to have sequencing dependencies on the LGPO, they have to physically wire the LGPO signal back to one of the GPIs. This approach requires two extra pins which could be an issue for applications that have limited pins available. The LGPO sequencing dependency feature was introduced with the UCD9090A to save the two extra pins for other functions.

What Is the Rail State?

Each device has up to nine states: INIT, IDLE, SEQ_ON, TON_DELAY, RAMP_UP, REGULATED, SEQ_OFF, TOFF_DELAY and RAMP_DOWN. The state of the rail can help you easily determine the status of the system so that you can more easily bring up or debug the power system. Figure 2 shows how the rail states are changed.

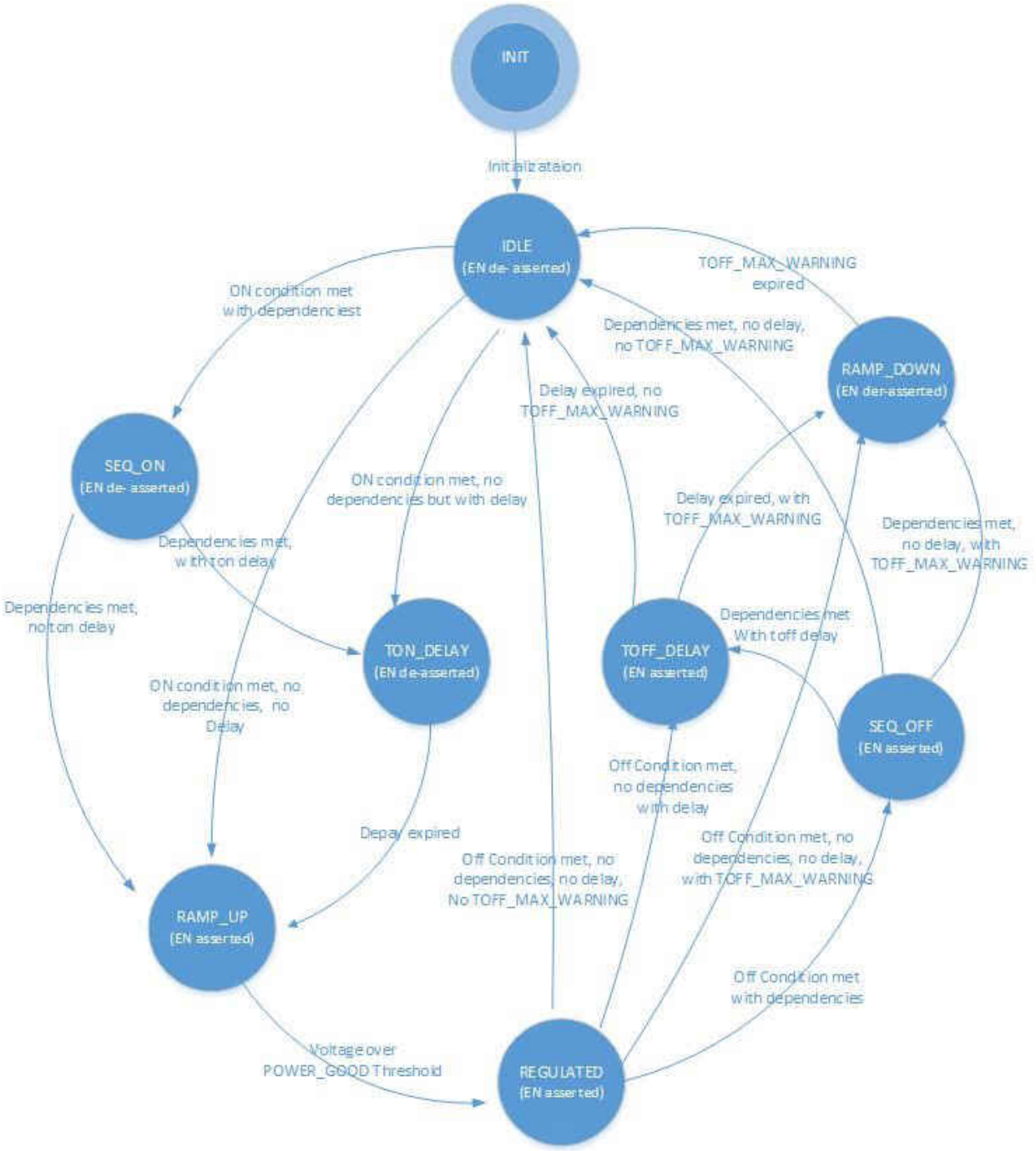

Figure 2. Rail State Machine Diagram

What Is Cold Boot Mode?

Cold boot is a feature specifically designed for cold-temperature applications like telecom. It has the intelligence to heat up a system by turning on the cold boot rails for certain amounts of time when it is experiencing extremely cold temperatures. The UCD9090A device communicates with the system through a particular GPI called the thermal-state GPI, which is a digital output from a thermal sensing device. The cold boot feature is fully configurable, enabling you to select enable/disable, the number of cold boot rails and the timeout period. Figure 3 is a pseudo processing call of how cold-boot is handled by the device.

```
- If system temperature is < threshold degree C (Thermal State GPI)
        o   Yes(DE_ASSERTED):
            § Log GPI fault
            § Start Cold Boot Timeout
            § No System Watchdog output
            § Ramp up the power supplies based on ON_OFF_CONFIG
            § Wait for thermal state GPI ASSERTED OR "Cold Boot Mode Timeout expired"
            § Disable the thermostat input listening mode
            § Force to shutdown down all cold boot rails with EN control immediately
            § Wait all cold boot rails with EN control below POWER_GOOD_OFF
            § Start and Wait "Normal boot Start Delay expired"
- Disable the thermostat input listening mode
- Treated Thermal State GPI as ASSERTED
- Ramp up power supplies based on ON_OFF_CONFIG
```

Figure 3. Cold-boot Processing Call

Will TI Continue to Offer the UCD9090?

Having these new features makes the UCD9090A a better candidate over the UCD9090 for various applications, but note that TI will continue supporting and building the UCD9090 until it reaches ten consecutive years of no sales.

Migrating from the UCD9090 to UCD9090A

The UCD9090 and UCD9090A are pin-to-pin compatible devices. The UCD9090A supports all features of the UCD9090. Moving to the UCD9090A does not require any schematic changes. Moreover, you can seamlessly import the project file (.xml) file generated from the UCD9090 into the UCD9090A with TI's Fusion Digital Power Designer ™ GUI to help reduce the migration effort.

Because of the new features, the script file (.csv) and data flash image file (.hex, .x0) are not compatible between the UCD9090 and UCD9090A. You cannot import files generated from the UCD9090 into the UCD9090A because the device will not function as expected. To use script file or data flash image file on the UCD9090A, follow these steps:

1. Install www.ti.com/tool/fusion_digital_power_designer and open the latest Fusion Digital Power Designer GUI.
2. Import the old UCD9090 project (.xml) into the UCD9090A. See Figure 4.

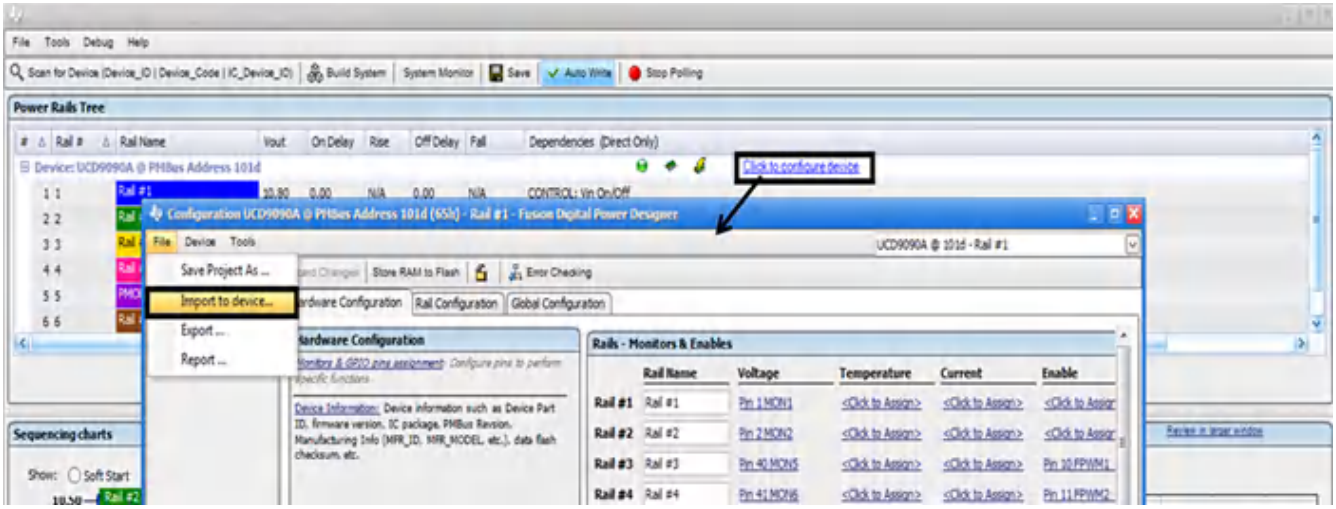

Figure 4. Import the UCD9090 Project File

3. Once you have successfully imported the project, use the export function from the Fusion Digital Power Designer GUI to regenerate the .csv/.hex file. See Figure 5.

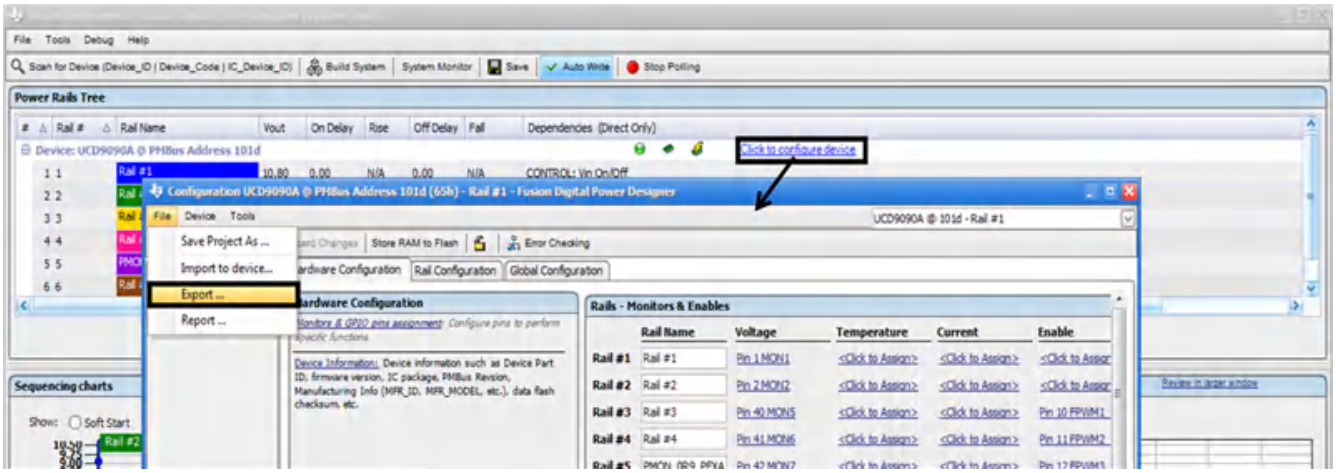

Figure 5. Fusion Digital Power Designer GUI Export Settings

4. Use the .csv/.hex file generated from step No. 3 for any programming utilities.

Hopefully this blog post provides you with a good comparison between the two devices and will help you migrate from the UCD9090 to the UCD9090A. If you have any additional questions, please post a response below or submit through TI's E2E™ Community Sequencers forum.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265