Technical Article

Powering Intel's Xeon D SoC in Servers, Storage and Switches

George Lakkas

Intel's Xeon D chip, developed under the Broadwell-DE code name, is the first Xeon central processing unit (CPU) to bear the system-on-chip (SoC) title by including two physical chips in one package. This 14nm SoC has the cores, memory controllers, L3 cache, dual Ethernet and Peripheral Component Interconnect (PCI) Express 3.0 controllers all on one die.

A second chip – what used to be called Southbridge – includes legacy PCI Express 2.0 peripheral slots and USB/Serial AT Attachment (SATA) ports, and connects to the first chip in the same package through a dedicated link.

The Xeon D SoC makes it possible to develop high-density servers for hyperscale workloads and fits well within cloud infrastructures where servers, storage and networking switches interconnect.

TI's complete power solution for Intel's Xeon D SoCs includes the TPS53631 and TPS53641 VR12.5 driverless 3- and 4-phase pulse-width modulation (PWM) Vcore controllers with the Power Management Bus (PMBus).

You can evaluate the 45W and 65W Xeon D CPU, double-data-rate (DDR) memory core and chipset core multiphase power-supply performance with the TPS53631/TPS53641 evaluation module, shown in Figure 1.

The Vcore controllers are on the east side of the socket, while the power stages and output inductors are on the north side.

The evaluation board has the Intel CPU interposer and socket in order to accept Intel's voltage transient test tool (CPU emulator) for testing. It also has a PMBus connector to configure, control and program the controllers via PMBus, as well as to monitor the input and output voltage, current, power, temperature and report-fault conditions through TI's Fusion Digital Power Designer.

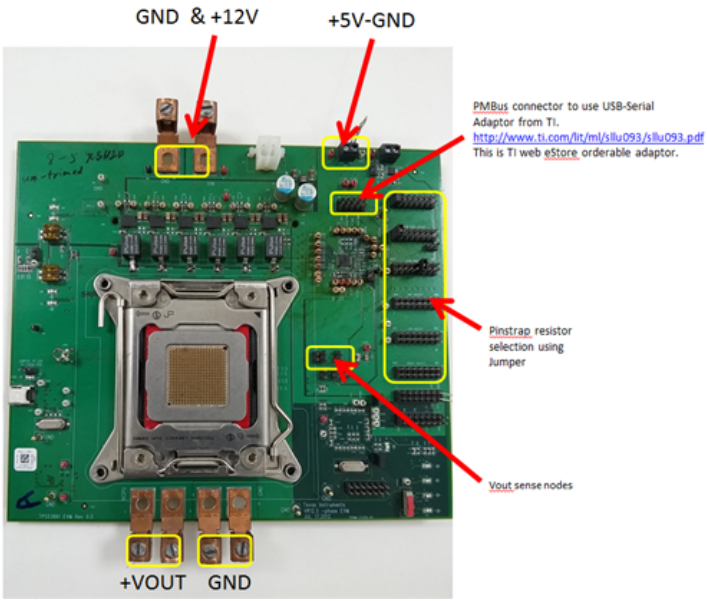

Figure 1. Xeon D System v Interface Definition (SVID) Vcore Power-supply Evaluation Module

Copyright © 2023 Texas Instruments Incorporated

TI has a complete Xeon D TI Designs reference design for the three Intel SVID rails: CPU, DDR core and chipset core. The reference design features:

- Complete three-rail VR12.5 SVID power solution for Intel Xeon D platforms.
- PMBus programming of VID, SoC load line and voltage margining.
- PMBus monitoring of input/output voltage, current, power and temperature.
- Complete test report per Intel test template guidelines – see the load line (output voltage vs. load regulation) example shown in Figure 2.

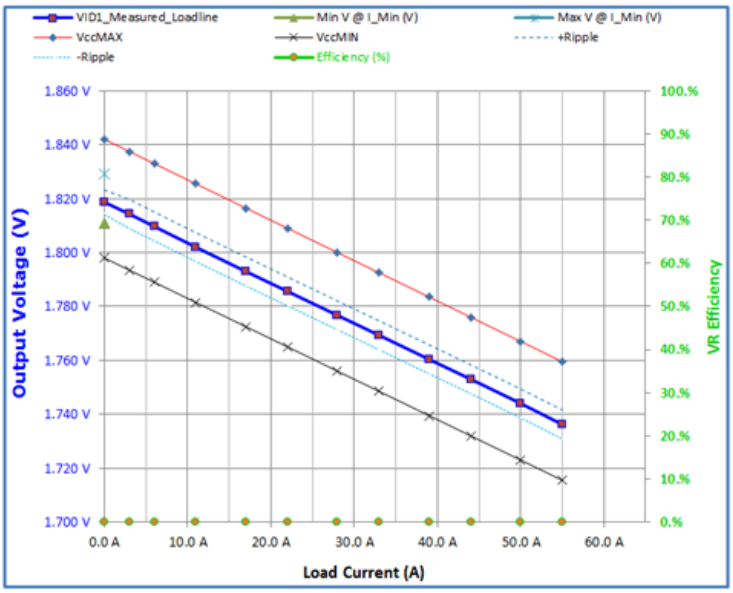

Figure 2. Xeon D SVID Vcore Power-supply Load Line as Tested on the TPS53631/41 Evaluation Module

If you are designing with Intel's Xeon D processors (D-1548, D-1557, D-1567, D-1571 and D-1577), TI has power solution and reference design support tools to enable your high-performance microserver, enterprise switch or storage system. To receive the complete Xeon D TI Designs reference design for the three Intel SVID rails, email vr@list.ti.com.

Copyright © 2023 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated