Technical Article

Issues with Jitter, Phase Noise, Lock Time or Spurs? Check the Loop-filter Bandwidth of Your PLL

Dean Banerjee

As one of the most critical design parameters, the choice of loop bandwidth involves trade-offs between jitter, phase noise, lock time and spurs. The loop bandwidth that is optimal for jitter, BW_{JIT}, can often be the best choice for many clocking applications, such as data converter clocking. In cases where BW_{JIT} is not the best choice, starting there is still the first step to finding the optimal loop bandwidth.

In Figure 1, the offset where the phase-locked loop (PLL) and voltage-controlled oscillator (VCO) noise cross, BW_{JIT} (about 140kHz) optimizes jitter by minimizing the area under the curve.

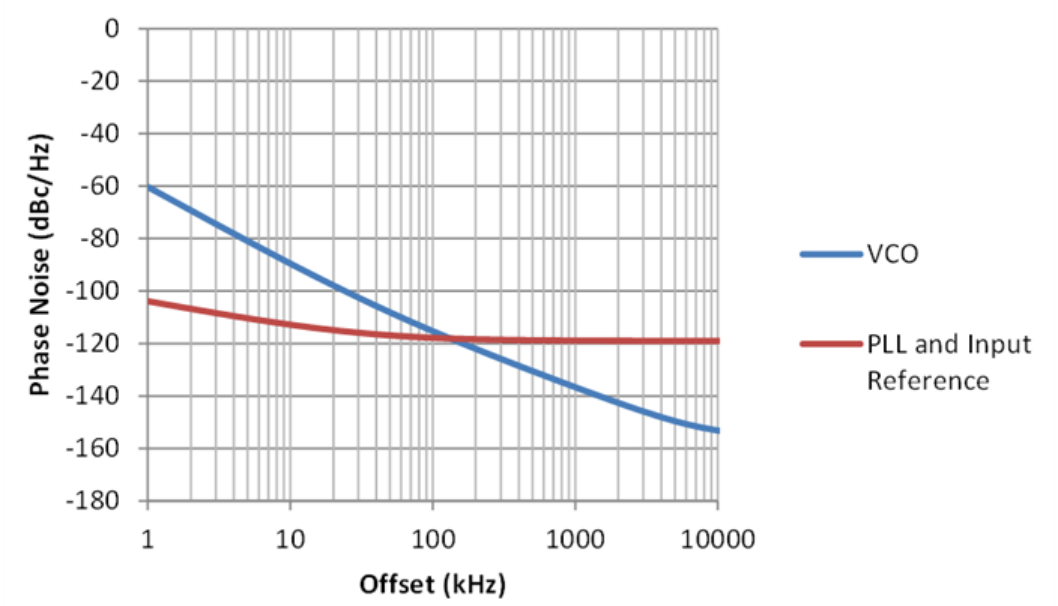

Figure 1. Optimal Jitter Bandwidth

Although this bandwidth, BW_{JIT}, is optimal for jitter, it is not for phase noise, lock time and spurs. Figure 2 gives a relative idea of the impact of loop bandwidth on these performance metrics.

Performance metric	Optimal bandwidth	Comments
Jitter	BW_{JIT}	The optimal value is typically at BW_{JIT}. In some cases where the lower integration limit is higher, sometimes a narrower loop bandwidth might actually be better.
Lock time	Infinite	VCO lock time improves with a wider loop bandwidth until at some point it is either limited by the VCO calibration time (for integrated VCOs) or cannot be made wider due to parasitic capacitances, such as VCO input capacitances.
Spurs	0Hz	Spurs are generally better for narrower loop bandwidths, but at some point, they can be dominated by crosstalk that goes around the loop filter, such as from the board or on the chip.
Phase noise	0Hz or infinite	If the phase noise is less than the optimal jitter bandwidth, it will improve with wider bandwidths until it is just the noise due to the input reference and the PLL. If the phase-noise offset is greater than the optimal jitter bandwidth, it will improve for narrower loop bandwidths until it becomes just free-running VCO noise.

Figure 2. Impact of Loop Bandwidth on Critical Parameters

To illustrate Figure 2, consider the simulation in Figure 3, which shows the effect of varying the loop bandwidth. The lock time and jitter-normalized metrics are the percentage increase from the lowest value shown in Figure 3. The spur and phase-noise metrics are the decibel increase from the lowest value shown in Figure 3.

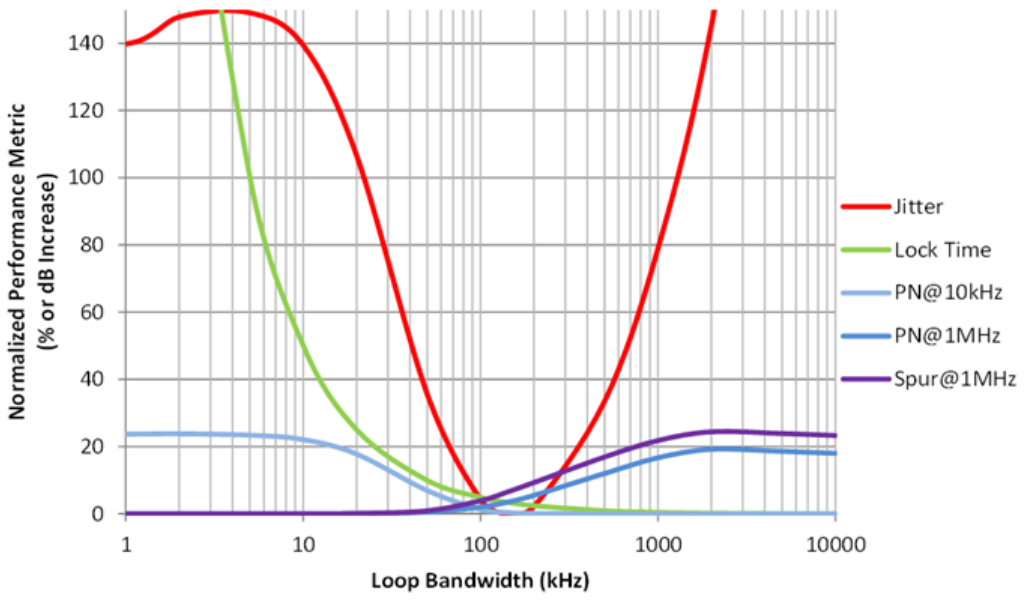

Figure 3. Impact of Loop Bandwidth on Normalized Performance

As Figure 1 predicted, the optimal jitter is indeed best for a loop bandwidth around 140kHz. Increasing the loop bandwidth beyond this benefits lock time and 10kHz phase noise, but degrades the spur and phase noise at 1MHz offset.

Thus, a good approach to choosing loop bandwidth might be to choose the optimal jitter bandwidth (BW_{JIT}) as a starting point, then increase to improve lock time or close in phase noise, or decrease to improve far-out phase noise or spurs.

Have questions about choosing the correct loop bandwidth? Sign in and leave a comment below.

Additional Resources

- Start designing now with the PLL loop bandwidth calculator.
- Download the LMX2592 data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265