TPS80032 Schematic Checklist

Application Report

Literature Number: SWCA291
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Contents

List of Figures

List of Tables

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ABSTRACT

This application note for TPS80032, a power companion device for application processors (see the device data sheet) lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

In addition to this list, customers are advised to use the information in the data sheet, (TI literature number SWCS059).

NOTE: Customer must ensure that the power-up sequence for the application processor is met. This document does not cover the details of the power-up sequence for TPS80032 or the application processor. Refer to the device data sheet and the reference designs for the application processors for the correct power-up sequence requirements.

1 TPS80032 Schematic Checklist

Table 1. Charger

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type BLUE: power path used RED: power path not used	Expected Components BLUE: power path used RED: power path not used
CHRG_BOOT	Analog	Output	No	Floating	Capacitor to CHRG_SW	100nF
CHRG_CSIN	Analog	Input	No	Tied to common ground	Capacitor to CHRG_PGND	
CHRG_CSOUT	Analog	Input	No	Tied to VSYS	"Resistor to CHRG_CSIN, Shorted to CSIN	68 mΩ
					Capacitor to CHRG_PGND	1 µF
CHRG_DET_N	Analog	Input	No	Tied to common ground	N/A	
CHRG_EXTCHRG_ENZ	Digital	Output	No	Floating	N/A	
CHRG_EXTCHRG_STATZ	Digital	Input	PU	Floating or Tied to VRTC, (fixed internal pullup to VRTC)	N/A	
CHRG_LED_IN	Power	Input	No	Tied to common ground	N/A	
CHRG_LED_TEST	Analog	In / Out	No	Tied to common ground or floating	LED to CHRG_PGND	
CHRG_PGND_B1	Ground	Input	No	Tied to common ground	N/A	
CHRG_PGND_B2	Ground	Input	No	Tied to common ground	N/A	
CHRG_PGND_B3	Ground	Input	No	Tied to common ground	N/A	
CHRG_PMID_B1	Analog	Output	No	Floating	Capacitor to CHRG_PGND	4.7 µF
CHRG_PMID_B2	Analog	Output	No	Floating		
CHRG_PMID_B3	Analog	Output	No	Floating		
CHRG_SW_B1	Power	Output	No	Floating	Inductor to CSIN	1 µH
CHRG_SW_B2	Power	Output	No	Floating		
CHRG_SW_B3	Power	Output	No	Floating		
CHRG_SW_B4	Power	Output	No	Floating		
CHRG_SW_B5	Power	Output	No	Floating		
CHRG_VREF	Analog	Output	No	Floating	Capacitor to CHRG_PGND	1 µF
VAC	Power	Input	No	Tied to common ground, if not used in BBS	Optional capacitor	100 nF
VBUS_B1	Power	In / Out	No	Tied to common ground (If also not used by BBS, OTG)	Capacitor to CHRG_PGND, USB connector / ESD Protection	4.7 µF
VBUS_B2	Power	In / Out	No			
VBUS_B3	Power	In / Out	No			
CHRG_VSYS	Power	Input	No	Tied to VSYS	Shorted to CHRG_CSOUT Capacitor to CHRG_PGND	10 µF

Table 1. Charger (continued)

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type BLUE: power path used RED: power path not used	Expected Components BLUE: power path used RED: power path not used
CHRG_VBAT	Power	In / Out	No	Tied to VSYS or VBAT	Shorted to CHRG_VSYS PMOS FET drain(source is connected to CHRG_VSYS)	PMOS FET (see SWCS059 for references)
VBUS_DET	Digital	Output	No	Floating		
CHRG_GATE_CTRL	Analog	Output	No	Floating	PMOS FET gates capacitor to CHRG_VSYS	PMOS FET (see SWCS059 for references) 4.7 nF
CHRG_PROT_GATE	Analog	Output	No	Floating	Protection FET gate(OPTION)	See SWCS059

Table 2. A+B223 Analog Sub Group

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
GND_ANA_B1	Ground	Input	No	Tied to common ground	N/A	
GND_ANA_B2	Ground	Input	No	Tied to common ground	N/A	
GND_ANA_B3	Ground	Input	No	Tied to common ground	N/A	
GND_ANA_B4	Ground	Input	No	Tied to common ground	N/A	
GND_DIG_VIO	Ground	Input	No	Tied to common ground	N/A	
GND_DIG_VRTC	Ground	Input	No	Tied to common ground	N/A	
PBKG_B1	Substrate	Input	No	Tied to common ground	N/A	
PBKG_B2	Substrate	Input	No	Tied to common ground	N/A	
PBKG_B3	Substrate	Input	No	Tied to common ground	N/A	
PBKG_B4	Substrate	Input	No	Tied to common ground	N/A	
VDD_B1	Power	Input	No	N/A	Tank capacitor	
VDD_B2	Power	Input	No	N/A	Tank capacitor	
VDD_B3	Power	Input	No	N/A	Tank capacitor	
VDD_B4	Power	Input	No	N/A	Tank capacitor	
VIO	Power	Input	No	N/A	Optional capacitor to GND_DIG_VIO	
VPROG	Power	Input	No	Tied to common ground	N/A	

Table 3. Backup

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
VBACKUP	Analog	Input	No	Tied to common ground (Preferred), Or Floating	Coin cell or capacitor to ground	XH414H-IV01E or equivalent 2.2 µF
VSYS_BB	Power	Input	No	N/A	Tank capacitor	

Table 4. Clock

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
CLK32KAO	Digital	Output	No	Floating	N/A	
CLK32KAUDIO	Digital	Output	No	Floating	N/A	
CLK32KG	Digital	Output	No	Floating	N/A	
OSC32KCAP	Analog	Output	No	Floating (degrading CLK32KAUDIO clock)	Capacitor to REFGND	2.2 µF
OSC32KIN	Analog	Input	No	Digital clock input, Analog clock input	Crystal to OSC32KOUT, Capacitor to REFGND	12 pF
OSC32KOUT	Analog	Output	No	Floating when digital clock input, Capacitor when analog clock input	Capacitor to REFGND	12 pF

Table 5. Reference

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
IREF	Analog	In / Out	No	N/A	Resistor to REFGND	510 kΩ
REFGND_B1	Ground	Input	No	Tied to common ground	N/A	
REFGND_B2	Ground	Input	No			
VBG	Analog	Output	No	N/A	Capacitor to REFGND	100 nF

Table 6. Test

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
TESTEN	Digital	Input	PD	Tied to common ground, (fixed internal pulldown to ground)	N/A	
TESTV	Analog	Output	No	Floating	N/A	

Table 7. I2C (CTRL)

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
CTLI2C_SCL	Digital	In / Out	PU	N/A	Resistor to VIO	
CTLI2C_SDA	Digital	In / Out	PU	N/A	Resistor to VIO	

Table 8. Interrupt

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
INT	Digital	Output	No	Floating	N/A	

Table 9. Power Management

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
BATREMOVAL	Digital	Output	No	Floating	N/A	
BOOT0	Digital	Input	No	Tied to common ground or VRTC	N/A	
BOOT1	Digital	Input	No	Tied to common ground or VRTC	N/A	
BOOT2	Digital	Input	No	Tied to common ground or VRTC	N/A	
NRESPWRON	Digital	Output	No	Floating	N/A	
NRESWARM	Digital	Input	PU	Floating, (fixed internal pullup to VIO)	N/A	
PREQ1	Digital	Input	PU/PD (Default)	Floating (use of internal PU/PD) Or tied to common ground or VIO (depending on selected sensitivity)	N/A	
PREQ2	Digital	Input	PU/PD (Default)	Floating (use of internal PU/PD), Or tied to common ground or VIO (depending on selected sensitivity)	N/A	
PREQ3	Digital	Input	PU/PD (Default)	Floating (use of internal PU/PD), Or tied to common ground or VIO (depending on selected sensitivity)	N/A	
PWM1	Digital	Output	No	Floating	N/A	
PWM2	Digital	Output	No	Floating	N/A	
PWRON	Digital	Input	PU	N/A	N/A	
REGEN1	Digital	Output	No	Floating	N/A	
REGEN2	Digital	Output	No	Floating	N/A	
RPWRON	Digital	Input	PU	Internal pullup on VSYS	N/A	
SYSEN	Digital	Output	No	Floating	N/A	

Table 10. MSECURE

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
MSECURE	Digital	Input	PD	Tied to common ground or Floating (Internal pulldown)	N/A	

Table 11. Smart Reflex

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
DVSI2C_SCL	Digital	In / Out	PU	Internal pullup on VIO	Resistor to VIO	
DVSI2C_SDA	Digital	In / Out	PU	Internal pullup on VIO	Resistor to VIO	

Table 12. Detection

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
ID	Analog	In / Out	PU/PD	Floating (Internal pullup to VUSB)	USB connector / ESD Protection	
MMC	Digital	Input	PU, PD (Default)	Internal pullup to VIO or pulldown to ground	N/A	
SIM	Digital	Input	"PU, PD (Default)"	Internal pullup to VIO or pulldown to ground	N/A	

Table 13. LDO

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
VANA	Power	Output	No	N/A	Capacitor to GND_ANA_B5	2.2 µF
VANA_IN	Power	Input	No	VSYS	Optional capacitor	
LDO2	Power	Output	No	Floating	Capacitor to GND_ANA_B1	2.2 µF
LDO2_IN	Power	Input	No	VSYS	Optional capacitor	
LDO4	Power	Output	No	Floating	Capacitor to GND_ANA_B2	2.2 µF
LDO4_IN	Power	Input	No	VSYS	Optional capacitor	
LDO3	Power	Output	No	Floating	Capacitor to GND_ANA_B1	2.2 µF
LDO3_IN	Power	Input	No	VSYS	Optional capacitor	
LDO6	Power	Output	No	Floating	Capacitor to GND_ANA_B3	2.2 µF
LDO6_IN	Power	Input	No	VSYS	Optional capacitor	
LDOLN	Power	Output	No	Floating	Capacitor to GND_ANA_B3	2.2 µF
LDLN_IN	Power	Input	No	VSYS	Optional capacitor	
LDO5	Power	Output	No	Floating	Capacitor to GND_ANA_B4	2.2 µF

Table 13. LDO (continued)

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
LDO5_IN	Power	Input	No	VSYS	Optional capacitor	
LDO1	Power	Output	No	Floating	Capacitor to GND_ANA_B6	2.2 µF
LDO1_IN	Power	Input	No	VSYS	Optional capacitor	
VRTC	Power	Output	No	N/A	Capacitor to GND_ANA_B4	2.2 µF
VRTC_IN	Power	Input	No	VSYS	Optional capacitor	
LDOUSB	Power	Output	No	Floating	Capacitor to GND_ANA_B5	2.2 µF
LDO7	Power	Output	No	Floating	Capacitor to GND_ANA_B5	2.2 µF
LDO7_IN	Power	Input	No	VSYS	Optional capacitor	

Table 14. Gas Gauge

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
GGAUGE_RESN	Analog	Input	No	Tied to common ground	N/A	20 mΩ
GGAUGE_RESP	Analog	Input	No	Tied to common ground	Resistor to GGAUGE_RESN	

Table 15. GPADC

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
GPADC_IN0	Analog	In / Out	No	Tied to ground / VRTC (No Chg)	N/A	
GPADC_IN1	Analog	In / Out	No	Tied to common ground	N/A	
GPADC_VREF1	Analog	Output	No	Floating	N/A	
GPADC_IN2	Analog	Input	No	Tied to common ground	N/A	
GPADC_IN3	Analog	Input	No	Tied to common ground	N/A	
GPADC_IN4	Analog	In / Out	No	Tied to common ground	N/A	
GPADC_IN5	Analog	Input	No	Tied to common ground	N/A	
GPADC_IN6	Analog	Input	No	Tied to common ground	N/A	
GPADC_START	Digital	Input	PD	Tied to common ground	N/A	

Table 16. Non Smart Reflex

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
SMPS4_FDBK	Analog	Input	No	Tied to common ground	Capacitor to SMPS4_GND	10 µF / 1 µH
SMPS4_GND_B1	Ground	Input	No	Tied to common ground	N/A	

Table 16. Non Smart Reflex (continued)

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
SMPS4_GND_B2	Ground	Input	No	Tied to common ground	N/A	
SMPS4_IN_B1	Power	Input	No	VSYS	Capacitor to SMPS4_GND	4.7 µF
SMPS4_IN_B2	Power	Input	No	VSYS	Capacitor to SMPS4_GND	
SMPS4_SW_B1	Power	Output	No	Floating	Inductor to SMPS4_FDBK	
SMPS4_SW_B2	Power	Output	No	Floating	Inductor to SMPS4_FDBK	
SMPS3_FDBK	Analog	Input	No	Tied to common ground	Capacitor to SMPS3_GND	10 µF/1 µH
SMPS3_GND_B1	Ground	Input	No	Tied to common ground	N/A	
SMPS3_GND_B2	Ground	Input	No	Tied to common ground	N/A	
SMPS3_IN_B1	Power	Input	No	VSYS	Capacitor to SMPS3_GND	4.7 µF
SMPS3_IN_B2	Power	Input	No	VSYS	Capacitor to SMPS3_GND	
SMPS3_SW	Power	Output	No	Floating	Inductor to SMPS3_FDBK	

Table 17. Smart Reflex

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
SMPS1_FDBK	Analog	Input	No	Tied to common ground	Capacitor to SMPS1_GND	22 µF / 1 µH (2*22 µF in case of 5A version)
SMPS1_GND_B1	Ground	Input	No	Tied to common ground	N/A	
SMPS1_GND_B2	Ground	Input	No	Tied to common ground	N/A	
SMPS1_GND_B3	Ground	Input	No	Tied to common ground	N/A	
SMPS1_GND_B4	Ground	Input	No	Tied to common ground	N/A	
SMPS1_IN_B1	Power	Input	No	VSYS	Capacitor to SMPS1_GND	4.7 µF
SMPS1_IN_B2	Power	Input	No	VSYS	Capacitor to SMPS1_GND	
SMPS1_IN_B3	Power	Input	No	VSYS	Capacitor to SMPS1_GND	
SMPS1_SW_B1	Power	Output	No	Floating	Inductor to SMPS1_FDBK	
SMPS1_SW_B2	Power	Output	No	Floating	Inductor to SMPS1_FDBK	
SMPS1_SW_B3	Power	Output	No	Floating	Inductor to SMPS1_FDBK	
SMPS1_SW_B4	Power	Output	No	Floating	Inductor to SMPS1_FDBK	
SMPS2_FDBK	Analog	Input	No	Tied to common ground	Capacitor to SMPS2_GND	10 µF, 1 µH
SMPS2_GND_B1	Ground	Input	No	Tied to common ground	N/A	
SMPS2_GND_B2	Ground	Input	No	Tied to common ground	N/A	
SMPS2_IN_B1	Power	Input	No	VSYS	Capacitor to SMPS2_GND	4.7 µF
SMPS2_IN_B2	Power	Input	No	VSYS	Capacitor to SMPS2_GND	

Table 17. Smart Reflex (continued)

Ball / Pad Macrocell (BPM)	Type	I/O	PU/PD	Connection When Not Used	Component Type	Expected Components
SMPS2_SW_B1	Power	Output	No	Floating	Inductor to SMPS2_FDBK	
SMPS2_SW_B2	Power	Output	No	Floating	Inductor to SMPS2_FDBK	
SMPS2_SW_B3	Power	Output	No	Floating	Inductor to SMPS2_FDBK	
SMPS5_FDBK	Analog	Input	No	Tied to common ground	Capacitor to SMPS5_GND	10 µF / 1 µH
SMPS5_GND_B1	Ground	Input	No	Tied to common ground	N/A	
SMPS5_GND_B2	Ground	Input	No	Tied to common ground	N/A	
SMPS5_IN_B1	Power	Input	No	VSYS	Capacitor to SMPS5_GND	4.7 µF
SMPS5_IN_B2	Power	Input	No	VSYS	Capacitor to SMPS5_GND	
SMPS5_SW	Power	Output	No	Floating	Inductor to SMPS5_FDBK	

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