

## CC2541-Q1 Errata Note

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This document provides information about known issues of the CC2541-Q1 system-on-chip (SoC).

### 1 Known Issue

[Table 1](#) summarizes the known issue.

**Table 1. Summary of Known Issue**

Issue ID	Title
1	Leaving PM2 or PM3 can produce glitches on the SCL and SDA pins.

#### 1.1 *Issue 1: Leaving PM2 or PM3 can Produce Glitches on the SCL and SDA Pins*

Glitches can occur on the SCL and SDA pins when leaving PM2 or PM3.

##### 1.1.1 Issue Description

The SCL and SDA I2C pins must be high impedance with pullup when not transmitting on the I2C bus. This issue can cause a low pulse for approximately 250 ns when going from PM2 or PM3 to active mode. This issue is due to an insufficient reset of the I2C module when exiting PM2 or PM3.

##### 1.1.2 Suggested Workarounds

To prevent these glitches, the I2C pin override bit (I2CWC.OVR) can be set before entering PM2. This bit overrides the I2C module control of the I/O lines and sets them to the state defined in I2CWC. The I/O lines must then be left in the reset state for I2CWC, which is input with pullup enabled. The I2CWC.OVR bit can be cleared just after returning to active mode, which prevents any glitches from propagating to the pins.

## 2 Revision History

Literature Number	Date	Description of Changes
SWRZ059*	April 2015	Initial release

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