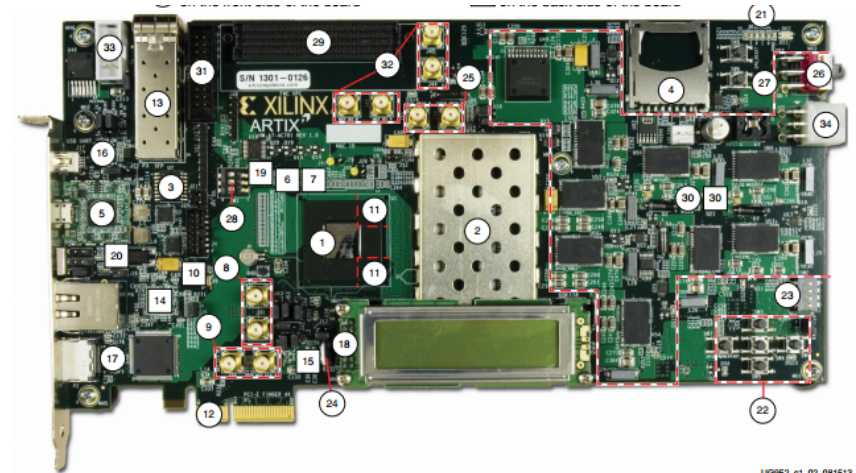


BOM

**TI Power Reference Design for
Xilinx® Artix®-7**

• Xilinx Artix-7 FPGA AC701 Evaluation Kit

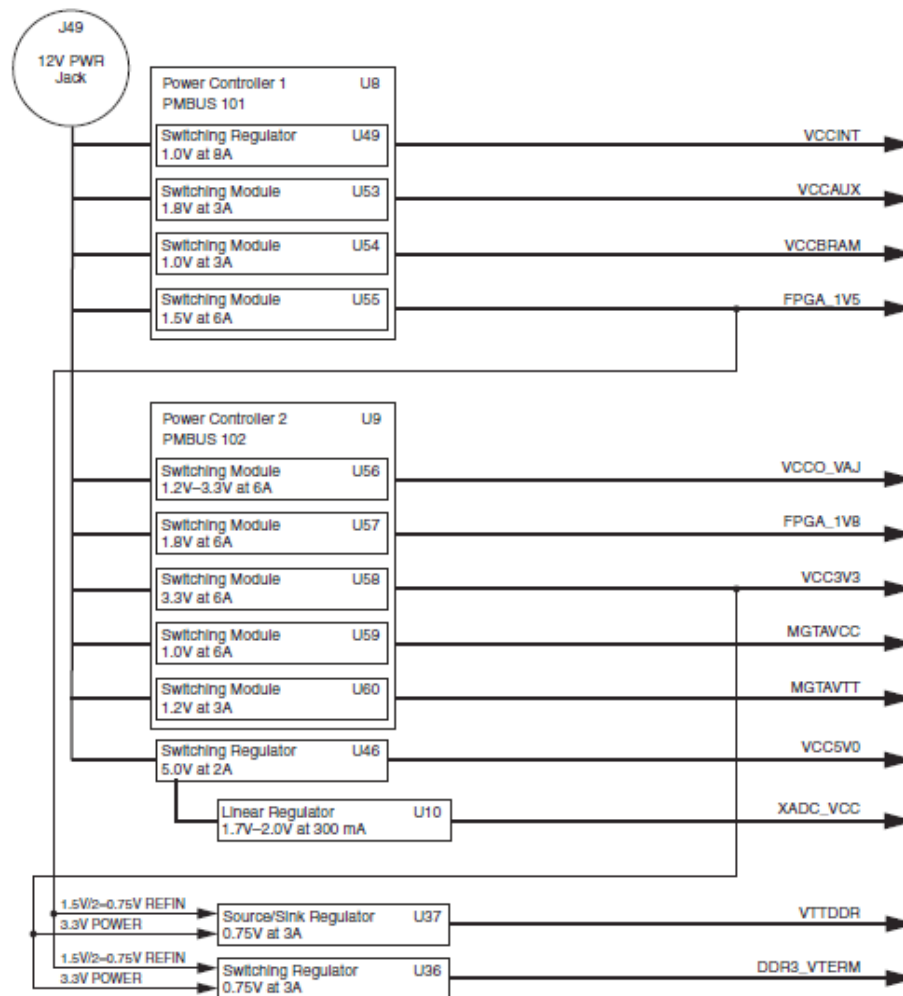
- BOM for AC701
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AC701 Evaluation Kit Power Tree - 1



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AC701 Evaluation Kit Power Tree - 2

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
UCD90120A (4 Rails)	U8	PMBus Controller - PMBus Addr = 101			39
LMZ22010TZ	U49	10A 0.8V - 6V Adj. Switching Regulator	VCCINT	1.00V	40
TPS84621RUQ	U53	6A 0.6V - 5.5V Adj. Switching Regulator	VCCAUX	1.80V	41
TPS84320RUQ	U54	3A 0.6V - 5.5V Adj. Switching Regulator	VCCBRAM	1.00V	42
TPS84621RUQ	U55	6A 0.6V - 5.5V Adj. Switching Regulator	FPGA_1V5	1.50V	43
UCD90120A (5 Rails)	U9	PMBus Controller - PMBus Addr = 102			45
TPS84621RUQ	U56	6A 0.6V - 5.5V Adj. Switching Regulator	VCCO_VADJ	2.50V	46
TPS84320RUQ	U57	3A 0.6V - 5.5V Adj. Switching Regulator	VCC1V8/ FPGA_1V8	1.80V	47
TPS84621RUQ	U58	6A 0.6V - 5.5V Adj. Switching Regulator	VCC3V3/ FPGA_3V3	3.30V	48
TPS84320RUQ	U59	3A 0.6V - 5.5V Adj. Switching Regulator	MGTAVCC	1.00V	49
TPS84320RUQ	U60	3A 0.6V - 5.5V Adj. Switching Regulator	MGTAVTT	1.20V	50
LMZ12002	U46	2A 0.8V - 6V Adj. Linear Regulator	VCC5V0	5.00V	34
TL1963ADCQR	U62	1.5A 1.21V - 5V Adj. LDO Linear Regulator	VCC2V5	2.50V	48
TPS51200DR	U37	3A Source-Sink DDR Termination Regulator	VTTDDR	0.75V	44
TPS51200DR	U36	3A Source-Sink DDR Termination Regulator	DDR3_VTERM_ R_0V75	0.75V	44
TPS79433DCQ	U61	0.25A 1.2V - 5.5V Adj. LDO Linear Regulator	V33D_CTL1	3.30V	39
TPS79433DCQ	U63	0.25A 1.2V - 5.5V Adj. LDO Linear Regulator	V33D_CTL2	3.30V	45
ADP123	U10	0.3A 0.8V - 5V Adj. Linear Regulator	XADC_VCC	1.85V	29
REF3012	U35	50uA Fixed 1.25V Voltage Reference	XADC_VREF	1.25V	29

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