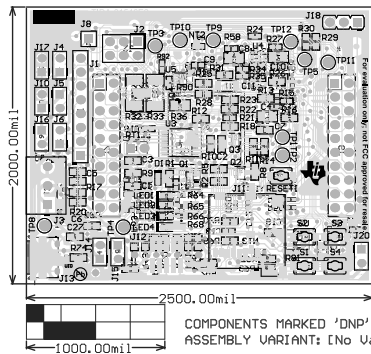


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.  
 Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.  
 Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.  
 Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 8 MIL  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTIE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:  
 Change in menu Project|Project Options|Parameters

DESIGNED FOR:  
 Public Release

FILE NAME:  
 TIDA-01546 Proj\_PCB.PcbDoc

ADG HAS BEEN REVISED FOR BOARD	CS	BOARD # 710A-01546	DATE: E2	SUN FEB 16 2008 10:58:08 AM
LAYER NAME = TOP OVERLAY		TID #: 710A-01546	# DIT	
PLOT NAME = Top Layer	Composite	GENERATED: 7/22/08 10:58:08 AM	COMPTON, TEXAS	INSTRUMENTS, LLP

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ENGINEER:  
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LAYOUT BY:  
 Whaddid the Layout?

SCALE: 1.00

ALTIUM DESIGNER VERSION:  
 16.1.9.221

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