Test Report: PMP30916

–8-V Inverting Buck-Boost Reference Design

Description

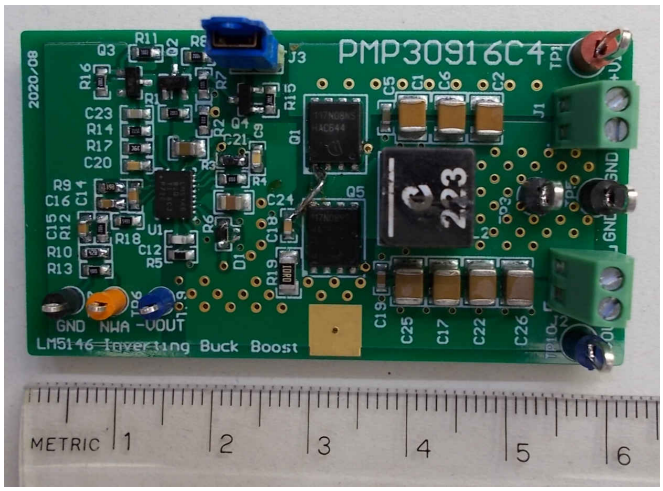
The LM5146-Q1 is used in this design as inverting buck-boost topology, generating –8 V out of the telecom input of +9 V to +56 V. By topology the controller is negative referenced, so a level shifter was added to provide an ENABLE function. The switching frequency of 400 kHz is a trade-off between switching losses and a reasonable board size.

Features

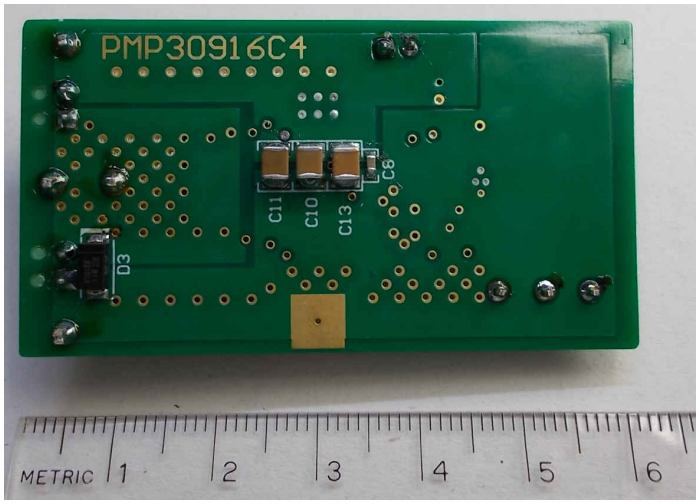
- Wide input voltage range supports telecom, industrial, and truck applications
- If using 100-V transistors, the circuit can withstand high load dump
- Output can be modified from –5 V to –15 V

Applications

- Active antenna system mMIMO (AAS)



Top Photo



Bottom Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Topology	Inverting Buck Boost
Input Voltage	9 V to 56 V
Output Voltage	–8 V
Maximum Output Current	2 A
Switching Frequency	400 kHz
IC	LM5146-Q1

1.2 Considerations

Note

For bode plot measurements, see the schematic about the correct connections (GND of the PCB must be connected to the positive input of the network analyzer).

A powered board may be hot.

Measurements were taken with R3 and R6 shorted.

Switching frequency of prototype = 408 kHz.

1.3 Dimensions

The size of the board is 58.4 mm × 31.7 mm. The 4-layer board was manufactured with the outer layers with 2-oz copper and inner layers with 1-oz copper thickness.

2 Testing and Results

2.1 Efficiency

Efficiency of the PMP30916 is shown in the following figure.

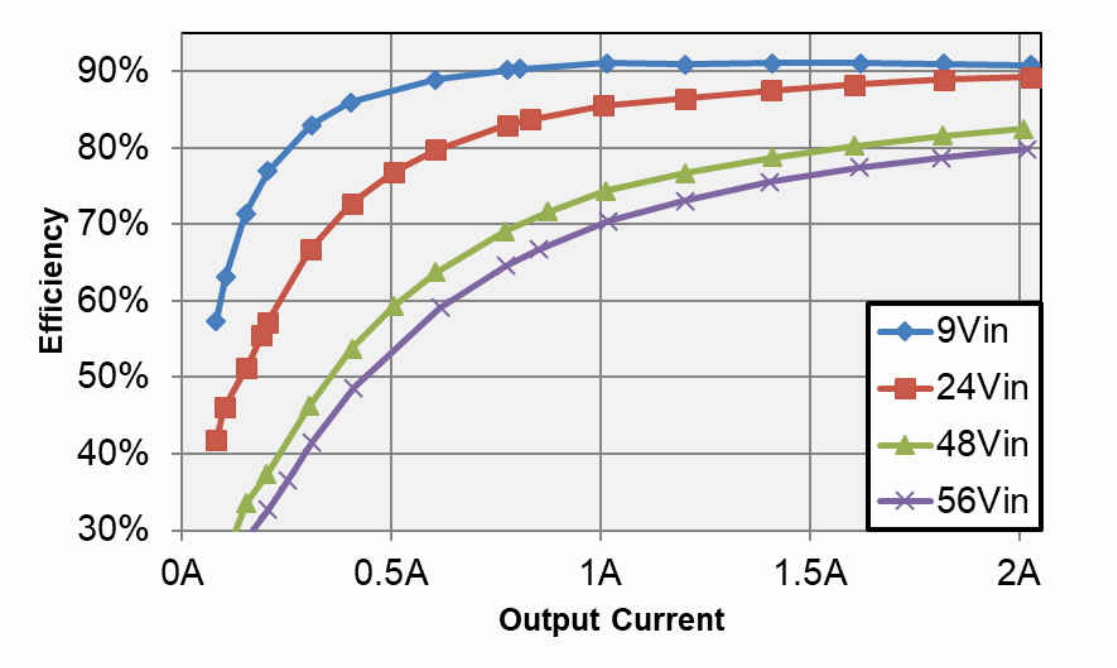


Figure 2-1. Efficiency vs Output Current

2.2 Loss

The following image shows the PMP30916 loss graph.

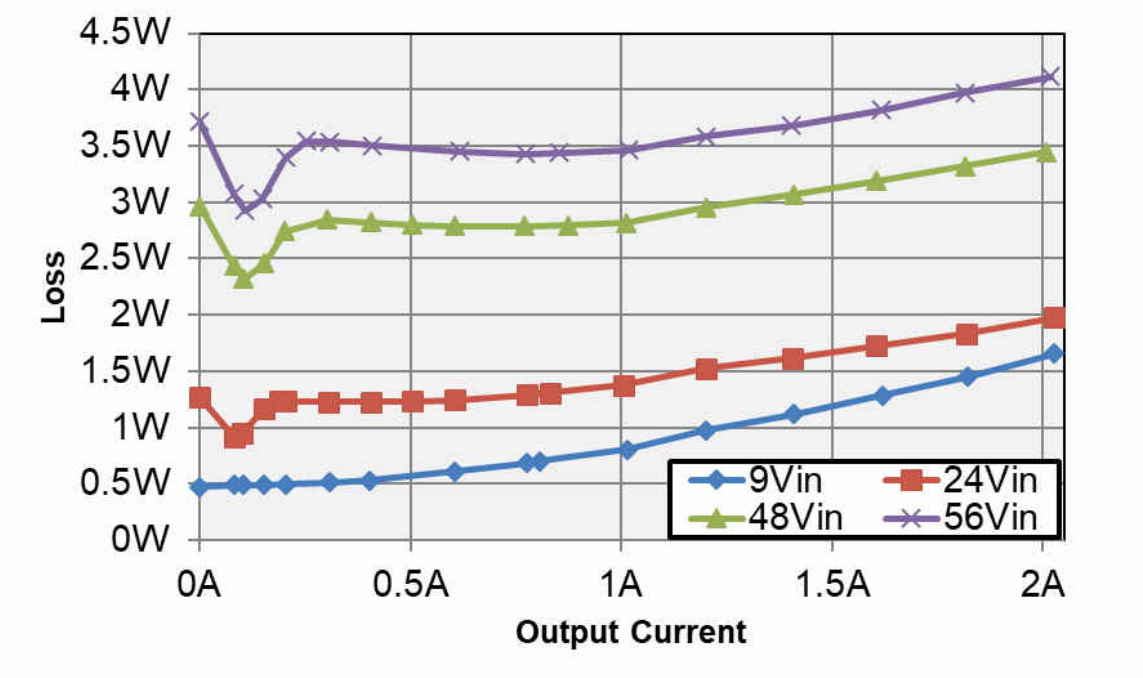


Figure 2-2. Loss vs Output Current

2.3 Load Regulation

The following image shows the PMP30916 load regulation graph.

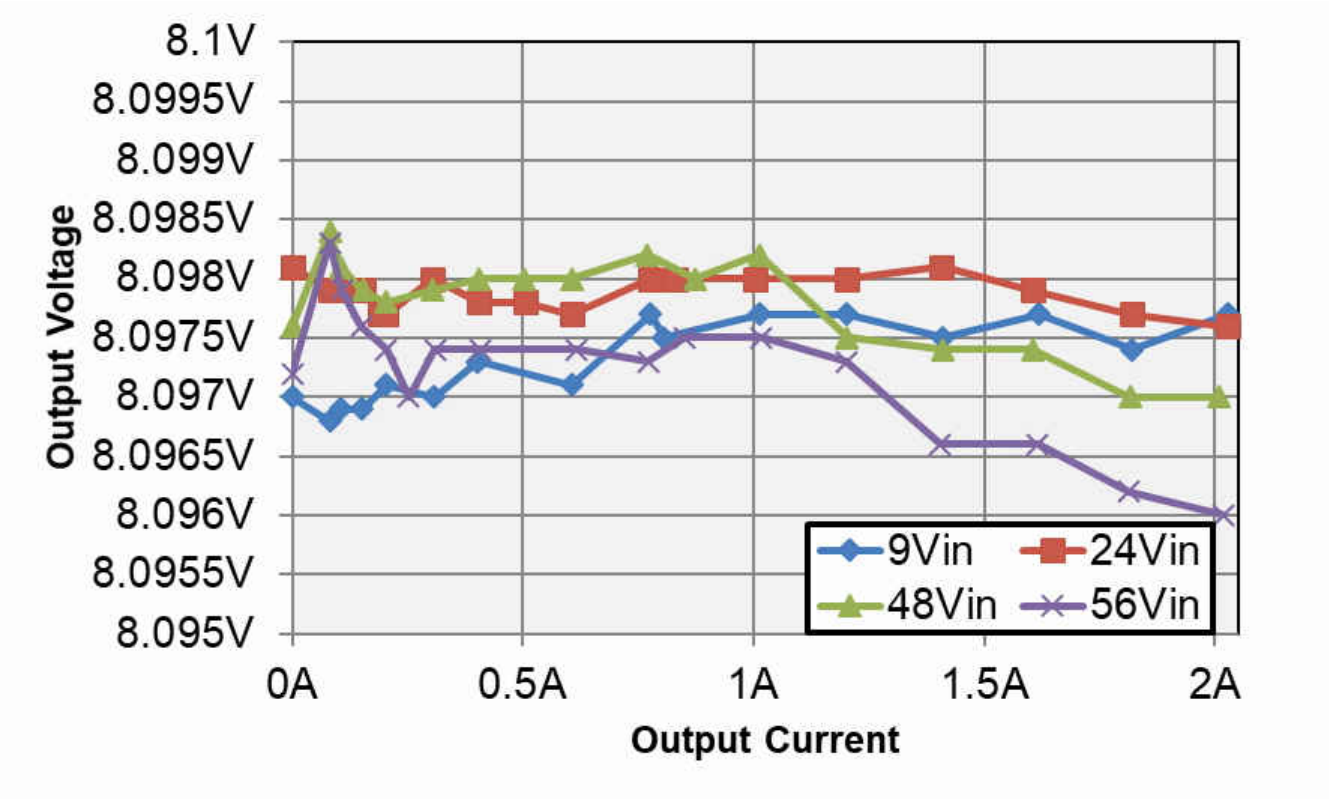


Figure 2-3. Output Voltage vs Output Current

2.4 Line Regulation

The following images show the PMP30916 line regulation graphs.

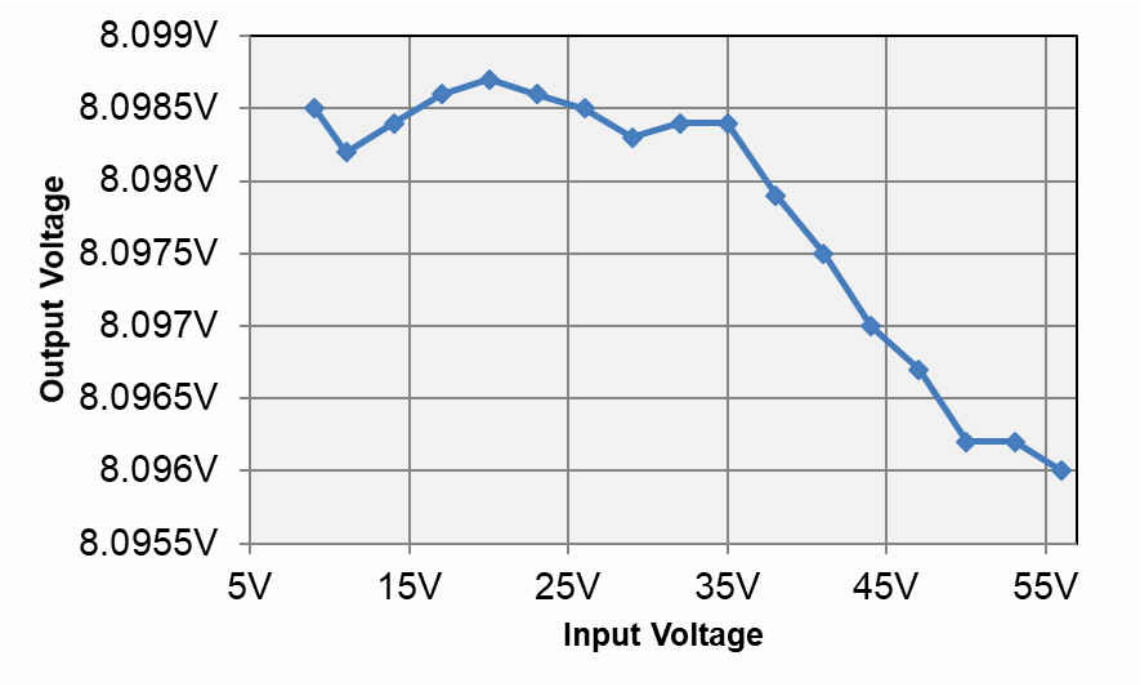


Figure 2-4. Output Voltage vs Input Voltage (2-A Load)

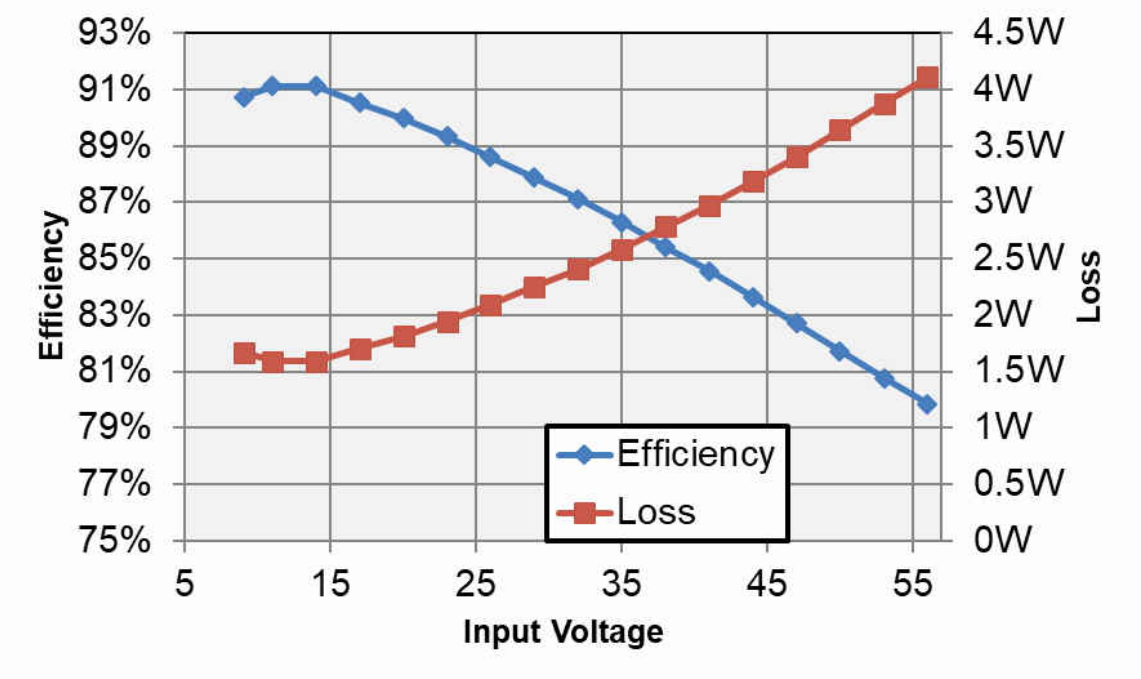


Figure 2-5. Efficiency and Loss vs Input Voltage

2.5 Thermal Images

The PMP30916 thermal images are shown in the following figures.

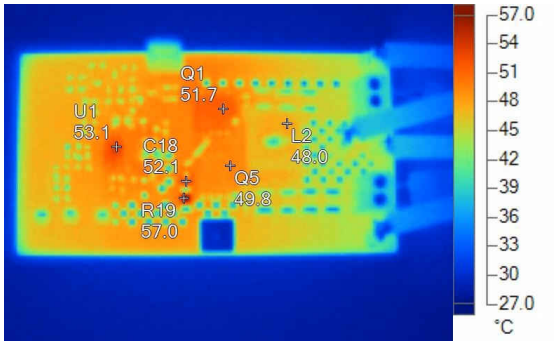
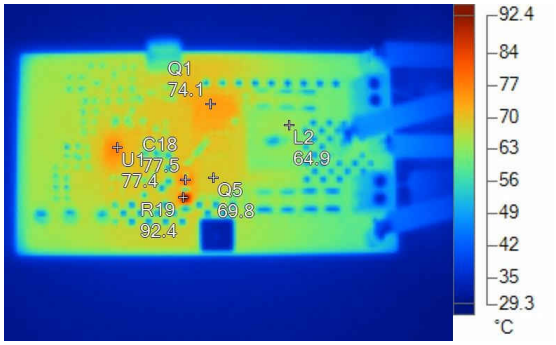
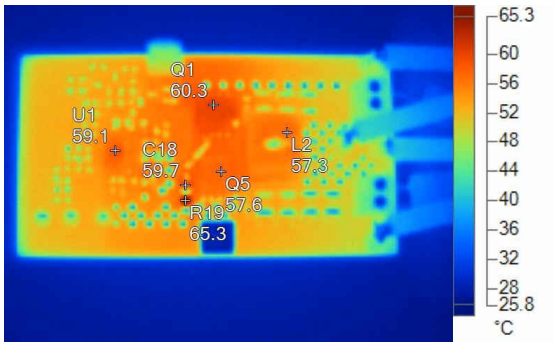
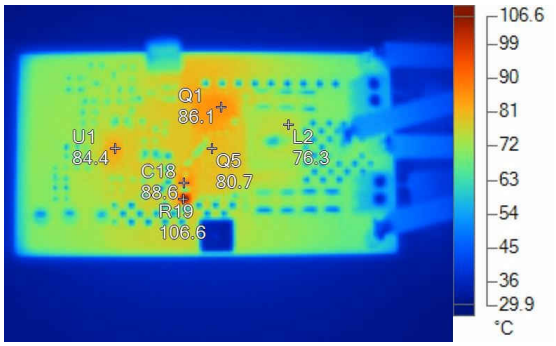
	24-V Input	48-V Input
1 A_{OUT}		
2 A_{OUT}		

Figure 2-6. Thermal Images

Name	24 V_{IN}, 1 A_{OUT}	24 V_{IN}, 2 A_{OUT}	48 V_{IN}, 1 A_{OUT}	48 V_{IN}, 2 A_{OUT}
C18	52.1°C	59.7°C	77.5°C	88.6°C
L2	48.0°C	57.3°C	64.9°C	76.3°C
Q1	51.7°C	60.3°C	74.1°C	86.1°C
Q5	49.8°C	57.6°C	69.8°C	80.7°C
R19	57.0°C	65.3°C	92.4°C	106.6°C
U1	53.1°C	59.1°C	77.4°C	84.4°C

2.6 Bode Plots

Table 2-1 shows the summary of the PMP30916 bode plots.

Table 2-1. Bode Plot Summary

	9 V_{IN}	24 V_{IN}	48 V_{IN}	56 V_{IN}
Bandwidth (kHz)	5.7	9.56	10.3	10.1
Phase Margin	66°	43.7°	52.4°	55.5°
Slope (20 dB/ decade)	–2	–2	–2	–1.98
Gain Margin (dB)	–15.3	–18.1	–20.3	20.9
Slope (20 dB/ decade)	–1.3	–2	–2	–2.2
Freq. (kHz)	18.8	33.8	43.3	45.3

2.6.1 9-V Input Voltage

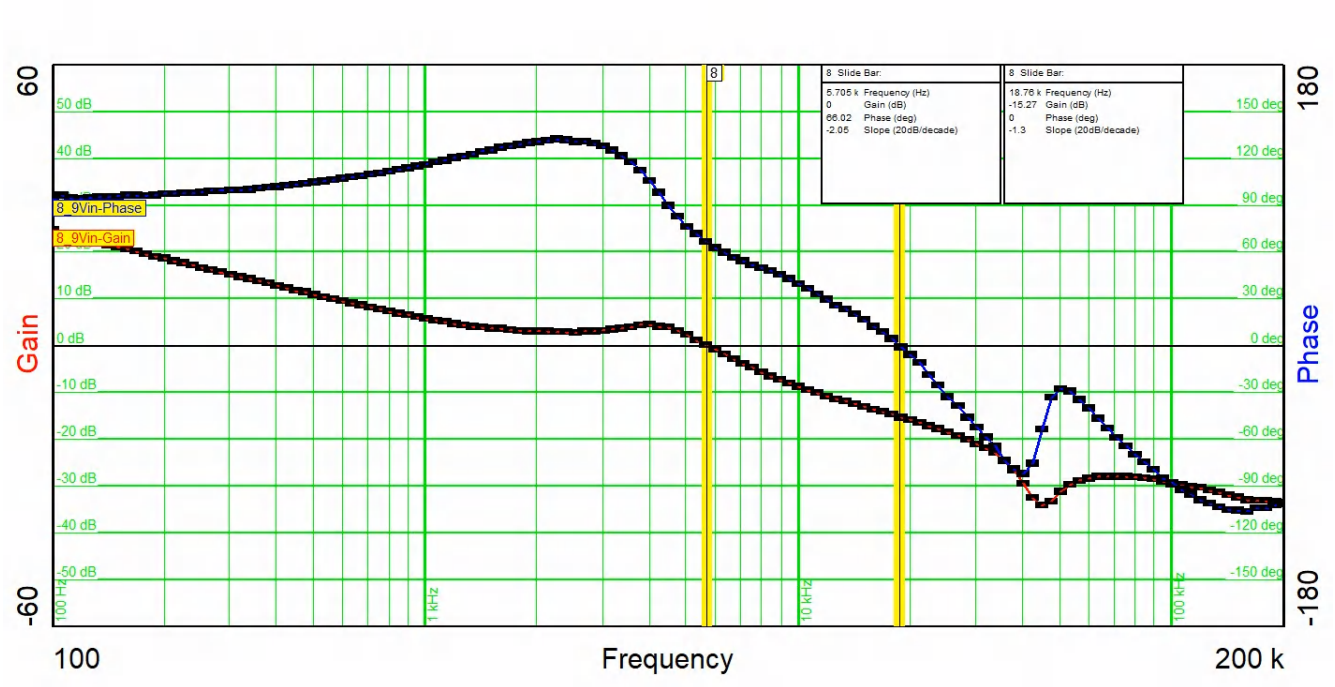


Figure 2-7. Bode Plot for 9-V Input Voltage

2.6.2 24-V Input Voltage

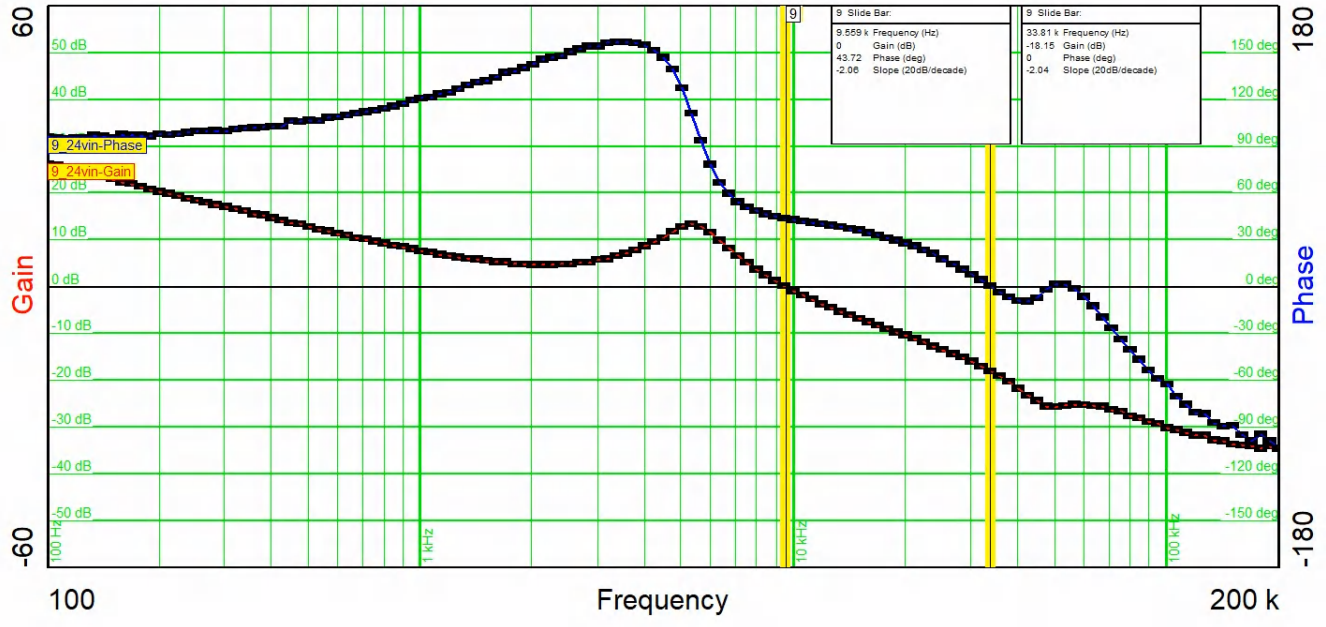


Figure 2-8. Bode Plot for 24-V Input Voltage

2.6.3 48-V Input Voltage

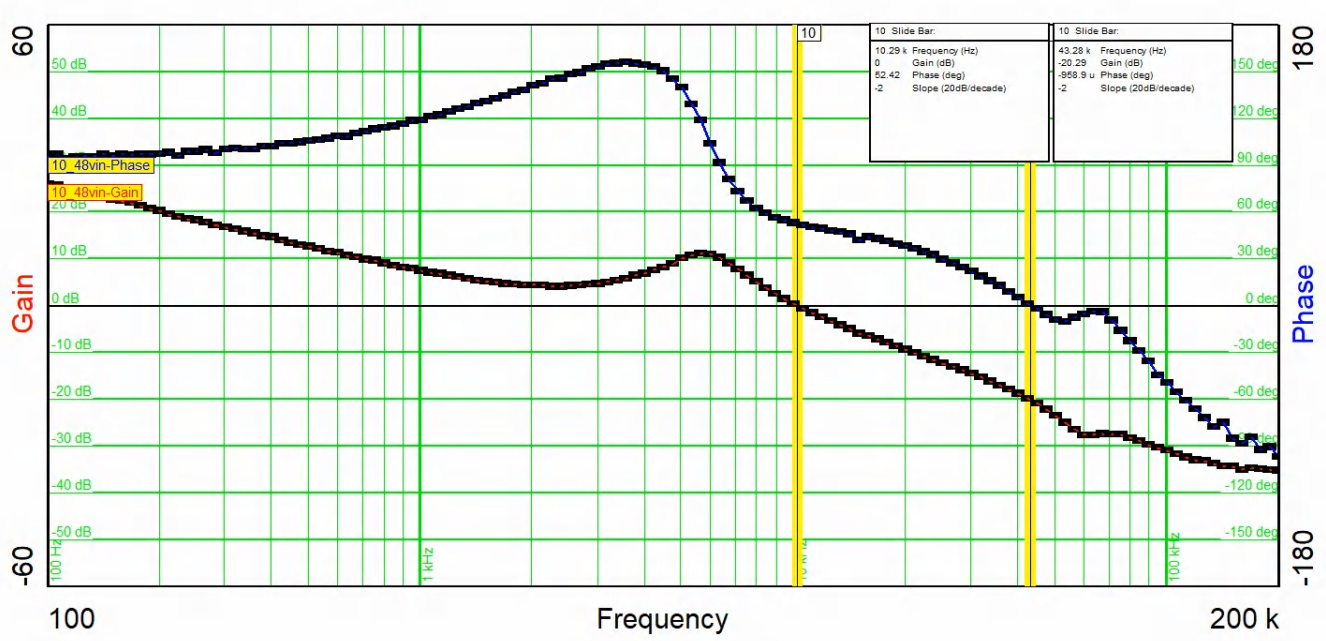


Figure 2-9. Bode Plot for 48-V Input Voltage

2.6.4 56-V Input Voltage

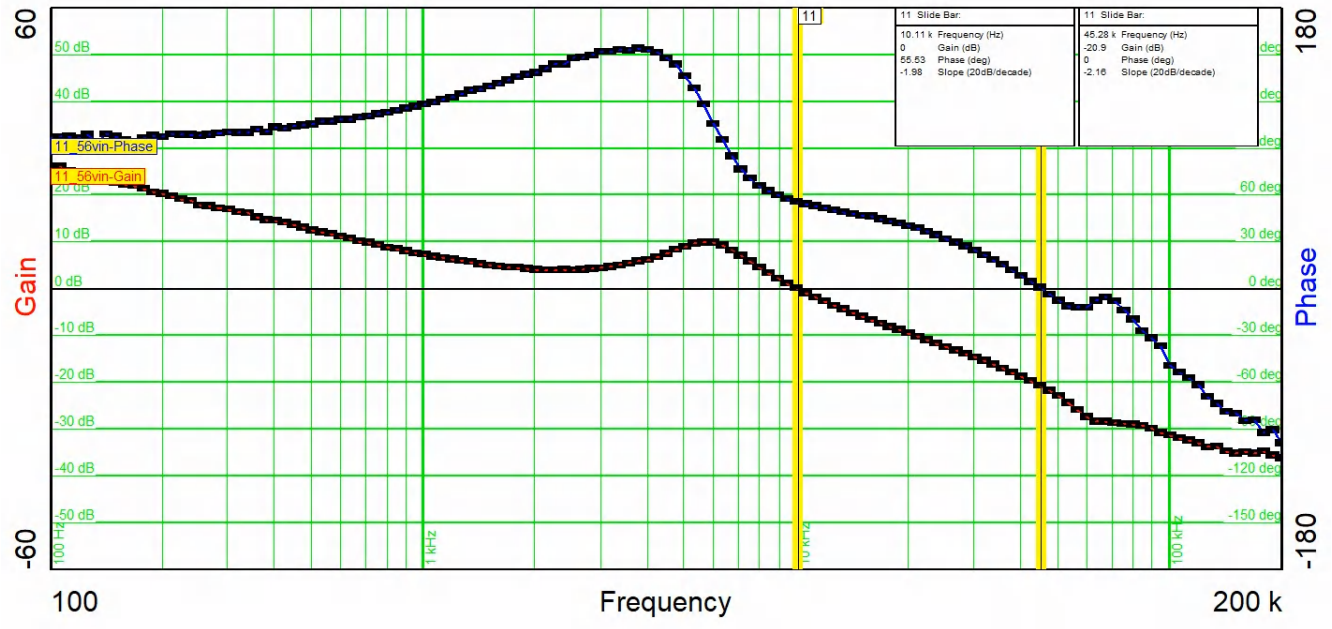


Figure 2-10. Bode Plot for 56-V Input Voltage

3 Waveforms

3.1 Switching

3.1.1 Transistor Q5 (Low-Side FET)

3.1.1.1 Drain - Source

3.1.1.1.1 9-V Input Voltage

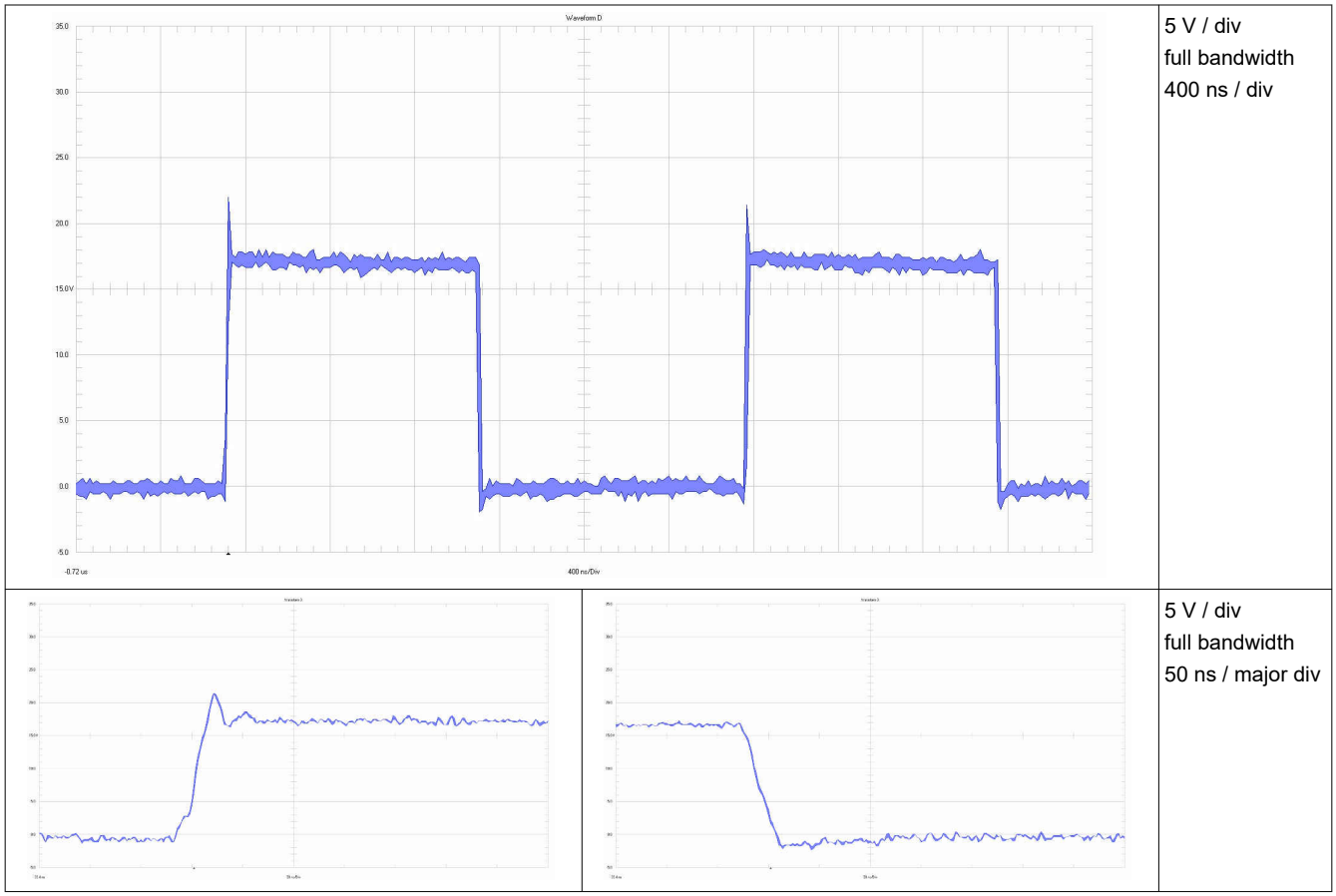


Figure 3-1. Q5 Drain-Source at 9 V_{IN}

3.1.1.1.2 56-V Input Voltage

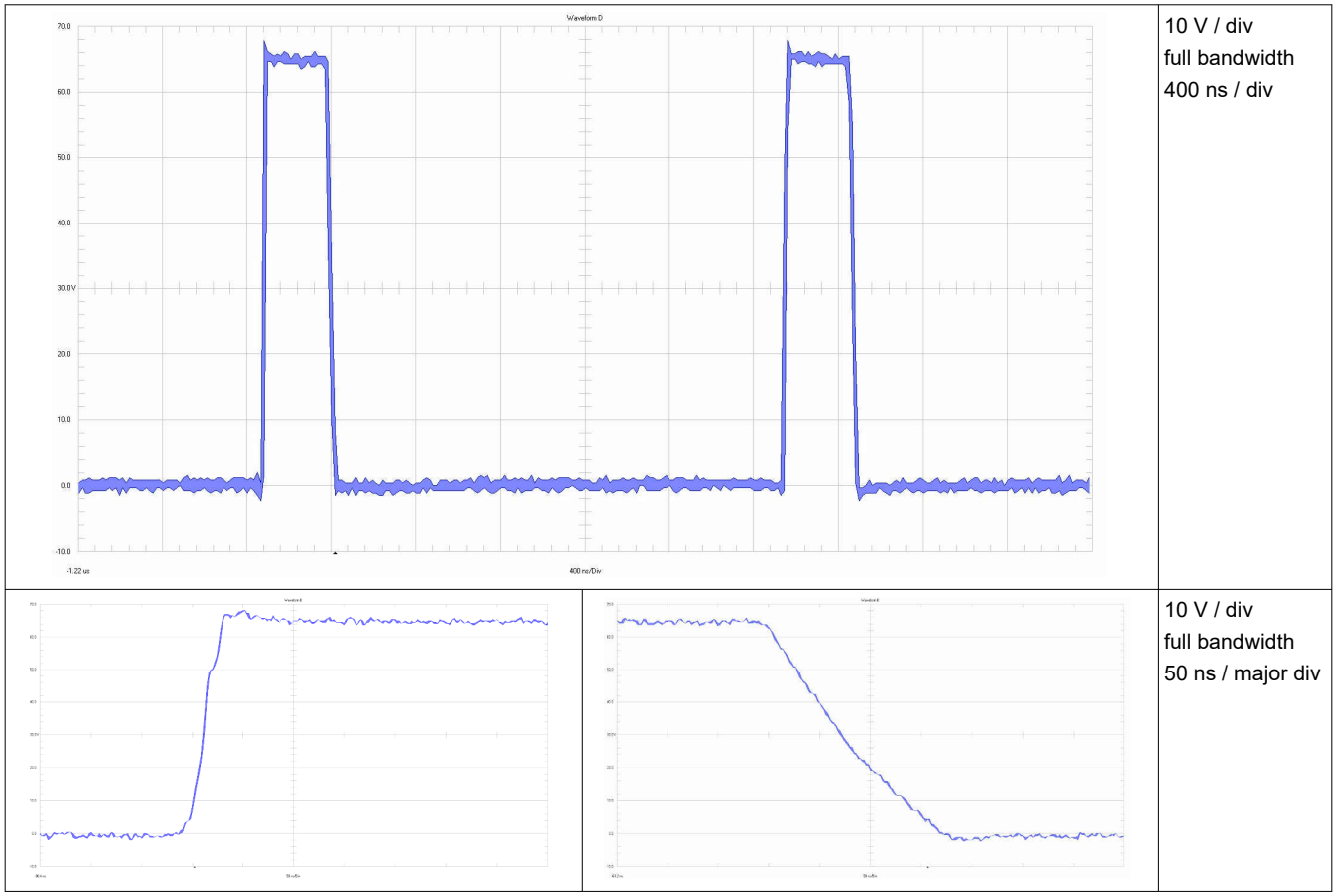


Figure 3-2. Q5 Drain-Source at 56 V_{IN}

3.1.1.2 Gate - Source

3.1.1.2.1 9-V Input Voltage

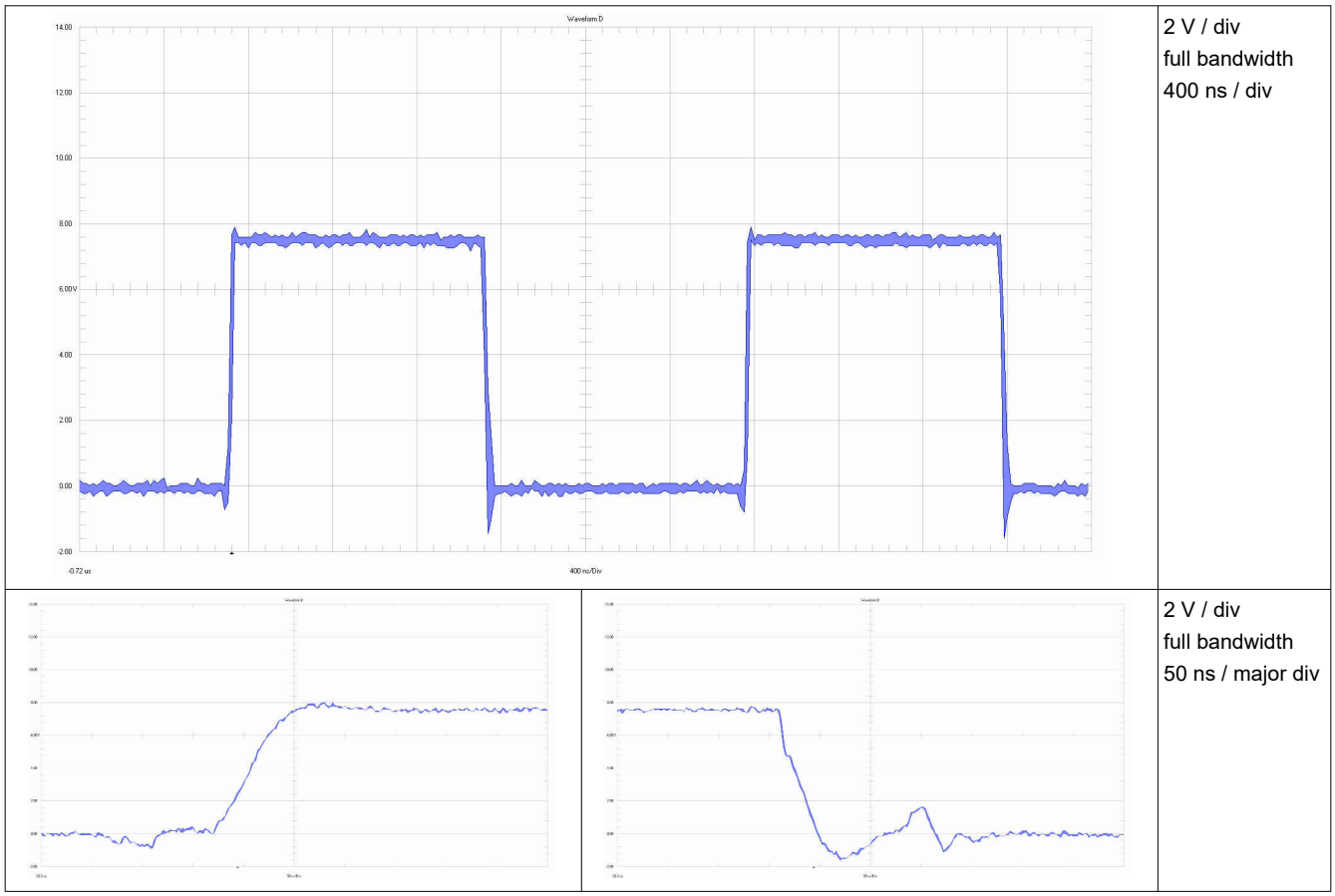


Figure 3-3. Q5 Gate-Source at 9 V_{IN}

3.1.1.2.2 56-V Input Voltage

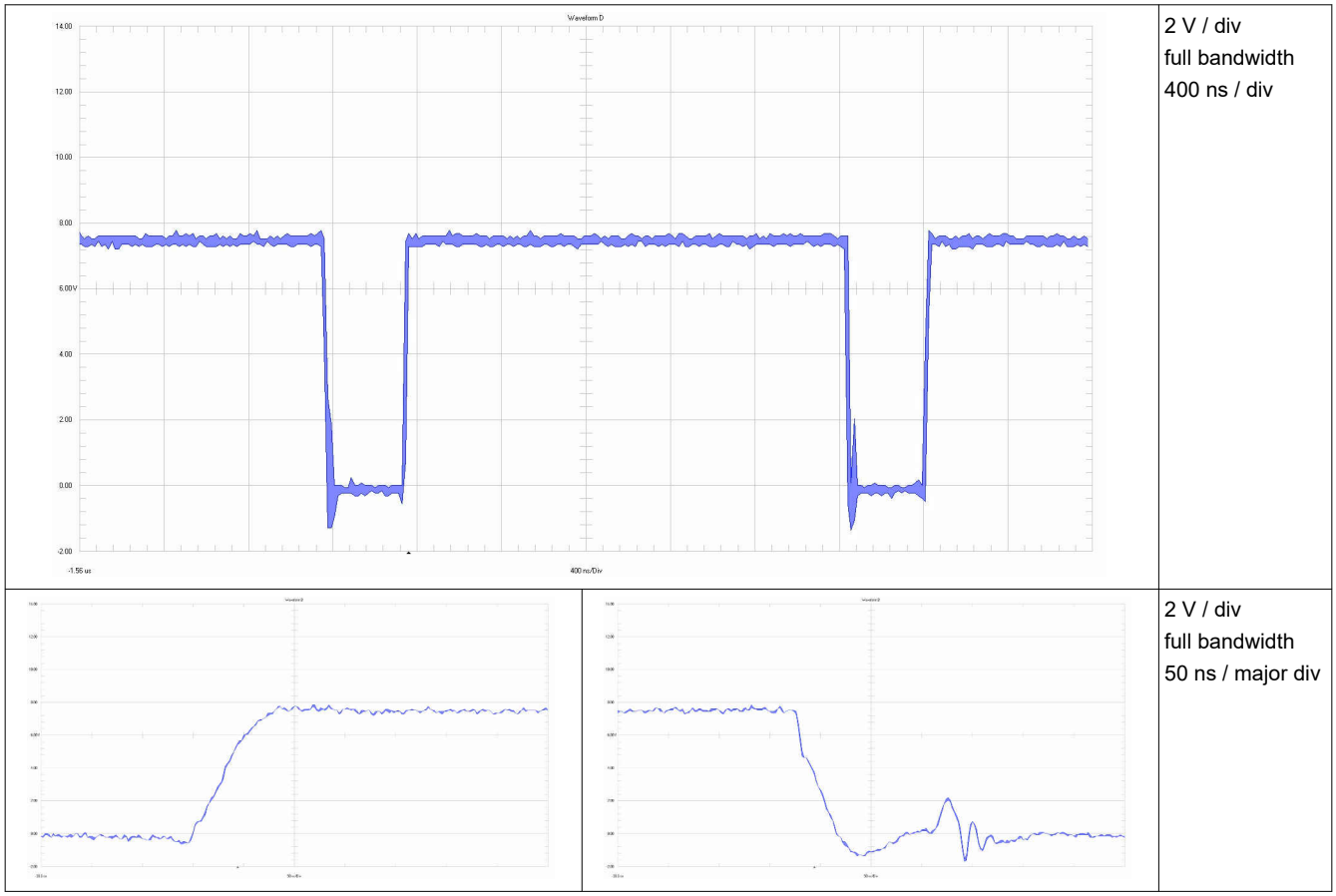
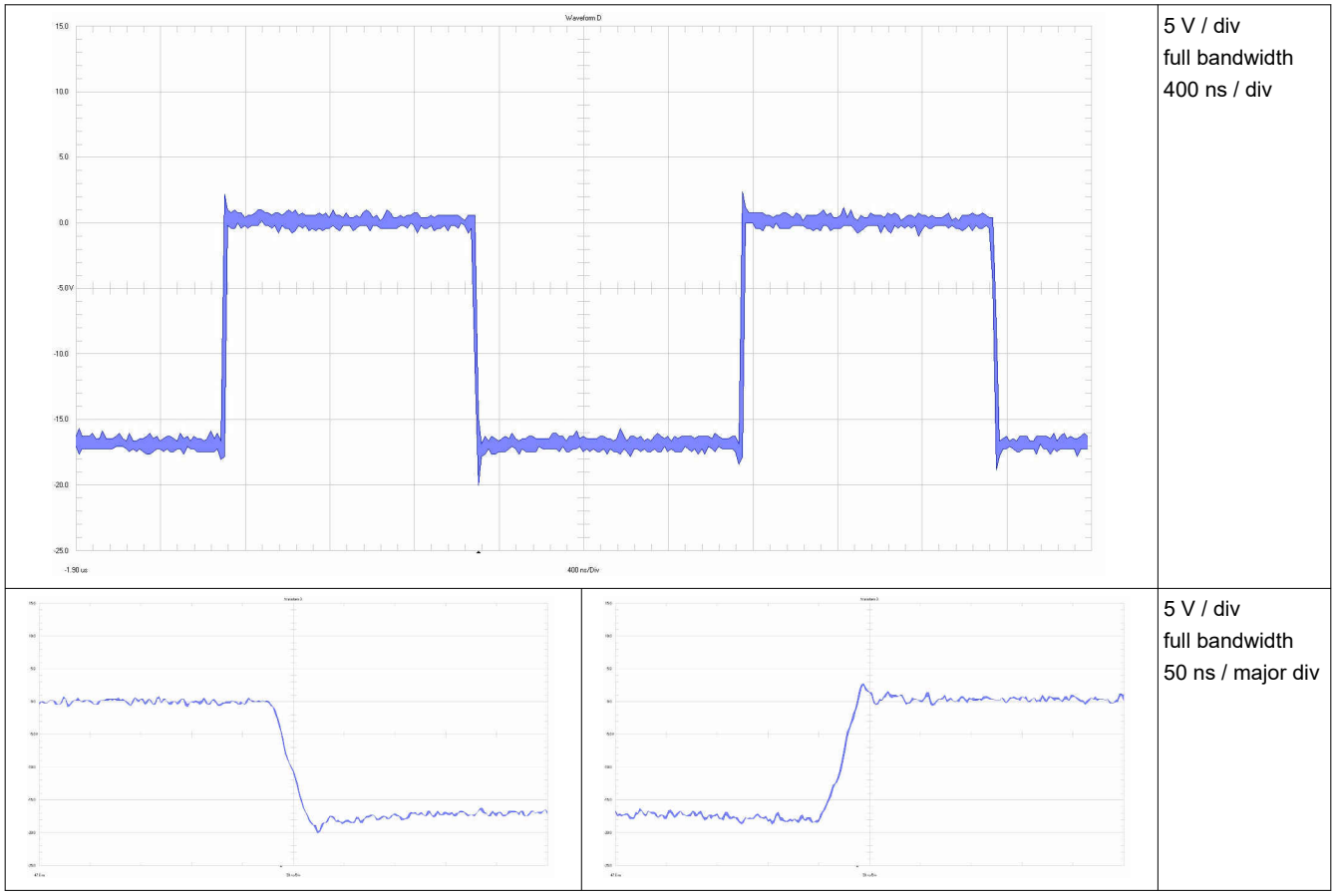


Figure 3-4. Q5 Gate-Source at 56 V_{IN}

3.1.2 Transistor Q1 (High-Side FET)

3.1.2.1 Source - Drain (Referenced to V_{IN})

3.1.2.1.1 9-V Input Voltage



	5 V / div full bandwidth 400 ns / div
	5 V / div full bandwidth 50 ns / major div

Figure 3-5. Q1 Source-Drain at 9 V_{IN}

3.1.2.1.2 56-V Input Voltage

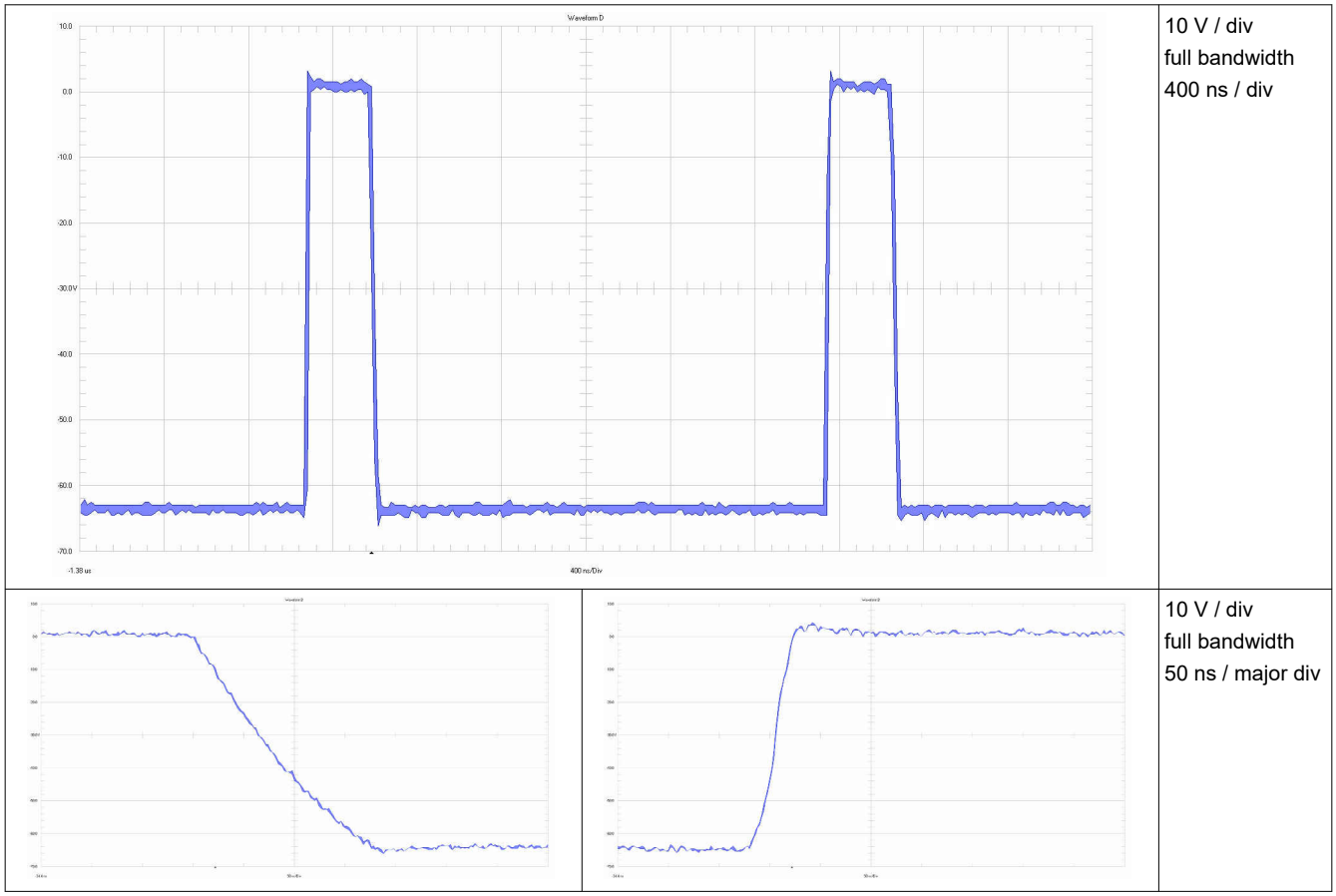


Figure 3-6. Q1 Source-Drain at 56 V_{IN}

3.1.2.2 Gate - Source

3.1.2.2.1 9-V Input Voltage

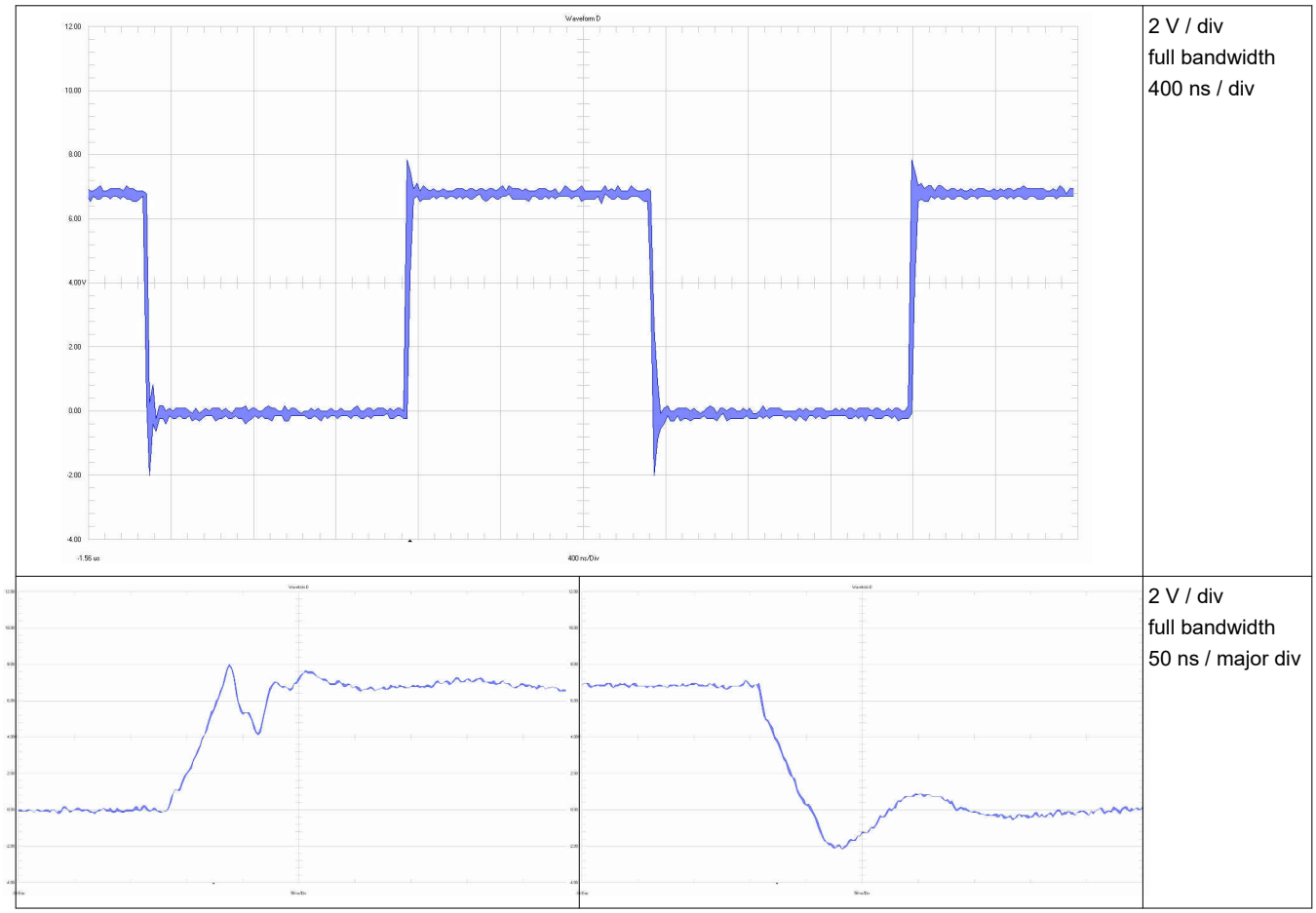


Figure 3-7. Q1 Gate-Source at 9 V_{IN}

3.1.2.2.2 56-V Input Voltage

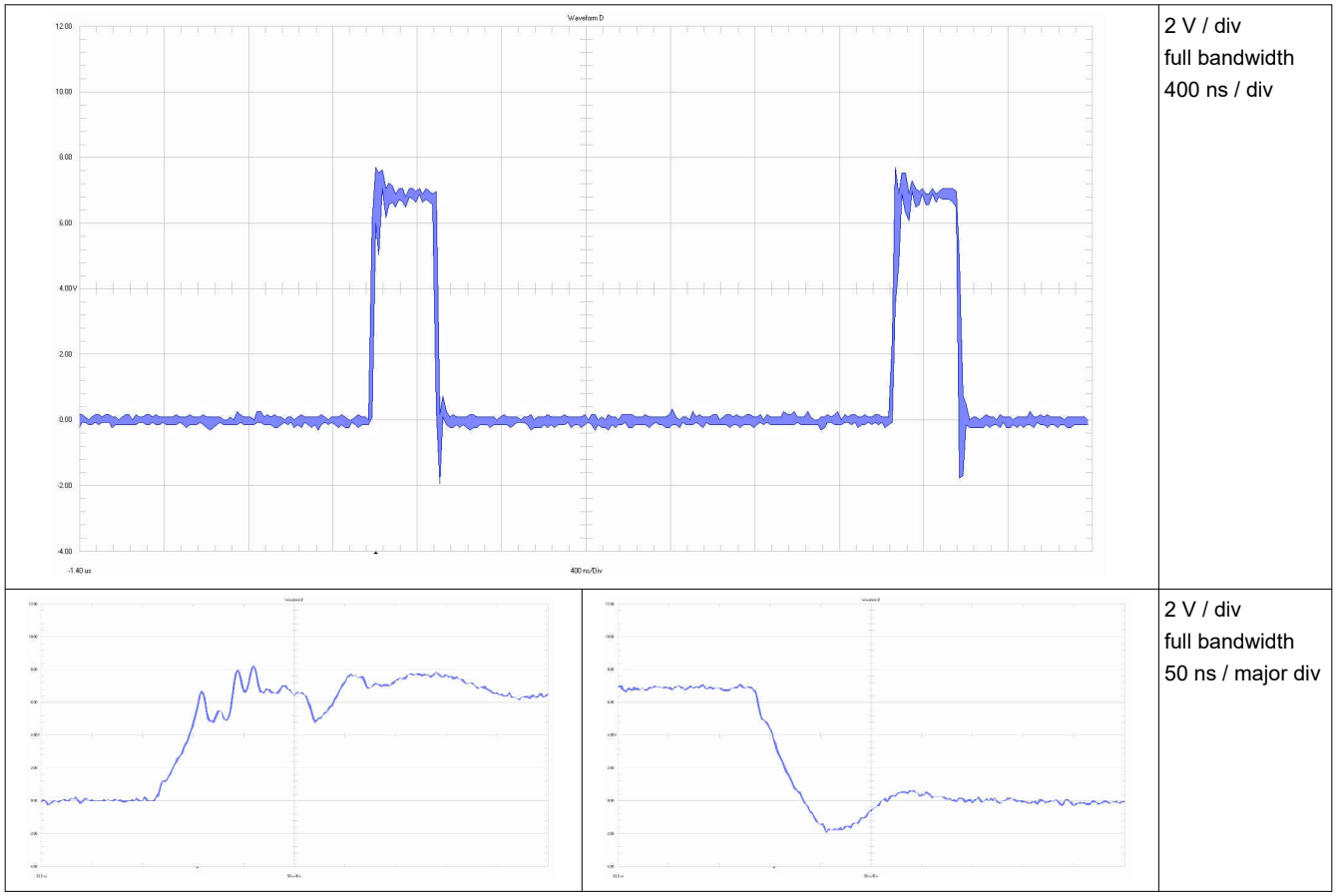


Figure 3-8. Q1 Gate-Source at 56 V_{IN}

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figure.

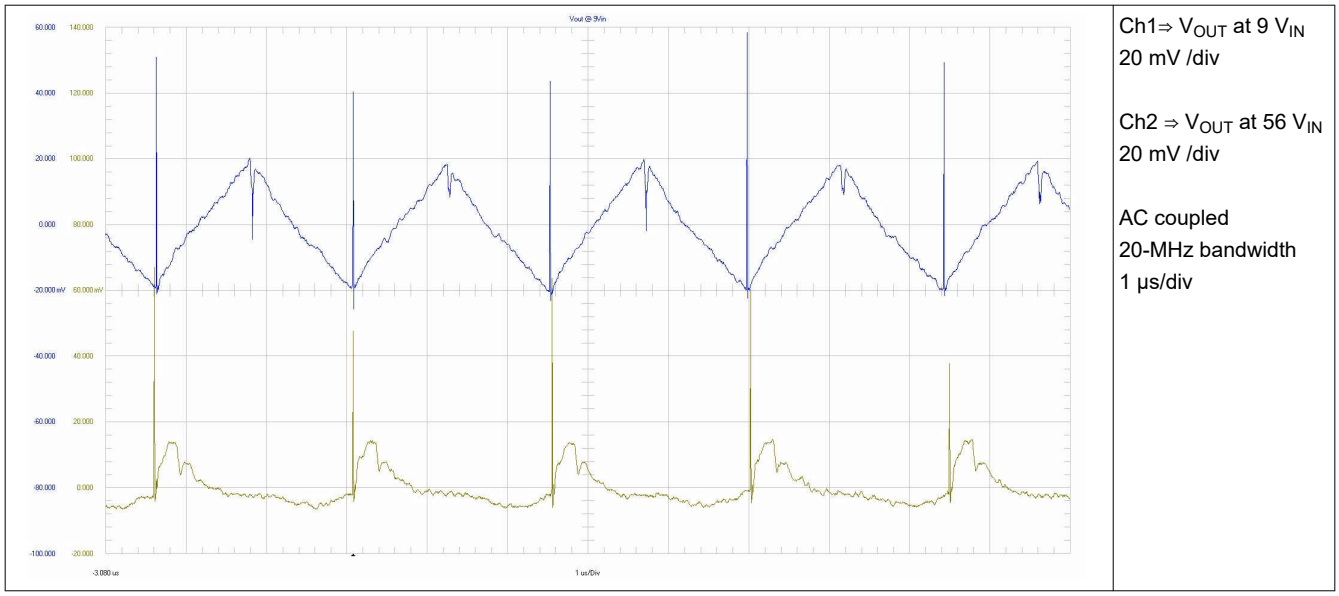


Figure 3-9. Output Voltage Ripple

3.3 Input Voltage Ripple

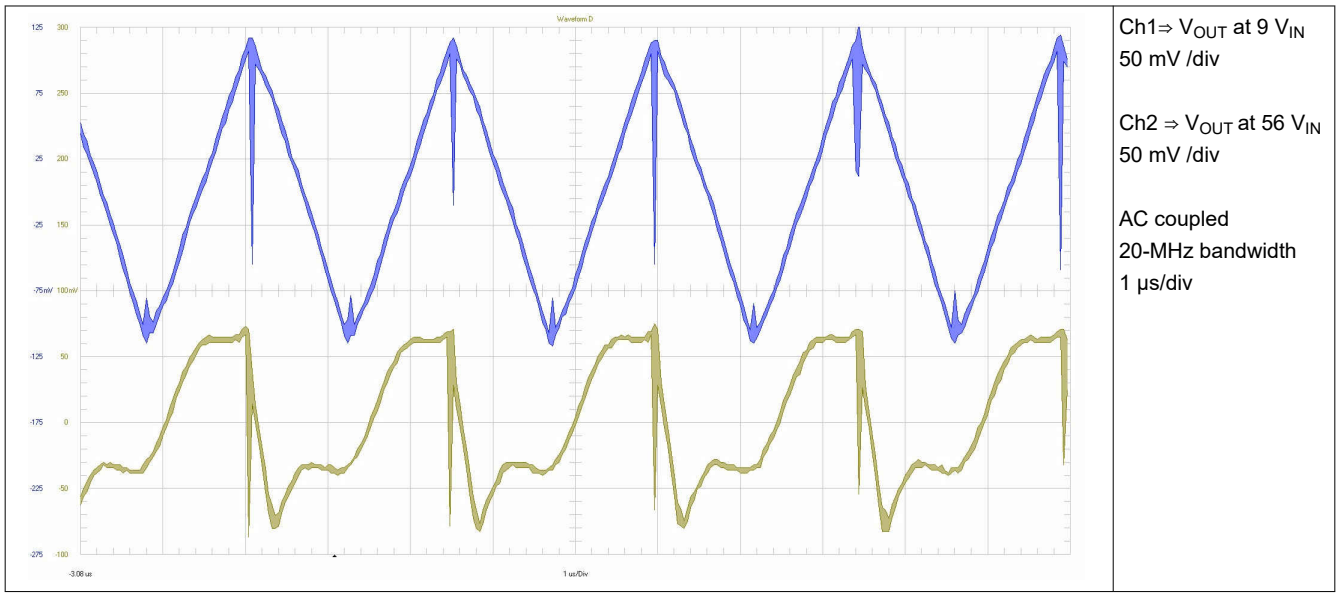


Figure 3-10. Input Voltage Ripple

3.4 Load Transients

Load transient response is shown in the following figures.

3.4.1 9-V Input Voltage

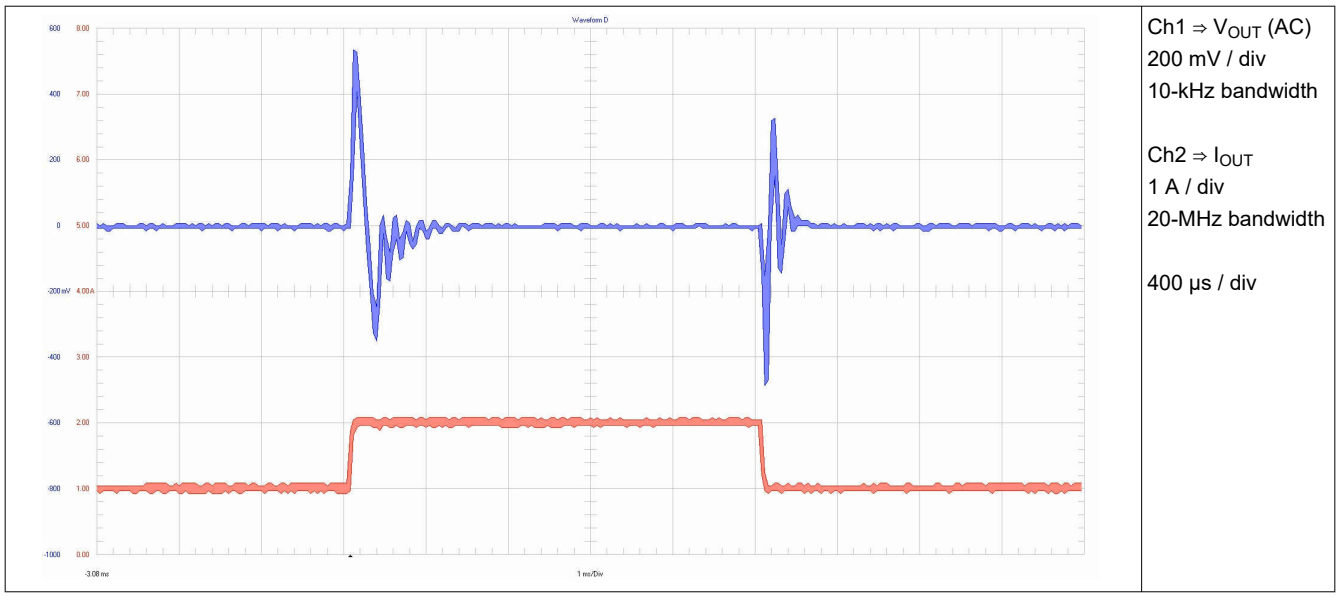


Figure 3-11. Load Transient 1 A to 2 A at 9-V Input Voltage

3.4.2 56-V Input Voltage

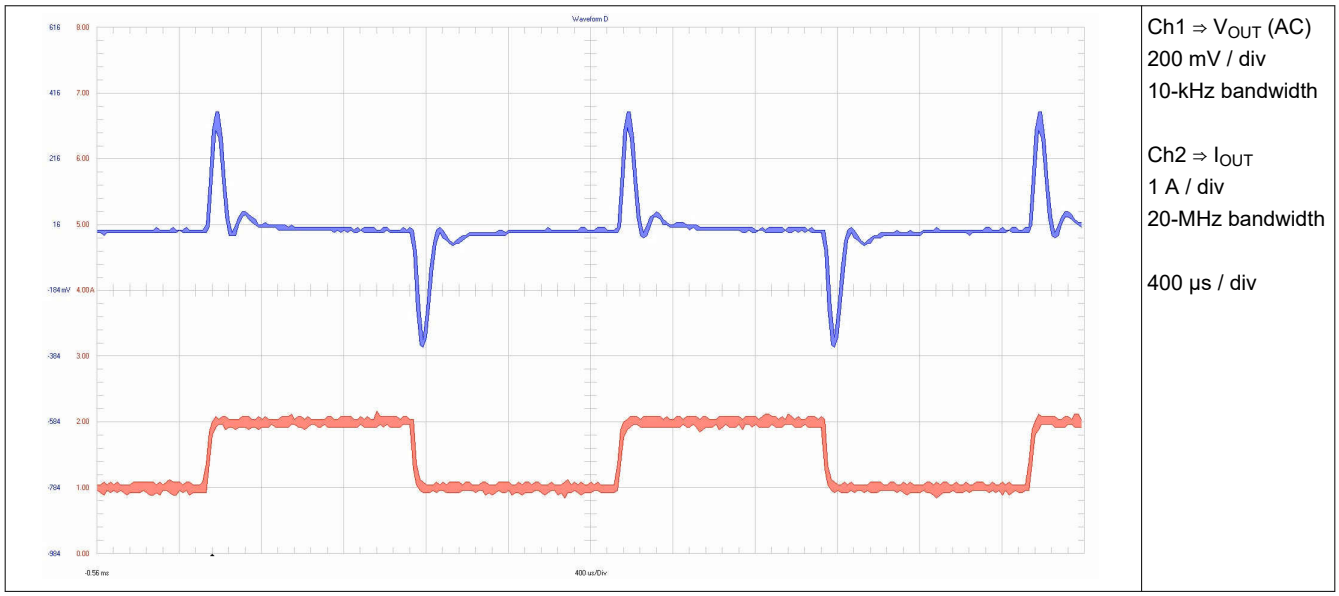


Figure 3-12. Load Transient 1 A to 2 A at 56-V Input Voltage

3.5 Start-Up Sequence

Start-up behavior is shown in the following figures.

3.5.1 9-V Input Voltage

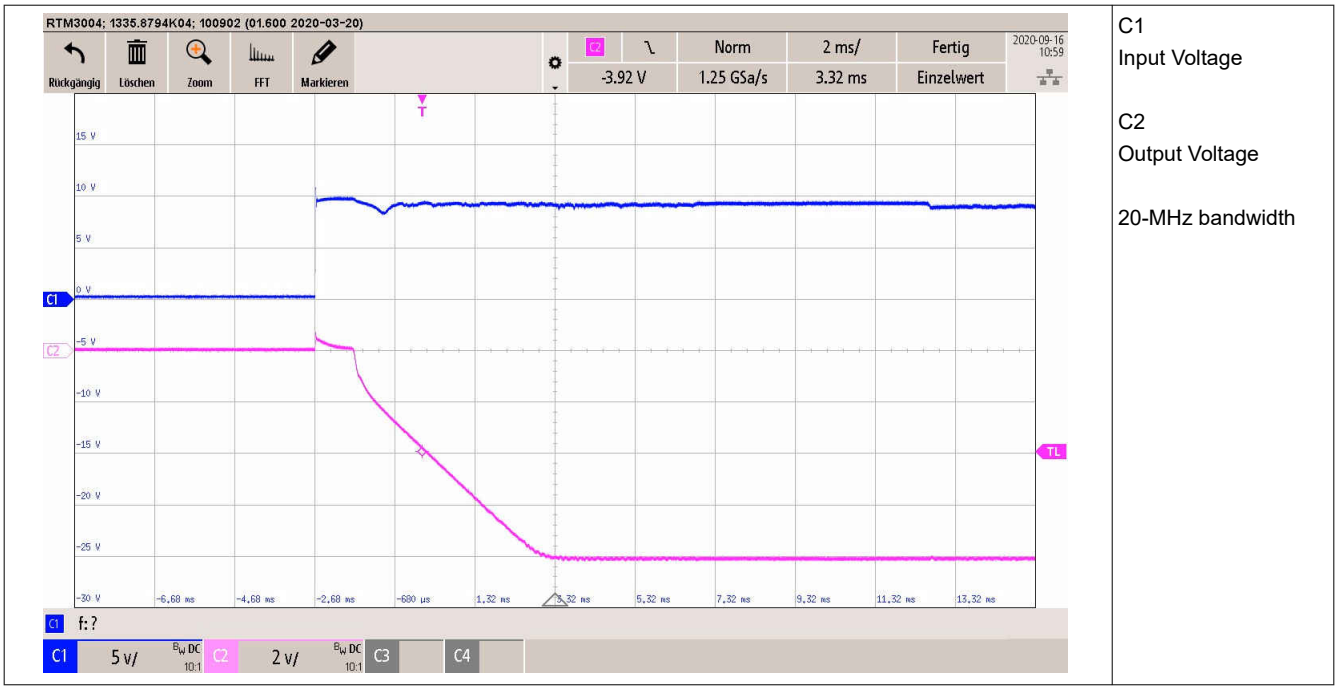


Figure 3-13. Start-Up at 9-V Input Voltage

3.5.2 56-V Input Voltage

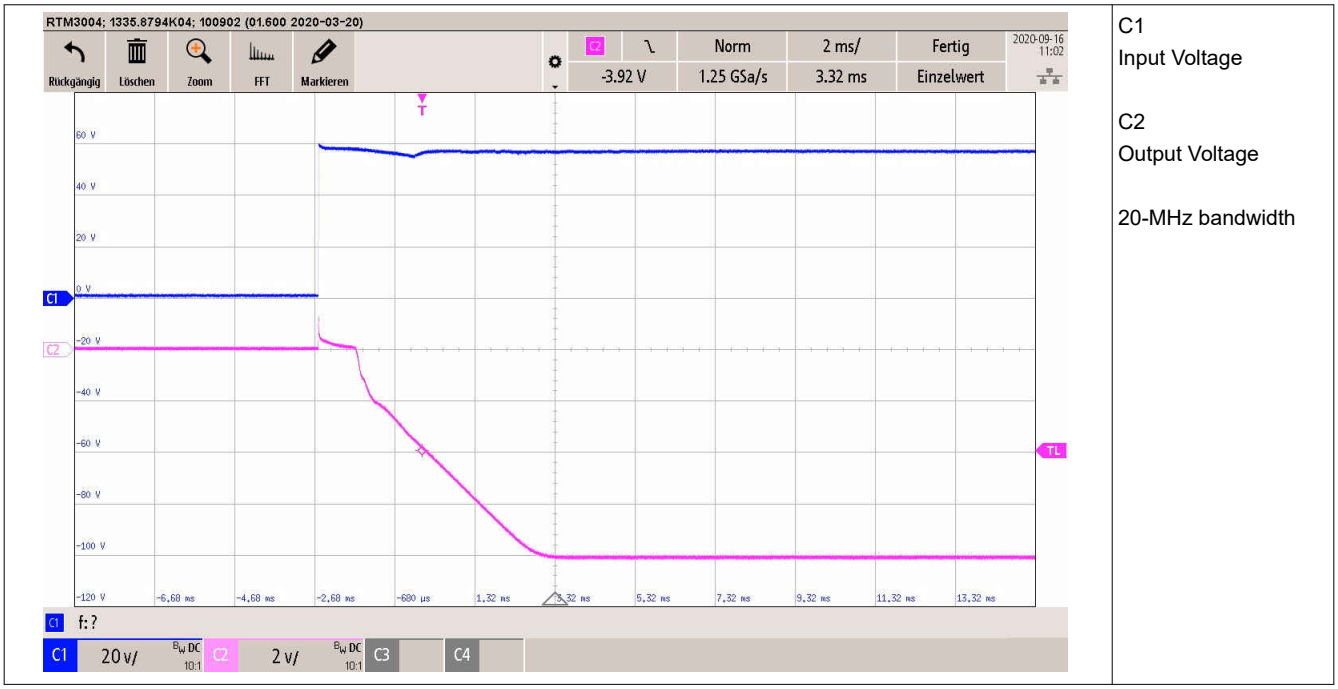


Figure 3-14. Start-Up at 56-V Input Voltage

3.6 Shutdown Sequence

3.6.1 9-V Input Voltage

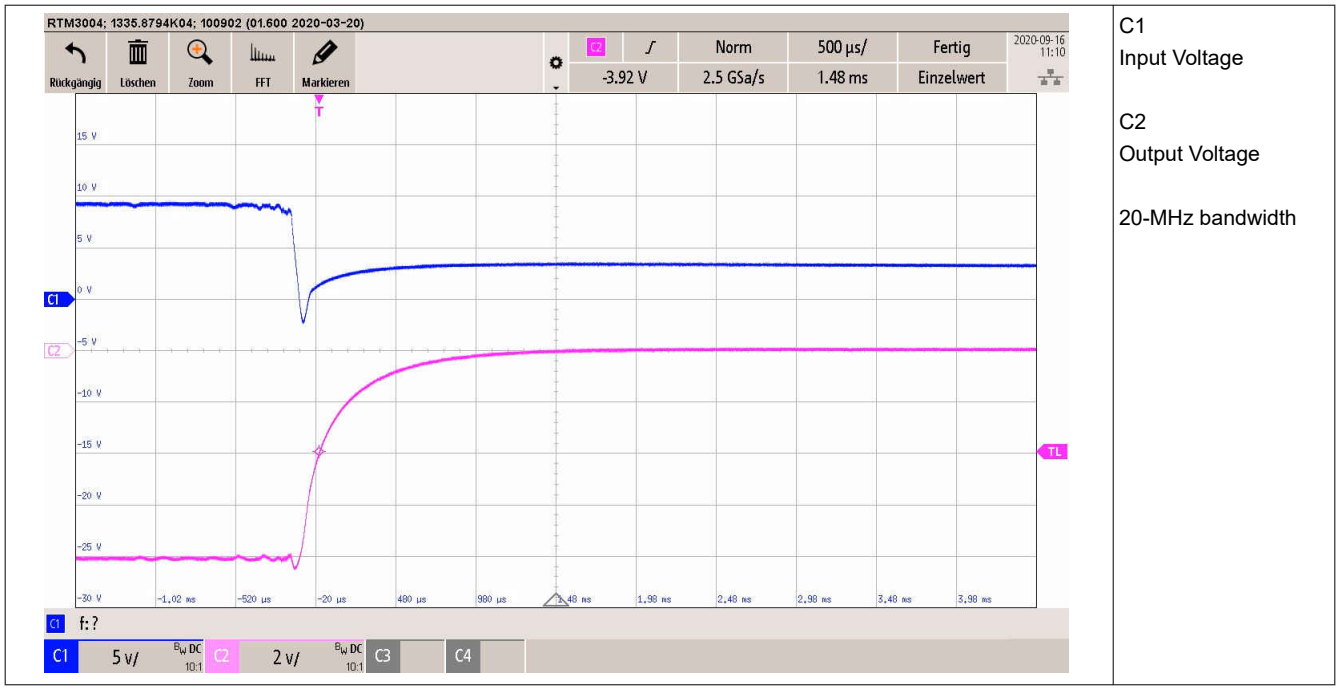


Figure 3-15. Shutdown at 9-V Input Voltage

3.6.2 56-V Input Voltage

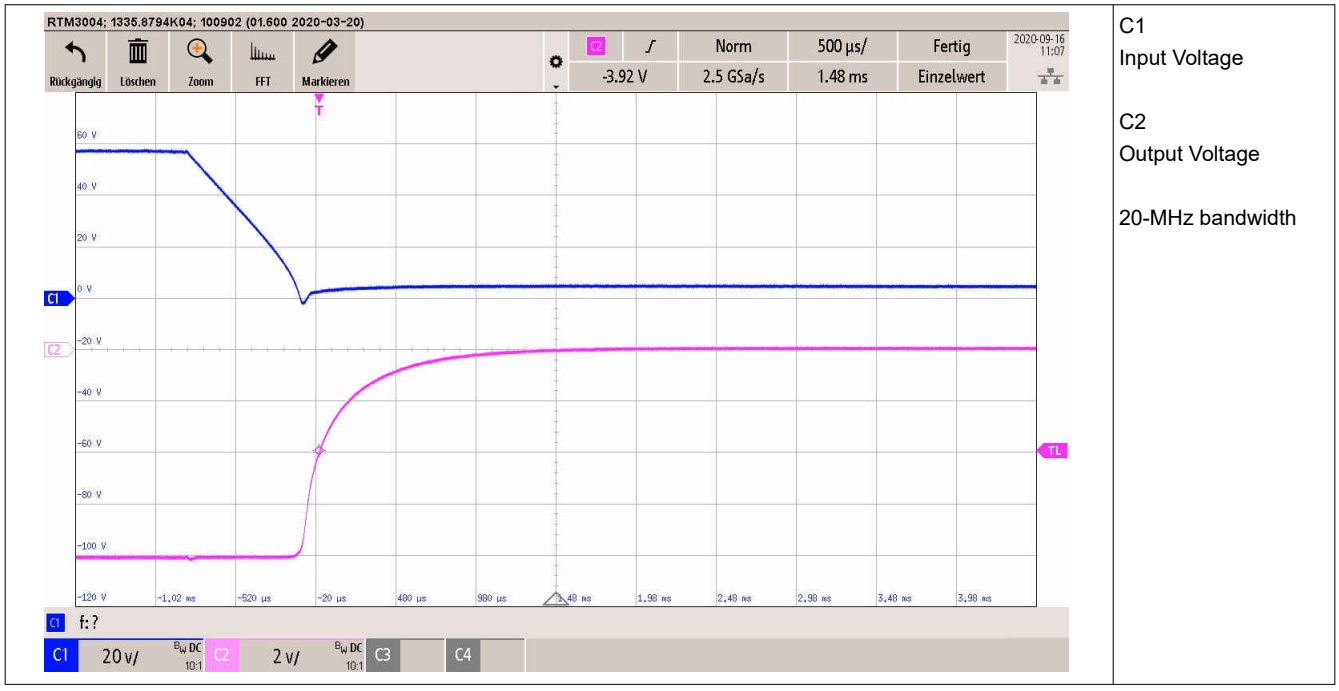


Figure 3-16. Shutdown at 56-V Input Voltage

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265