TI Designs

Bipolar TFT LCD Supply Using TPS65131-Q1 and Charge Pumps

Abstract

This reference design provides an easy solution for display applications requiring bipolar supply voltages $\pm AV_{DD}$ for the source driver and additional supply voltages V_{GH} and V_{GL} for the gate drivers.

The $\pm AV_{DD}$ part of this reference design uses a standard application circuit and is covered by the TPS65131-Q1 device, so this document focuses on the charge pump circuitry added to generate V_{GH} and V_{GL}.

The following guide describes a circuit that addresses the requirement of four output voltages by using only one converter IC and adding two charge pumps.

The components in this guide are for automotive applications, but the circuit is equally valid for consumer applications that normally use non-Q1 parts.

This reference design also details the design and selection of the components and provides measurement results showing the performance of the circuit.

1 Application Description

The following Figure 1 shows the standard application circuit supplying ±AV_{DD} for the display source drivers, as well as the additional circuitry generating V_{GH} and V_{GL} for the gate drivers. The basic application parameters are:

- Input supply voltage: V_{IN} = 3.3 V ± 10%
- Positive output voltage for source driver (+AV_{DD}): V_{POS} = 6.3 V at 100 mA
- Negative output voltage for source driver (–AV_{DD}): V_{NEG} = –6.3 V at 100 mA
- Positive output voltage for gate driver: V_{GH} = 16 V at 10 mA
- Negative output voltage for gate driver: V_{GL} = –10 V at 10 mA

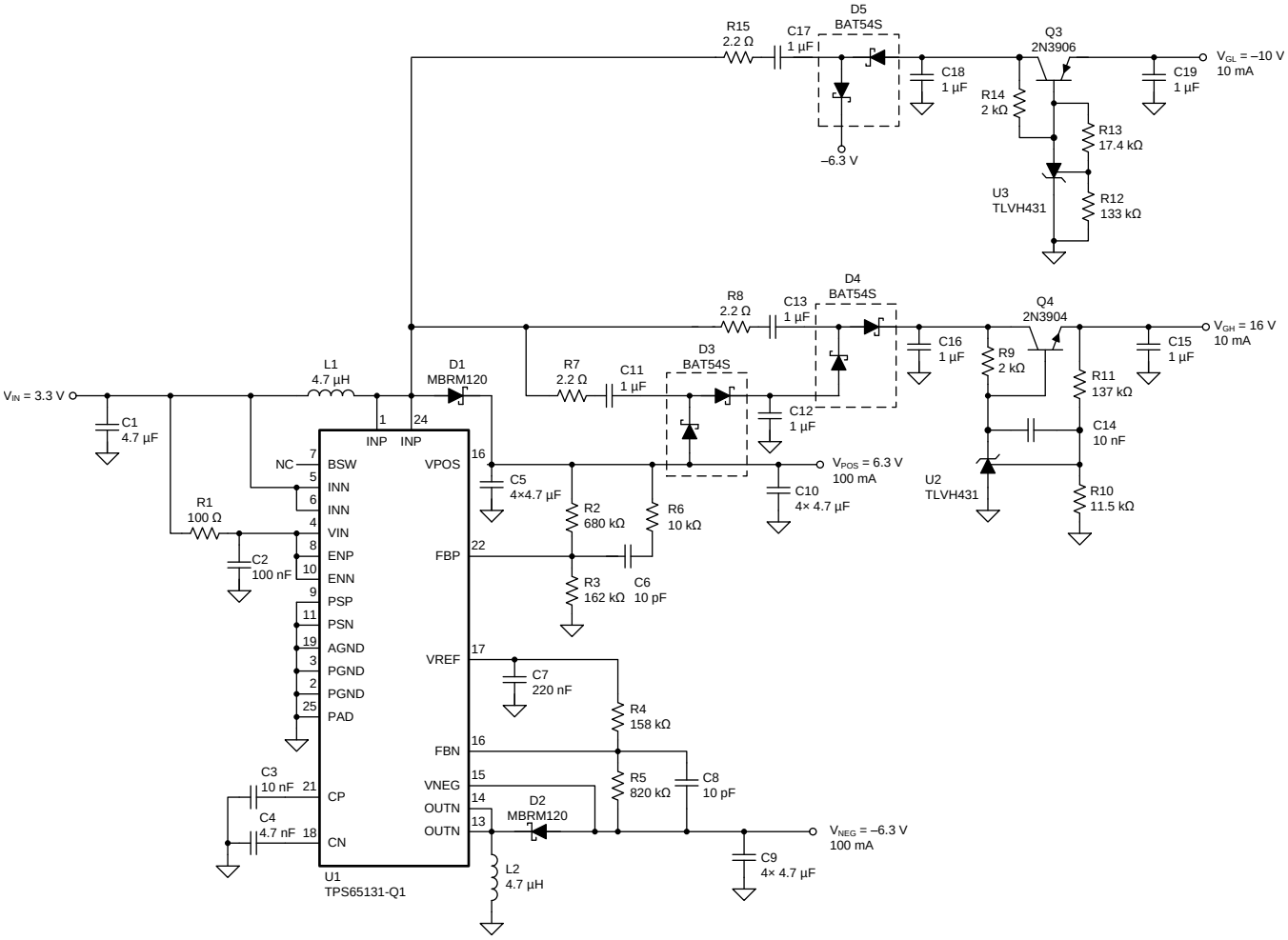

Figure 1. TPS65131-Q1 Circuit Schematic and Charge Pump

2 Circuit Description

Figure 1 is based on the TPS65131-Q1, a highly efficient, dual-output DC-DC converter. One output voltage generates $+AV_{DD}$ (boost converter) and the other generates $–AV_{DD}$ (inverting converter). For further details on the configuration of the TPS65131 device, refer to the TPS65131-Q1 datasheet (SLVSBB2). The main supply AV_{DD} provides a high current (in the range of 100 mA) and is required to be very precise (in the range of 1%), which is fulfilled by the TPS65131-Q1 device.

The main supply $\pm AV_{DD}$ provides a high current and is required to be very precise (in the range of 1%), which is fulfilled by the TPS65131-Q1 device. The additional supply for the gate driver (V_{GH} or V_{GL}) is less demanding, allowing a simpler solution. Because of the lower demands of the gate driver, two charge pumps driven from the switch pin of the boost converter can be used to generate the V_{GH} and V_{GL} rails.

The boost converter includes a small MOSFET that synchronously rectifies the output whenever the inductor current is negative. This rectification ensures that the boost converter always operates in continuous conduction mode (CCM) and that the connected charge pumps are driven continuously. The inverting buck-boost converter does not have a synchronous rectifier and operates in discontinuous conduction mode (DCM) at low output currents and is therefore not suitable to drive the charge pumps.

The power-save mode of the boost converter must be disabled, as in this mode the converter ramps up the output voltage with only one or several operating pulses, which disrupts correct operation of the charge pumps.

2.1 Output Regulation of TPS65131-Q1

2.1.1 Choosing Feedback Resistor

The output voltage V_{POS} is fed back to the TPS65131-Q1 through R2 and R3 and compared to a 1.21-V reference voltage. Calculate V_{POS} using the following Equation 1:

$$V_{POS} = \left(\frac{R2 + R3}{R3}\right) \times 1.21\ V \tag{1}$$

Rearrange the equation to solve for R2 in Equation 2:

$$R2 = \left(\frac{V_{POS}}{1.21} - 1\right) \times R3 \tag{2}$$

With R2 = 680 kΩ and R3 = 162 kΩ, the nominal value of V_{POS} = 6.29 V.

The same behavior applies to the negative output voltage V_{NEG} by following Equation 3.

$$V_{NEG} = -\left(\frac{R5}{R4}\right) \times 1.21\ V \tag{3}$$

Rearrange the equation to solve for R5 in Equation 4:

$$R5 = \left|\frac{V_{NEG}}{1.21}\right| \times R4 \tag{4}$$

With R4 = 158 kΩ and R5 = 820 kΩ , the nominal value of V_{NEG} = –6.28 V. For further detailed information, refer to the TPS65131 datasheet (SLVS493).

2.1.2 Choosing Output Capacitance

The allowed output voltage ripple of the converter defines the total capacitance value. Equation 5 defines the output capacitor for the boost converter and Equation 6 defines the output capacitor for the inverting converter. The following equations are valid assuming the equivalent series resistance (ESR) of the capacitors is negligible.

$$C_{MINp} = \frac{I_{OUTp} \times V_{POS} - V_{IN}}{fs\Delta V_p\,(V_{POS} \times V_{IN})} \tag{5}$$

$$C_{MIN_N} = \frac{I_{OUT_N} \times V_{NEG}}{fs\Delta V_N \times (V_{NEG} - V_{IN})} \tag{6}$$

With a chosen ripple voltage in the range of 10 mV, a minimum capacitance of 8 µF is required. Due to the high DC bias of ceramic capacitors, either the capacitor voltage rating or the capacitor value must be increased to meet the minimum capacitance requirements. TI recommends using 4 x 4.7 µF on both outputs. For further detailed information, refer to the TPS65131 datasheet (SLVS493).

2.2 Positive Charge Pump Description

The switch node of the boost converter generates a pulse with an amplitude of the output voltage minus the voltage drop of the rectifier diode ($V_{F(D)}$), using this node to drive the charge pump doubles the output voltage. Figure 2 shows the operation of a charge pump configured as a voltage doubler.

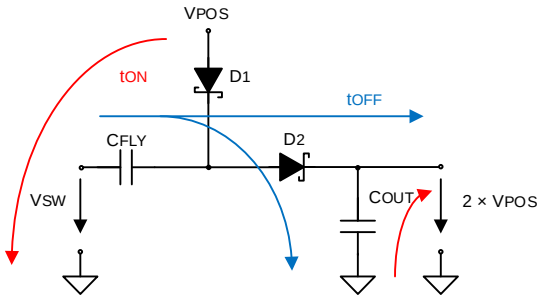

Figure 2. Positive Charge Pump Doubler

During the device on-time t_{ON} with V_{SW} = 0 V, the flying capacitor C_{FLY} charges to V_{POS} - $V_{F(D1)}$ through the D1 diode. During the off-time t_{OFF} with $V_{SW} = V_{POS} + V_{F(D)}$, the pre-charged C_{FLY} is lifted up with $V_{POS} + V_{F(D)} – V_{F(D2)}$, causing a capacitor charge of:

$$V_{C_{FLY}} = 2V_{POS} + V_{F(D)} - V_{F(D1)} - V_{F(D2)} \quad (7)$$

The charge pump structure allows n-times multiplication of the supply voltage by adding n-1 stages. With the given requirements, two stages are realized as the output voltage of the charge pumps is three times the output voltage of the boost converter.

In the inverting charge pump, the flying capacitor works the same as the positive, except the diodes are upside down and referring to GND, not to V_{POS}. When choosing the right components for the charge pump the requirements are the same as for the inverting charge pump.

2.3 Choosing Flying Capacitor

The flying capacitor delivers the energy to the load. The dimensions for the flying capacitor must not be too large, as the size increases. The flying capacitor must not be too small, either, as a smaller capacitance means higher peak currents. The typical range for the flying capacitor is between 100 nF and 1 µF.

To reduce the current spikes, a resistor is placed before the flying capacitor. Although a higher resistance limits the current sufficiently, the losses are too high, as it causes a voltage drop on the output. The typical range for the resistor value is between 2 Ω and 8 Ω.

2.4 Choosing Diodes

Choose the diodes that can withstand the peak current in addition to blocking at least twice the supply voltage of the charge pump stage. The forward voltage drop must be minimized for a higher efficiency.

TI recommends using the BAT54S diodes due to the low voltage drop and small package solution.

2.5 V_{GH} Regulation

The positive post regulator ensures that the output voltage remains stable when the load current varies. This stability is realized using a transistor Q4 and the shunt regulator U2, (see Figure 3). The voltage divider with R10 and R11 set the output voltage referring to the internal virtual reference voltage V_{REF} = 1.24 V of the TLVH431A, which enables to behave as an error amplifier.

Using a Zener diode instead of the shunt regulator is also possible, but TI recommends the TLVH431A due to a higher precision, small package solution, and the availability of a Q1-standard.

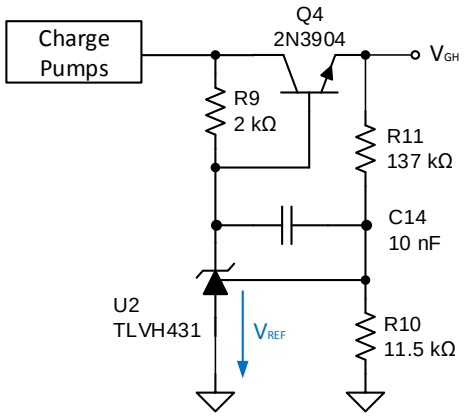

Figure 3. V_{GH} Regulator

The value of R9 is not critical, but it must be small enough to supply the Q4 base current under worst-case conditions.

The voltage on Q4 is approximately V_{GH} as Equation 8 shows:

$$V_{C(Q4)} = 3V_{POS} + 2V_{F(D2)} - V_{F(D3A)} - V_{F(D3B)} - V_{F(D4A)} - V_{F(D4B)}$$

$$VC(Q4) = 3(6.3\ V) + 2(0.5\ V) - 0.5\ V - 0.5\ V - 0.5\ V - 0.5\ V = 17.9\ V \quad (8)$$

The voltage on the base of Q4 is 16.7 V (V_{GH} + $V_{F(Q4)}$). For an output current of 10 mA (assuming a Q5 DC gain of 100), the base current is 100 µA. To bias U2, which requires at least 100 µA, R9 must not be larger then 8 kΩ.

The capacitor C14 provides stabilization of the feedback loop.

Because $V_{CE(Q4)}$ is included in the feedback loop, the voltage drop does not affect output voltage accuracy.

2.6 V_{GL} Regulator

A TLVH431A device also regulates V_{GL}, but because this device is not designed to regulate negative voltage, Q3 and $V_{BE(Q3)}$ are not included in the feedback loop (see Figure 4).

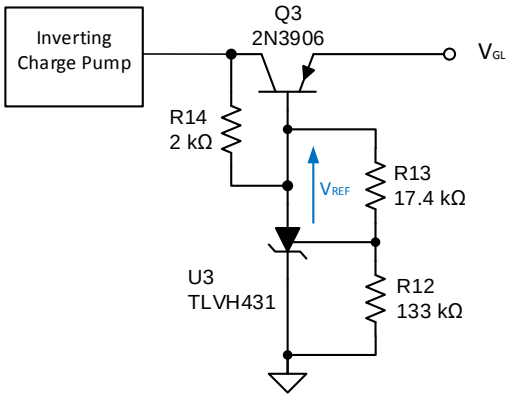

Figure 4. V_{GL} Regulator

Taking this control problem into account, the voltage divider with R13 and R12 must be set using Equation 9:

$$V_{GL} = -\left(\frac{R12}{R13}\right) \times V_{REF} + V_{BE(Q3)} \quad (9)$$

Equation 10 shows the voltage on the Q3 collector.

$$V_{C(Q3)} = -(V_{POS} + V_{F(D2)} - V_{NEG}) + V_{F(D5A)} + V_{F(D5B)}$$

$$V_{C(Q3)} = -(6.3\ V + 0.5\ V - -6.3\ V) + 0.5\ V + 0.5\ V = -12.1\ V \quad (10)$$

The value of R14 must also be no larger than 8 kΩ. Due to the feedback loop, the V_{GL} regulation over temperature and output current is slightly worse than the regulation of V_{GH}.

2.7 Unregulated

For less demanding applications, omitting the post regulator circuits is possible.

3 Performance

The following tests were performed with a 3.3-V input voltage supply. All measurements show functionality while the power safe mode is OFF on both output stages of the TPS65131-Q1 device.

3.1 Start-Up and Shutdown

3.1.1 Start-Up

Figure 5 shows the startup behavior of the positive and negative output rail V_{POS} and V_{NEG} at a load current of 100 mA. The input voltage V_{IN} has a rise time of 100 µs. The output rails V_{GH} and V_{GL} are shown at a load of 10 mA. Figure 6 shows the inrush current.

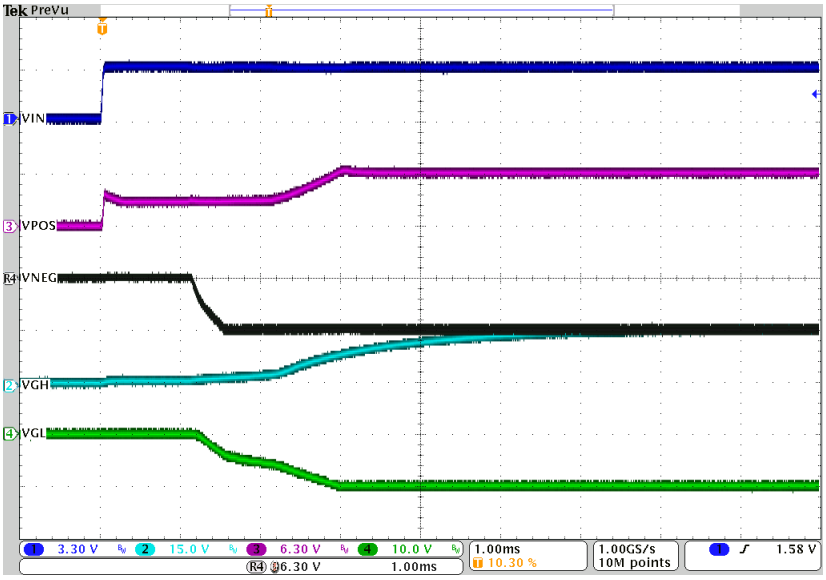

Figure 5. Start-Up

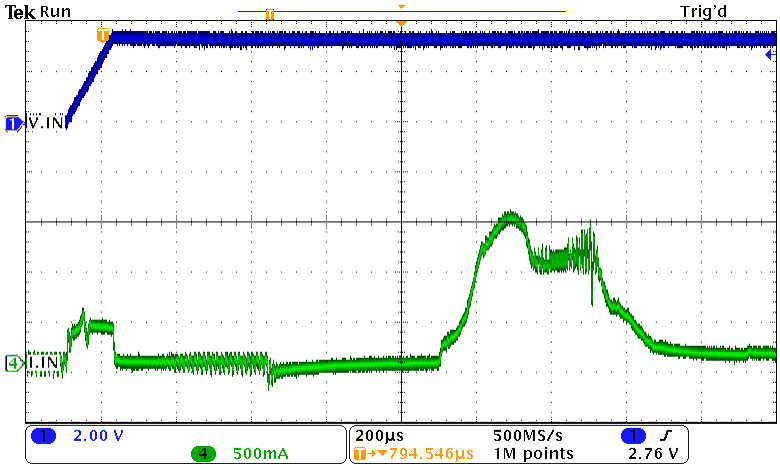

Figure 6. Inrush Current I_{IN}

3.1.2 Shutdown

Figure 7 shows the shutdown behavior of the V_{POS} and V_{NEG} outputs at a load of 100 mA.

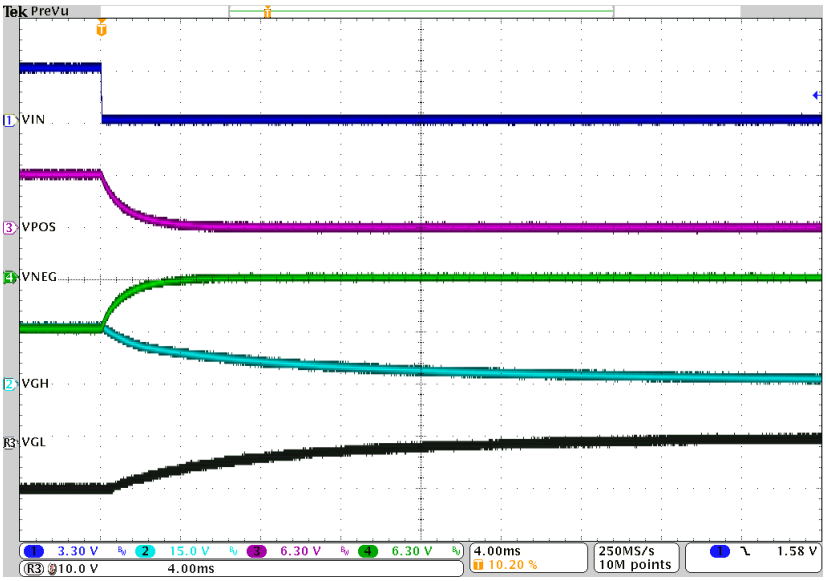

Figure 7. Shutdown

3.2 Load Transient

Figure 8 shows the load transient of the output stages of the converter. The figure also shows the voltage regulated at the load. In this example, the voltage variation of V_{POS} during load transients is up to ±20%.

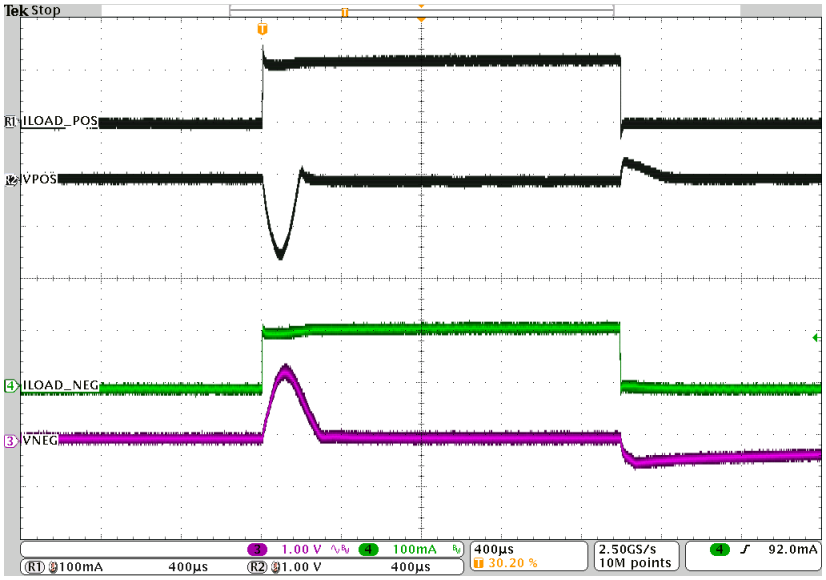

Figure 8. V_{POS} and V_{NEG} Load Transient Response (I_{OUT} = 0 mA to 100 mA)

Figure 9 shows the load transient of the charge pumps at a load of 0 A to 10 mA.

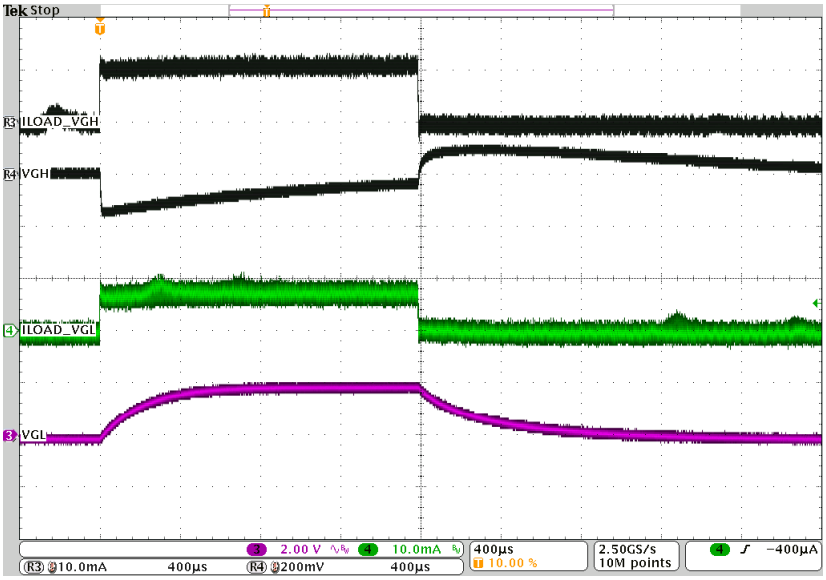

Figure 9. V_{GH} and V_{GL} Load Transient Response (I_{OUT} = 0 mA to 10 mA)

3.3 Line Transient

Figure 10 shows the line transient behavior of the output rails of the converter. The supply voltage change at V_{POS} lies in the range of ±6%, V_{NEG} lies in the range of 3%. Line transient measurements were performed for a step from V_{IN} = 0 V to V_{IN} = 3.3 V.

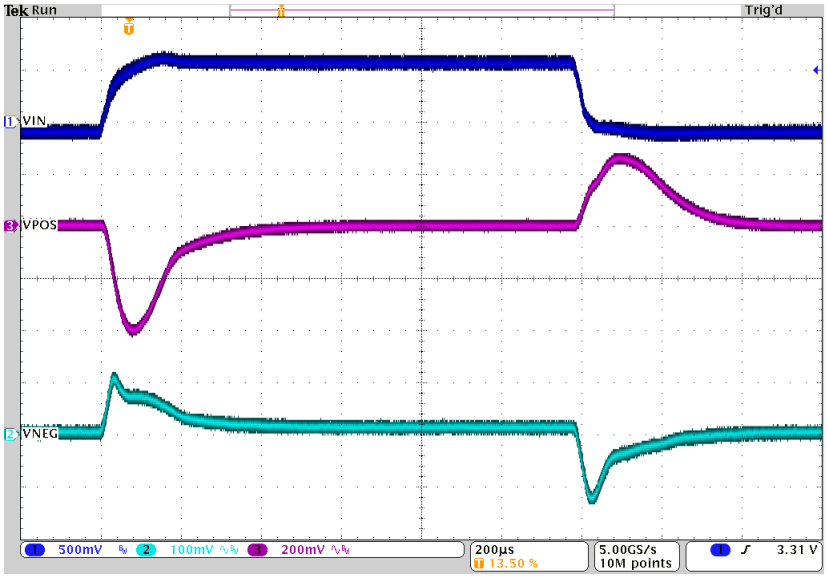

Figure 10. V_{POS} and V_{NEG} Line Transient Response

Figure 11 shows the line transient behavior of the charge pumps. The supply voltage variation is almost not visible in the curves of the load voltage.

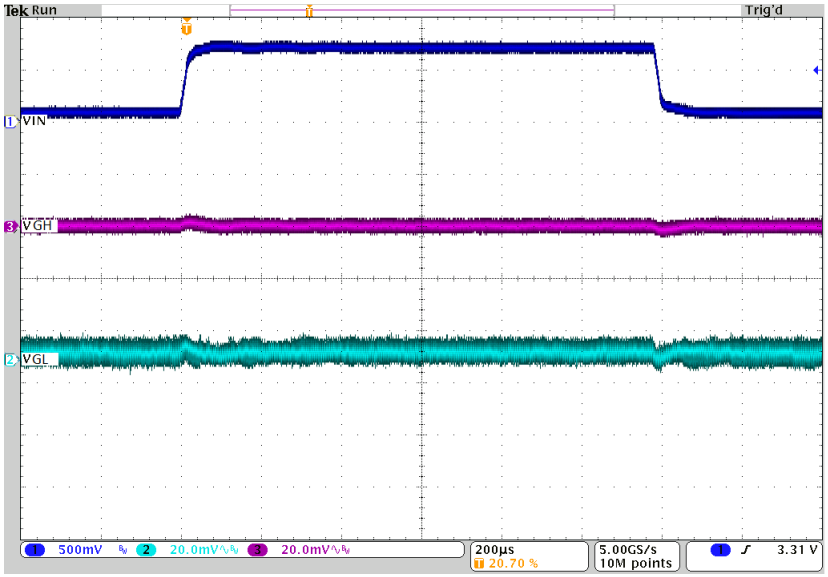

Figure 11. V_{GH} and V_{GL} Line Transient Response

3.4 Load Regulation

Figure 12 and Figure 13 show the percent change of the output voltages when increasing the load current up to 50% above the specified output current. The output voltages of the converter V_{POS} and V_{NEG} stay constant at ±6.3 V with a slight difference of almost 0.3% at 150 mA.

Due to the good performance of the positive post regulator, the output voltage of the charge pump V_{GH} is perfectly stable. V_{GL} shows a slight variation up to 1.5% at 15 mA.

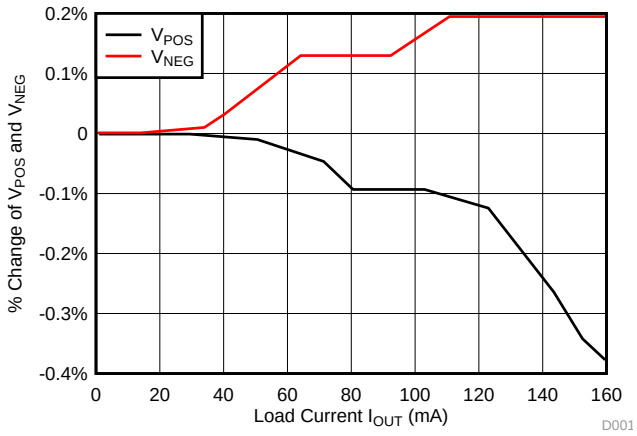

Figure 12. V_{POS} and V_{NEG} Load Regulation

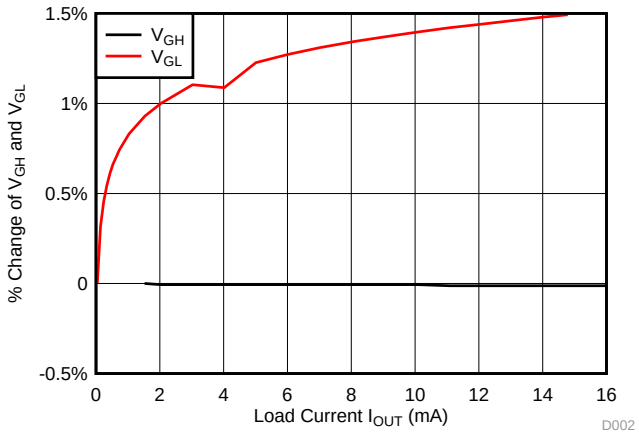

Figure 13. V_{GH} and V_{GL} Load Regulation

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