TI Designs

100-A Current Source Reference Design Using Two Power Modules in Parallel

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00582	Tool Folder Containing Design Files
PTH08T250W	Product Folder

TI E2E™ Community

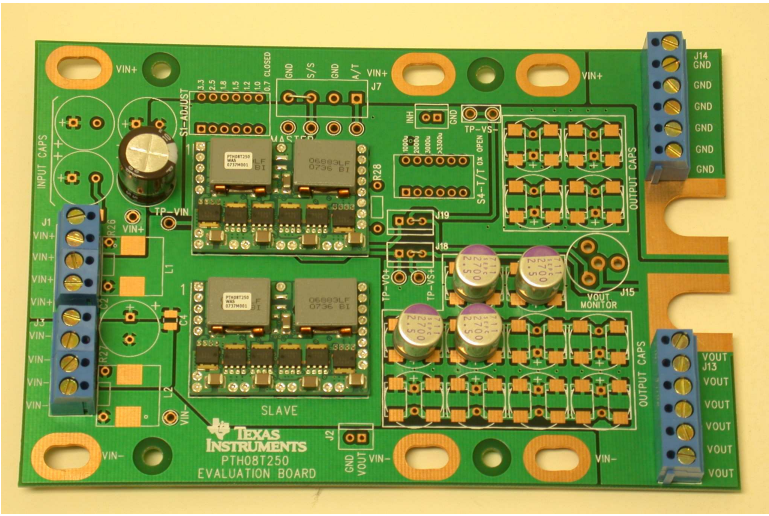
ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- Facilitates low supply voltages at very high DC currents at 100 A or more
- Low external component count
- High power density in a small package
- High-current design using a fully tested and qualified power module

Featured Applications

- FPGA Core Rails
- Blade Servers
- Telecom Base Stations



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1 Description

Powering servers and memory cards requires the generation of low supply voltages at very high DC currents approaching 100 A or more. In addition to the high-current supply requirements, dynamic load requirements are extremely demanding. The load may quickly go from an inactive low-current state to a fully processing high-current state while requiring precise voltage regulation.

A stand-alone, dual-phase power module like the Texas Instruments (TI) PTH08T250W can supply up to 50 A of output load current. However, the PTH08T250W incorporates a stackable controller feature that allows the outputs of multiple modules to be connected in parallel, thereby producing a reliable solution capable of supplying a load current of 100 A or more. Configuring a PTH08T250W as a master and each additional module as a slave allows start-up and transient conditions to be controlled by a single module. Figure 10 shows a typical two-module solution where all of the features and inputs are controlled by the master device while the slave inputs are left open.

2 Design Features

The PTH08T250W operates over a wide 4.5- to 14-V input voltage range and generates a positive output voltage of 0.7 to 3.6 V. Additionally, the PTH08T25xW family of power modules is designed to meet a very tight 1.5% DC tolerance, deliver exceptional transient response, and have the ability to synchronize to an external frequency.

3 Specifications

Table 1. Operating Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		4.5		14	V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		0.7		3.6	V
I_{OUT}	Output current				100	A

4 Test Data

4.1 Efficiency

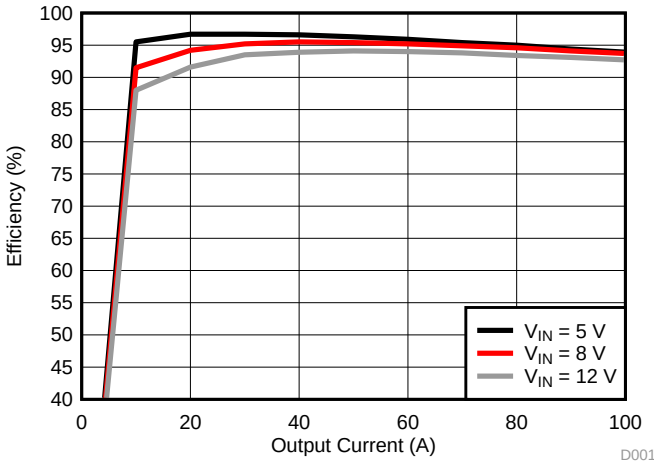

Figure 1. Efficiency, V_{OUT} = 3.3 V

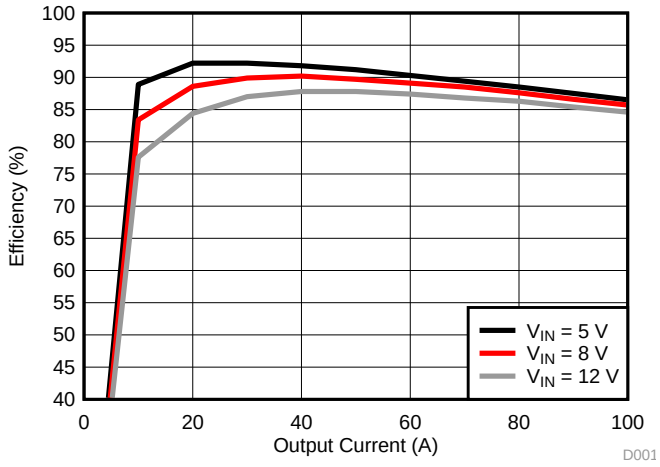

Figure 2. Efficiency, V_{OUT} = 1.2 V

4.2 Power Dissipation

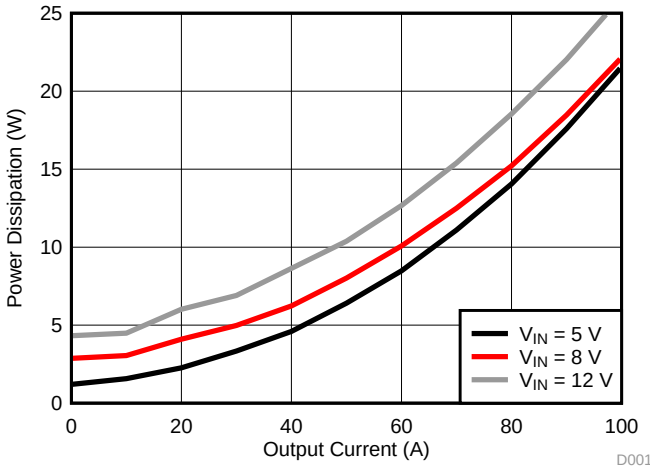

Figure 3. Power Dissipation, V_{OUT} = 3.3 V

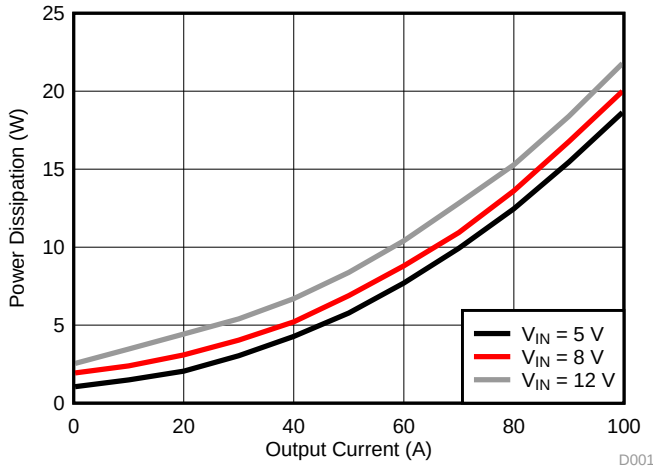

Figure 4. Power Dissipation, V_{OUT} = 1.2 V

4.3 Output Voltage Ripple

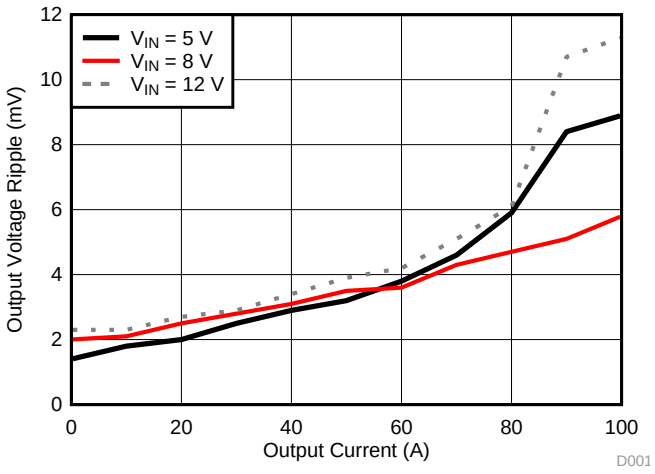

Figure 5. Output Voltage Ripple, V_{OUT} = 3.3 V

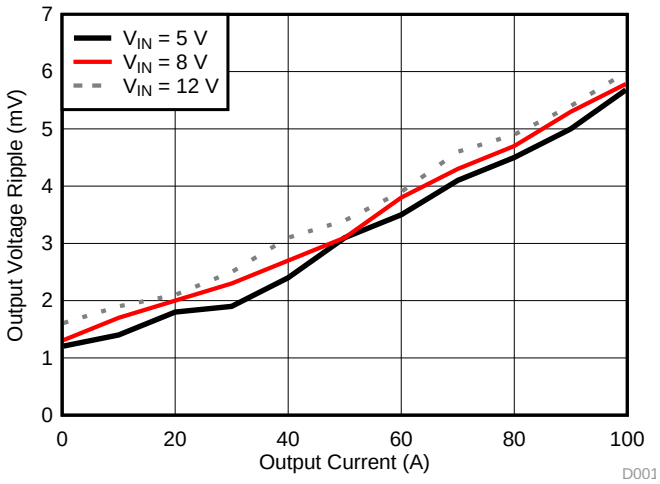

Figure 6. Output Voltage Ripple, V_{OUT} = 1.2 V

4.4 Transient Response Waveforms

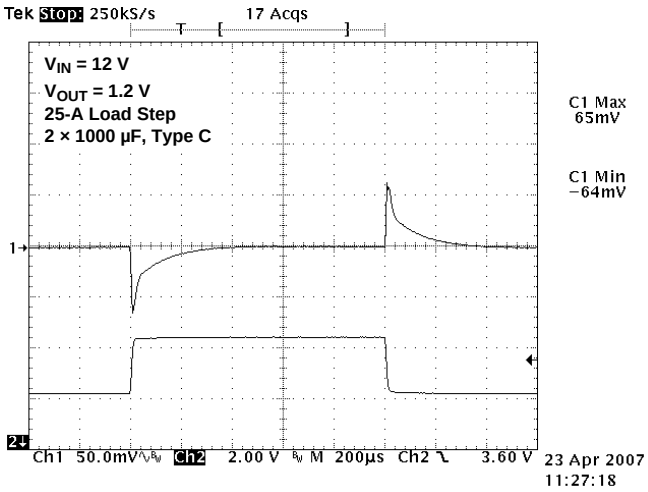

Figure 7. Transient Response

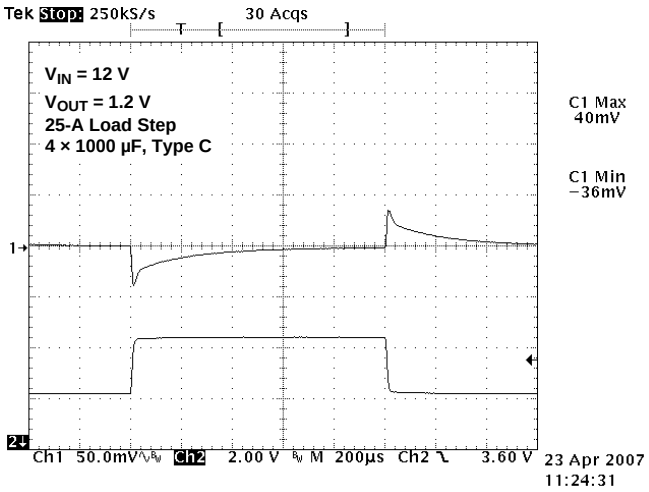

Figure 8. Transient Response

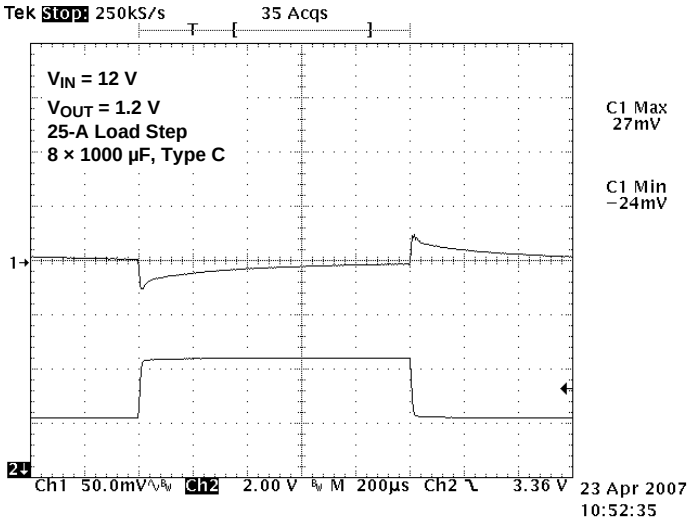

Figure 9. Transient Response

5 Design Files

5.1 Schematic

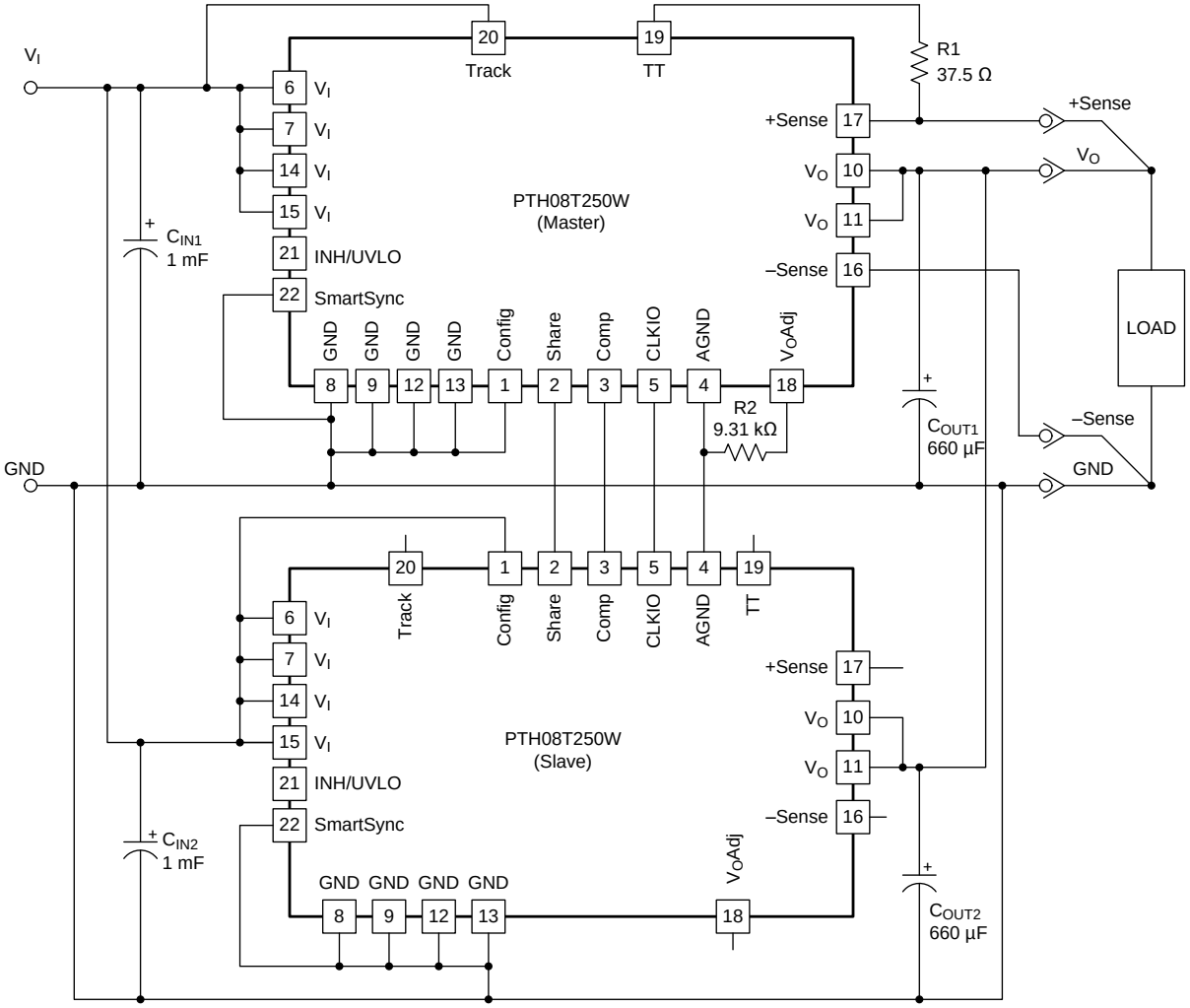

Figure 10. 100-A Current Source Design Schematic

To download the full EDA schematic, see the design files at TIDA-00582.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00582.

5.3 PCB Layout

Pay special attention to the board layout for this parallel application. These items determine the amount of current each solution can deliver:

- amount of board space
- number of layers
- amount of copper

- A careful layout maintains the interconnection pins as clean as possible.
- Route the power planes, (V_{IN}, V_{OUT}, and GND) to the power pins in a tight, short, and wide path.
- Prevent the VIN plane from running above or below the V_{OUT} plane wherever possible helps reduce

overall switching noise.

- Maintain a short and tight path from the output of each module to the load minimizes losses.
- Route the +Sense and –Sense connections to the load in a direct path, closely coupled with one another. The layout around these traces should be isolated as much as possible to avoid picking up switching noise. Additionally, connecting the ±Sense lines through a surface-mount resistor to the load allows a resistor with a value between 1 Ω and 2 Ω to be placed in the sense path to aid in filtering.
- Ensure to isolate the three interconnection traces (Share, Comp, and CLKIO) from the rest of the board to prevent switching noise from aggravating the signals to the slave modules.
- Because AGND acts as a shield ensure that it runs on an adjacent layer to the other three traces.
- Route the CLKIO trace to maintain a slight distance from the Comp trace to reduce the chance of clock pulses disturbing the Comp signal.
- See Figure 11 for an example layout of the interconnection pins. The three interconnection traces are routed on one layer, and the AGND is routed as a copper area that shields the three traces on an adjacent layer. When multiple modules are operated in parallel, an eight-layer layout with 2-oz. copper is recommended to improve thermal conduction. Increased copper thickness is required to distribute the higher current over the power planes. Increased airflow is also strongly recommended to help the copper remove the heat associated with the higher power solution.

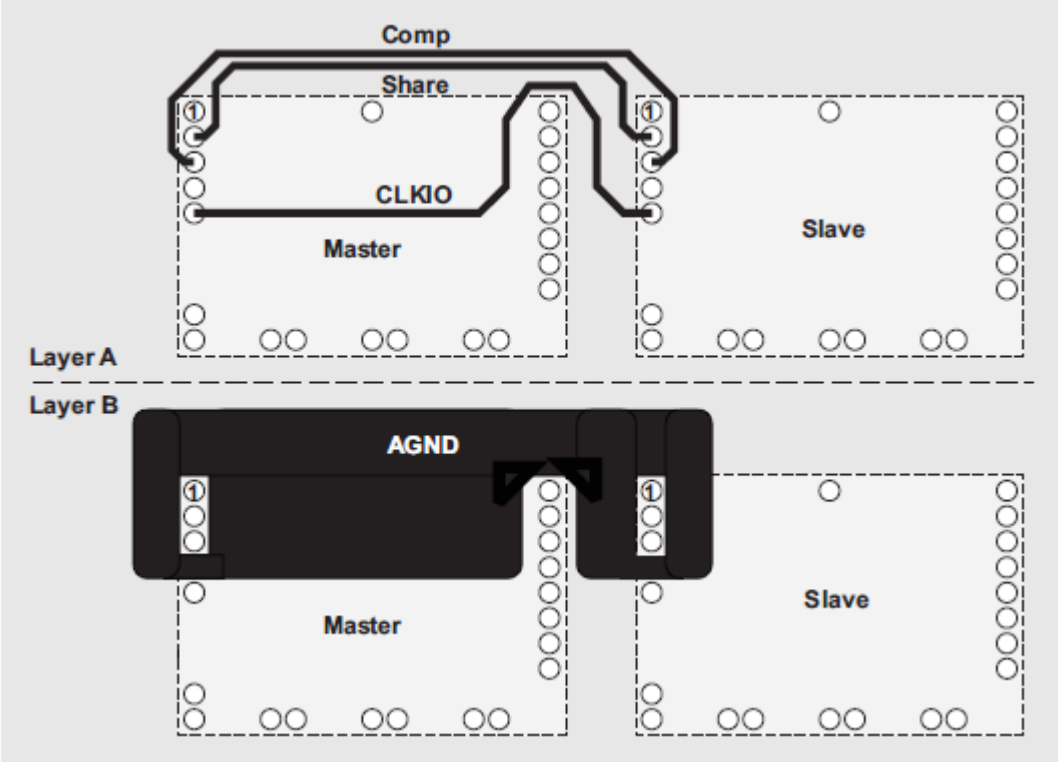

Figure 11. Board Layout Interconnection Pins

5.3.1 Parallel Connections

When multiple modules are operated in parallel, the control of each device feature is set only on the master device. A device is configured as a master by connecting the Config pin to the power GND. All slave devices must connect the Config pin to VIN. The slave devices must leave all other control pins open (connect the SmartSync pin to the GND). See Table 2 for pin connections of the master and slave modules. See Figure 11 in the Section 5.3 section.

Table 2. Master and Slave Pin Connections

PIN NAME	MASTER	SLAVE
V_{IN}	Connect to the input bus.	Connect to the input bus.
V_{OUT}	Connect to the output bus.	Connect to the output bus.
GND	Connect to the common power GND.	Connect to the common power GND.
INH/UVLO	Use for inhibit control and UVLO adjustment. If unused, leave open-circuit.	No connection. Leave open-circuit.
V_{OUT} Adjust	Use to set the output voltage. Connect R_{SET} resistor between this pin and AGND.	No connection. Leave open-circuit.
+Sense	Connect to the output voltage either at the load or at the module.	No connection. Leave open-circuit.
–Sense	Connect to the output GND either at the load or at the module.	No connection. Leave open-circuit.
Track	Connect to Track control. If unused, connect to VIN.	No connection. Leave open-circuit.
TurboTrans	Connect TurboTrans resistor, RTT, between this pin and +Sense pin.	No connection. Leave open-circuit.
SmartSync	Connect to an external clock. If unused, connect to GND.	Connect to the common power GND.
Config	Connect to the common power GND.	Connect to the input bus.
Share	Connect to pin 2 of the slave.	Connect to pin 2 of the master.
Comp	Connect to pin 3 of the slave.	Connect to pin 3 of the master.
AGND	Connect to pin 4 of the slave.	Connect to pin 4 of the master.
CLKIO	Connect to pin 5 of the slave.	Connect to pin 5 of the master.

To download the layer plots, see the design files at TIDA-00582.

5.4 TIDA-00582 Assembly Drawing and PCB Layout

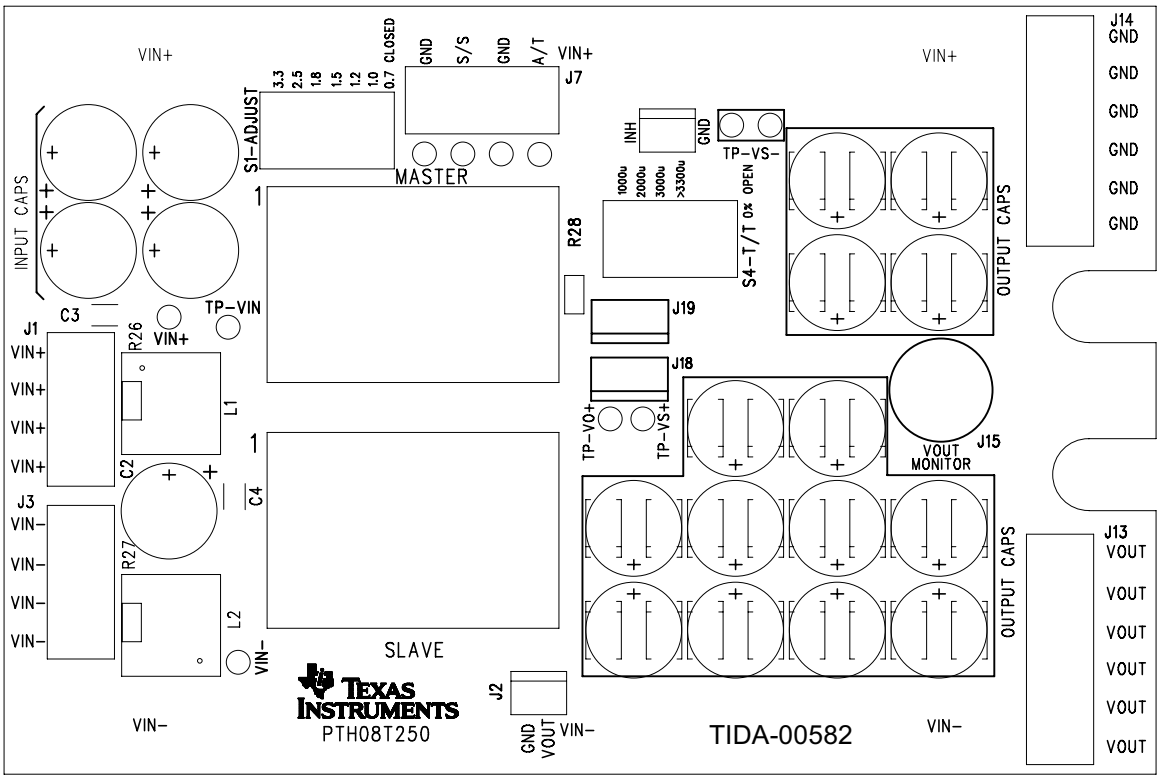

Figure 12. Top Layer (Top View)

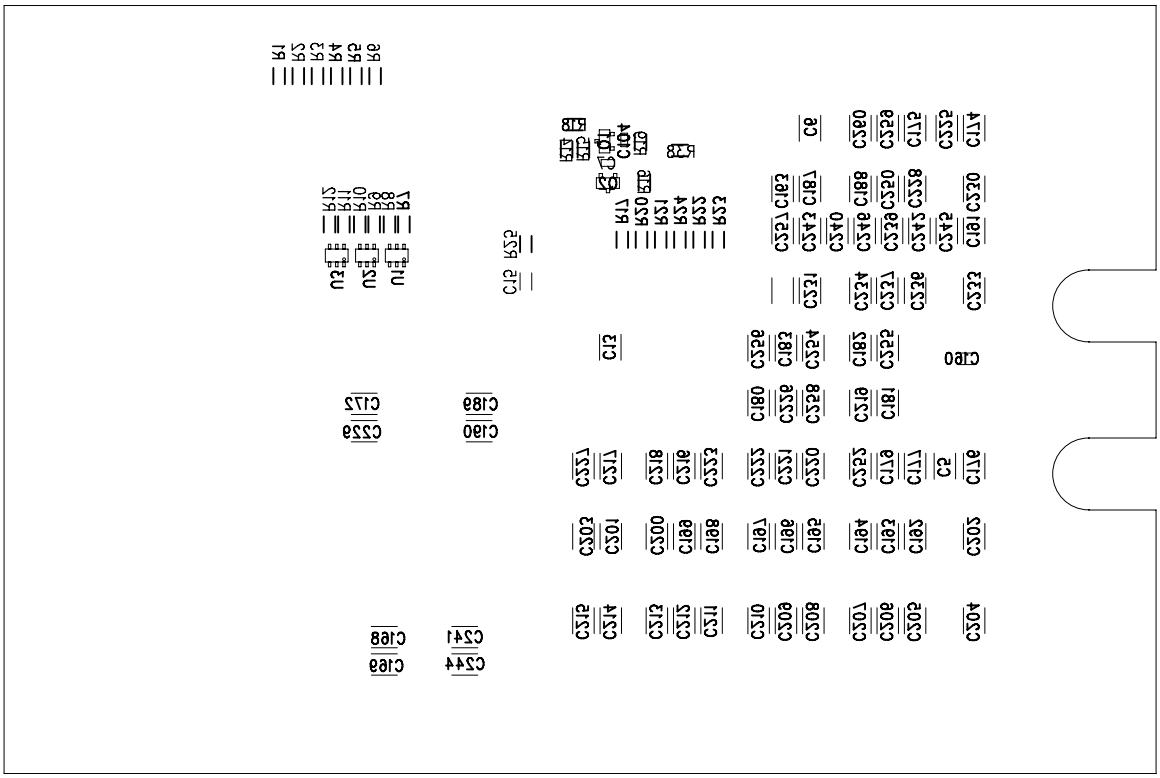

Figure 13. Bottom Layer (Bottom View)

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00582

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