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Fast Settling 16-bit 1MSPS Multiplexed Data Acquisition Reference Design

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Design Resources

TIPD169	All Design files
TINA-TI™	SPICE Simulator
OPA625	Product Folder
OPA320	Product Folder
OPA333	Product Folder
REF5045	Product Folder
THS4281	Product Folder
ADS8860	Product Folder
TS5A3159	Product Folder

Circuit Description

This design is for a 16-bit 1MSPS single ended multiplexed data acquisition system (DAQ) for dc inputs. The system is composed of a 16-bit successive-approximation-register (SAR) analog-to-digital converter (ADC), SAR ADC driver, reference driver, and multiplexer. The design shows the process to optimize a single-ended multiplexed DAQ to achieve fast settling at a sampling rate of 1MSPS.

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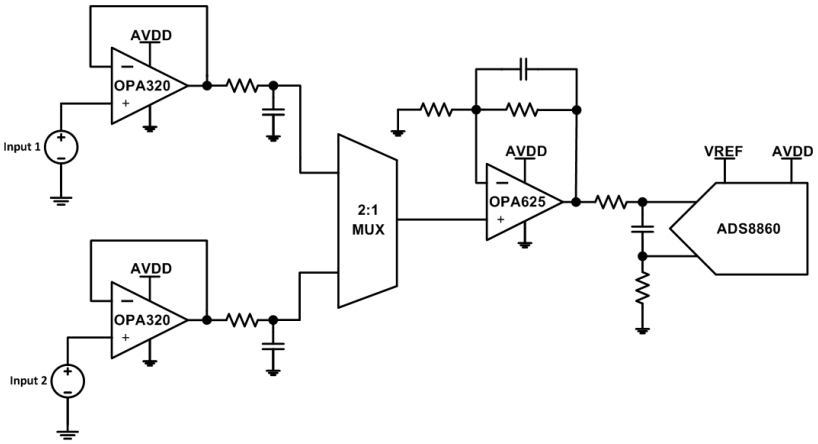
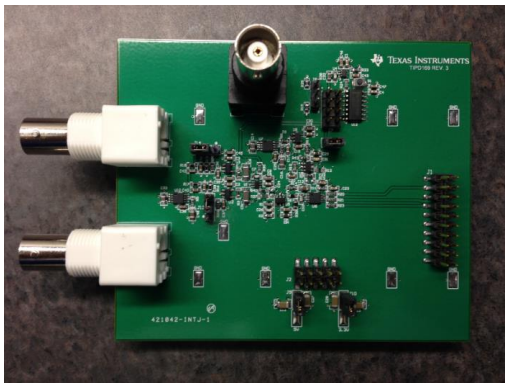




1 Design Summary

The design requirements are as follows:

- System Supply Voltage: 5 V
- ADC Supply Voltage: 3.3 V
- ADC Reference Voltage: 4.5 V
- ADC Sampling Rate: 1 MSPS
- Input Voltage Step: 2 Vpp

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Settling Time	<500 ns	341 ns	390 ns
Effective Resolution	15.5 bits	N/A	15.72 bits
Signal-to-Noise Ratio$_{SYS}$(SNR$_{SYS}$)	> 83 dB	N/A	83.51 dB
Total Harmonic Distortion$_{SYS}$(THD$_{SYS}$)	< -100 dB	N/A	-102.99 dB
Effective Number of Bits$_{SYS}$(ENOB$_{SYS}$)	> 13.5 bits	N/A	13.57 bits

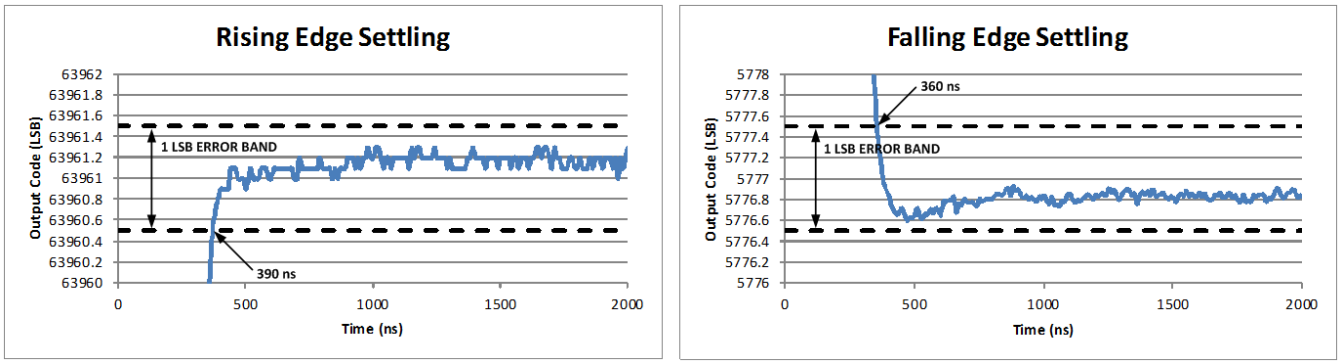


Figure 1: Measured Settling Times

2 Theory of Operation

Figure 2 shows a complete system block diagram of the multiplexed DAQ. The system consists of an input low pass filter, multiplexer, SAR ADC driver, anti-aliasing filter, SAR ADC, and a reference driver. To achieve the fast settling required at a sampling rate of 1MSPS each block in the system must carefully be designed.

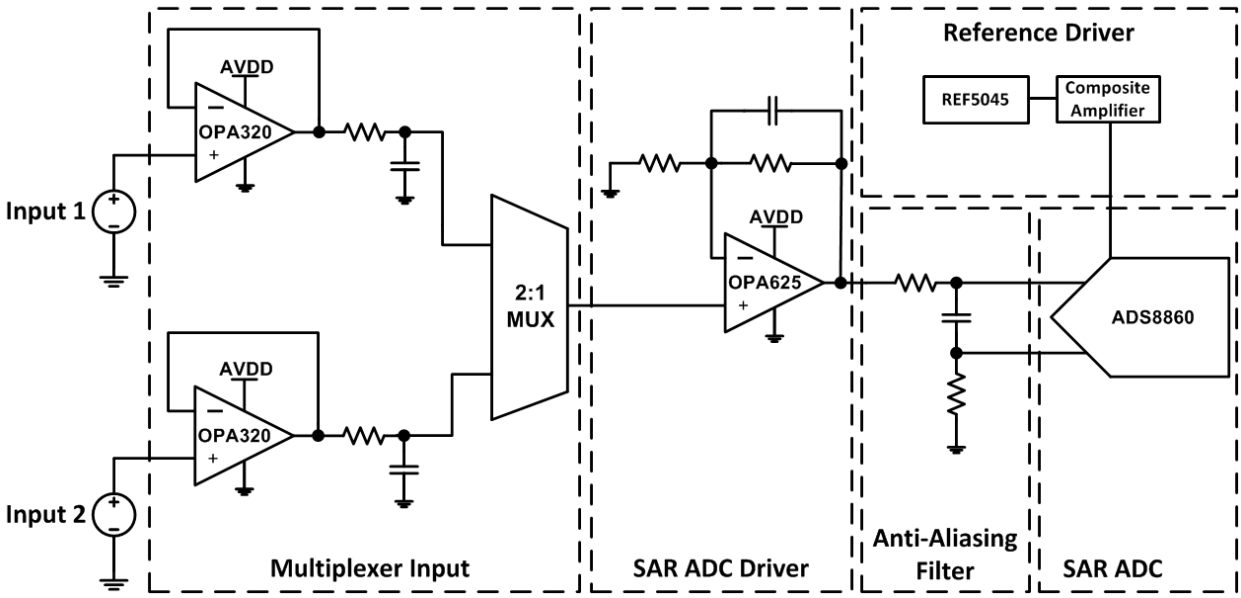


Figure 2: System Block Diagram

2.1 Understanding ADC Static and Dynamic Performance

The overall performance of a system is determined by measuring specifications such as SNR, THD, SINAD, ENOB, and effective resolution. The ac performance is determined using SNR, THD, SINAD, and ENOB while dc performance is determined using effective resolution. Please refer to TIPD173 for more details about these specifications.

2.2 Understanding Multiplexed DAQ Linearity Requirements

In a multiplexed DAQ, two main design considerations must be taken with the multiplexer to ensure high linearity and fast settling of the system. The first is to drive the input of the multiplexer with a low impedance source and provide sufficient charge transfer when the multiplexer is switched to eliminate voltage errors. The second is to provide a high impedance at the output of the multiplexer to eliminate gain error and gain non-linearity introduced by the multiplexer's on resistance.

2.2.1 Low Impedance Input and Charge Transfer

Figure 3 shows a simplified model of a multiplexer. Multiplexers typically have ohms of on resistance (R_{on}) and tens of picofarads of drain capacitances (C_D). When the multiplexer is switched, C_D needs to quickly settle to the voltage applied to the input of the newly selected channel. If a high impedance source is at the input of the multiplexer, C_D will take a long time to settle to the new channels input voltage, creating a voltage error at the output of the multiplexer. Therefore, the input of the multiplexer must be driven with a low impedance source as shown in Figure 4.

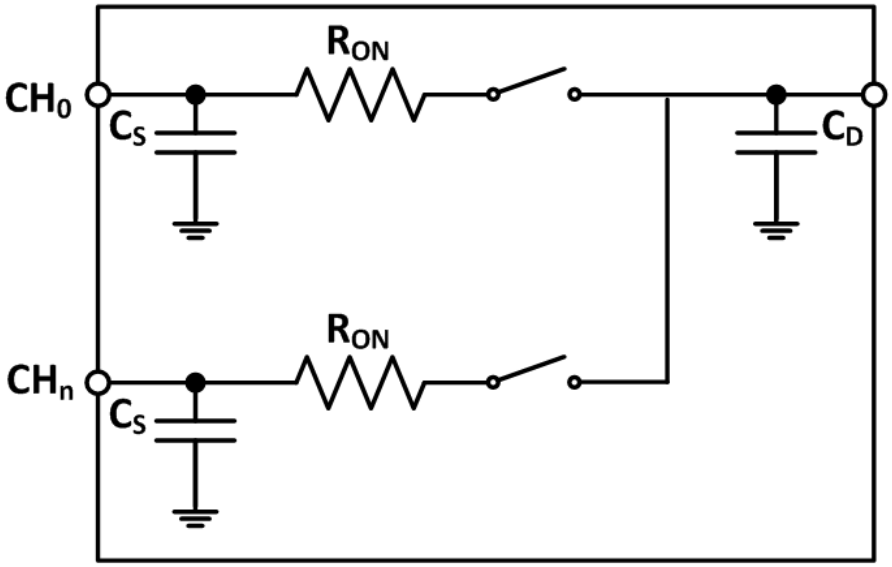


Figure 3: Simplified Multiplexer Model

It is important to select an appropriate value for C_{FLT} to allow for instant charge transfer between C_{FLT} and C_D when the multiplexer is switched. Small values for C_{FLT} cause the voltage on C_{FLT} to droop, causing long settling times. The value of C_{FLT} can be calculated using Equation **(1)**. For a derivation of Equation **(1)**, please refer to TIPD151.

$$C_{FLT} > \frac{C_D}{0.1} - C_D - C_S \quad (1)$$

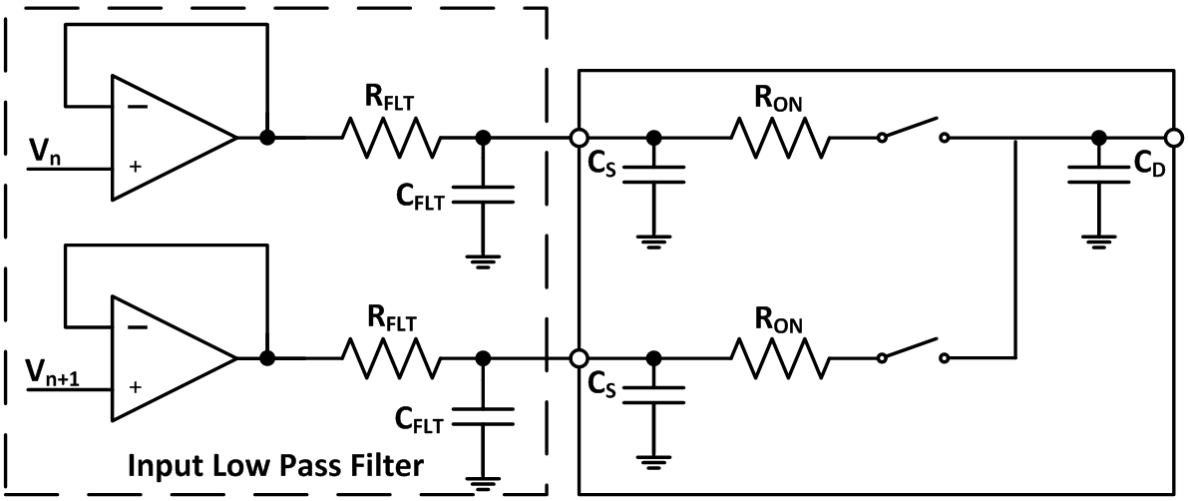


Figure 4: Low Impedance Input and Charge Distribution Circuitry

In Figure 4, R_{FLT} acts as an isolation resistor to stabilize the op amp driving the multiplexer. Choosing a large value for R_{FLT} will increase the phase margin of the op amp but also increases the settling time. Therefore, choose R_{FLT} such that the op amp is stable but the settling time does not exceed the design requirements.

The bandwidth of the input to the multiplexer (BW_{FLT}) is dependent upon R_{FLT} and C_{FLT} and can be calculated using Equation **(2)**.

$$BW_{FLT} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (2)$$

2.2.2 High Impedance at the Multiplexer Output

The R_{on} of a multiplexer can vary between channels of the multiplexer and is dependent on the common mode voltage. These variances in R_{on} cause gain error and gain non-linearity. To eliminate these errors, the output of the multiplexer must connect to a high impedance node. Equation **(3)** and Equation **(4)** show the equations for gain error and gain non-linearity at the output of the multiplexer.

$$GainError = \left(1 - \frac{R_{out}}{R_{out} + R_{on}}\right) \times 100 \quad (3)$$

$$Gain\_NonLinearity = \left(1 - \frac{R_{out}}{R_{out} + R_{on} + \Delta R_{on}}\right) \times 100 \quad (4)$$

Where: R_{out} is the resistance at the output of the multiplexer

R_{on} is the on resistance of the multiplexer

ΔR_{on} is the change in on resistance of the multiplexer due to common mode voltage

Equation **(3)** and Equation **(4)** show that higher multiplexer output impedances result in lower gain errors and gain non-linearities. Buffering the output of the multiplexer with a non-inverting amplifier results in a very high multiplexer output impedance.

2.3 Settling Time Requirements

In a multiplexed DAQ, the ADC input must settle to within the desired error band in less than the combined acquisition and conversion times of the ADC. For a robust design, the ADC input should settle in half of that time. This allows for variation in component specifications, temperature drift, process shift, and aging over the products life. Equation **(5)** estimates the total settling time of the system (t_{System}) by calculating the root sum square (RSS) of each block in Figure 2.

$$t_{System} = \sqrt{t_{Multiplexer}^{\ 2} + t_{OPA}^{\ 2} + t_{ADC\_Driver}^{\ 2} + t_{Filter\_ADC}^{\ 2}} \quad (5)$$

Where: $t_{Multiplexer}$ is the settling time of the multiplexer.

t_{OPA} is the settling time of the amplifier in the input low pass filter circuit.

t_{ADC_Driver} is the settling time of the ADC driver.

t_{Filter_ADC} is the settling time of the anti-aliasing filter.

2.3.1 Multiplexer and ADC Timing

Figure 5 shows a timing diagram that is optimized to allow for the longest time possible for the system to settle.

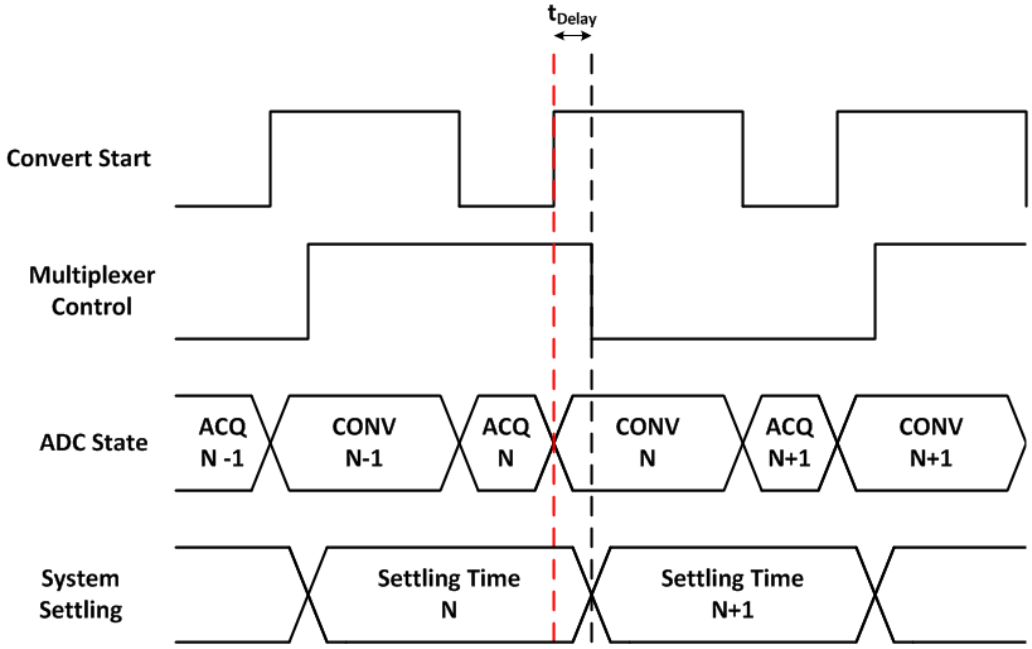


Figure 5: Multiplexer Timing Diagram

During the conversion phase (CONV), the ADC input is disconnected from the circuit and converts the previous acquired sample (N-1) into a digital value. Because the input to the ADC is disconnected from the circuit during conversion, the multiplexer can switch and have no effect on sample N-1. After the conversion phase, the acquisition of the current sample (N) begins. During acquisition (ACQ), the ADC input is connected to the circuit and the internal sample and hold capacitor of the ADC charges to the voltage at the input of the ADC. To avoid a conversion error of sample N, the system must settle before the conversion of sample N begins, indicated by the red line in Figure 5. Switching the multiplexer at the start of conversion gives the combined conversion and acquisition times of the ADC for the system settle. To prevent the multiplexer from switching before the conversion begins, a time delay (t_{delay}) is added after the convert start goes high. The total time the system has to settle is shown in Equation **(6)**.

$$t_{settle} = t_{acq} + t_{conv} - t_{delay} \quad (6)$$

Where: t_{settle} is the maximum time the system has to settle.

t_{acq} is the acquisition time of the ADC.

t_{conv} is the conversion time of the ADC.

2.3.2 SAR ADC Driver/Multiplexer Buffer Settling Time Considerations

In multiplexer applications, large steps can be applied to the input of the amplifier when the multiplexer switches. When a large step is applied to a non- inverting amplifier with differential input clamp diodes, the diodes will conduct. During this time, the non-inverting input and inverting input are shorted together through the forward biased diodes. When the diodes conduct, the output of the multiplexer is connected to the gain network of the amplifier as shown in Figure 6. This allows current flow through the diodes, which can damage the device if not limited properly. The current through the diodes can be calculated using Equation **(7)**.

$$I_{diode} = \frac{V_{positive} - V_{negative} - V_{diode}}{R_{on} + R_f \,//\, R_g} \quad (7)$$

Where: $V_{positive}$ is the positive full-scale input

$V_{negative}$ is the negative full-scale input

V_{diode} is the voltage drop across the diode

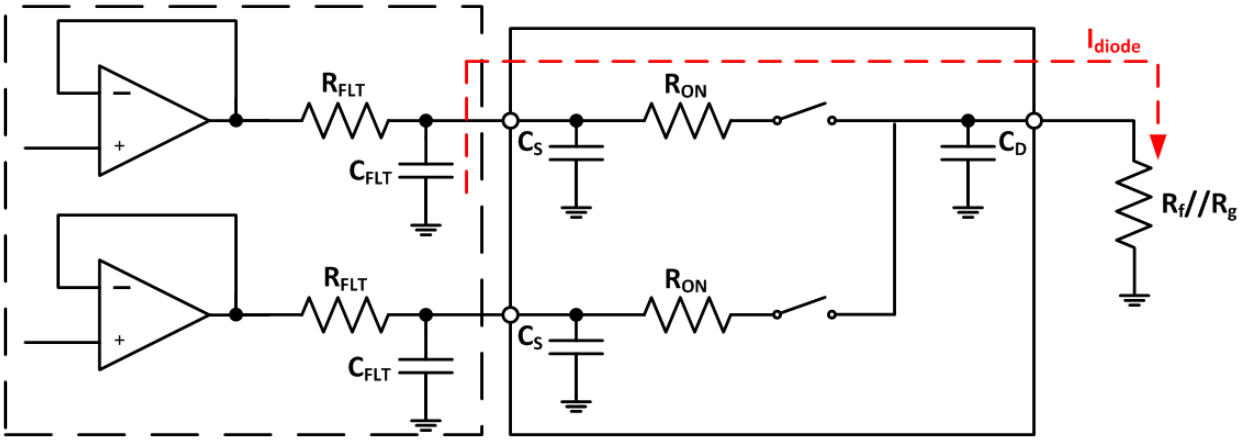


Figure 6: Amplifier Gain Network Connected to the Output of Multiplexer

When current flows through the diodes, a large voltage droop will occur on C_{FLT} resulting in long settling times. To limit the voltage droop on C_{FLT}, the resistors in the gain network can be increased to reduce the current or C_{FLT} can be increased to supply more charge for the increase in current. Increasing the resistors in the gain network introduces more noise in the system and degrades the ac performance and increasing the capacitance of C_{FLT} decreases the bandwidth of the input to the multiplexer as shown in Equation **(2)**. Therefore, a balance must be made to meet the design requirements.

2.4 SAR ADC Driver Requirements

The amplifier that buffers the output of the multiplexer also operates as the SAR ADC driver as shown in Figure 2. To properly drive a SAR ADC, the amplifier must have low total harmonic distortion (THD), low noise, high slew rate, fast settling, and high bandwidth. Low THD and low noise is required so that the amplifier does not degrade the ac performance of the ADC. High slew rate and fast settling are required to achieve fast settling when large steps are required on the output of the amplifier. When the output of the amplifier is required to change rapidly, the rate at which the output can change is dominated by the slew rate. Therefore, driving the SAR ADC with an amplifier with high slew rate, high bandwidth, and fast settling allows the output to transition at a fast rate with minimal ringing.

2.5 Anti-Aliasing Filter Requirements

The RC anti-aliasing filter, shown in Figure 2, filters out noise introduced by components in the signal chain and reduces kick back from the sample and hold capacitor of the ADC. The capacitor of the anti-aliasing filter should be sized according to the datasheet of the ADC. The capacitor acts as a charge bucket to quickly charge the sample and hold capacitor of the ADC during the acquisition phase. Having a capacitor on the output of an amplifier degrades the phase margin; therefore, an isolation resistor must be used to stabilize the amplifier. The resistor must be large enough to stabilize the amplifier but should be kept below what is recommended in the ADC datasheet. The bandwidth of the filter should be chosen such that it does not attenuate the input signal but kept low enough to filter out noise fed into the ADC to increase the SNR of the system. The bandwidth of the anti-aliasing filter can be calculated using Equation **(8)**.

$$BW_{Anti-Alia\sin g} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (8)$$

2.6 Noise and THD Requirements

The total noise of the system is the contribution of each component in the signal chain shown in Figure 2. The components should be chosen carefully to not degrade the overall SNR of the system. It is important to do a full noise analysis of the system to determine what the main source of noise is. It is best to refer all noise sources to the input of the amplifier so that the noise calculations are not dependent on gain.

The bandwidth of the input filter can be calculated using Equation 2 and should be used as the cutoff frequency (f_c) for the noise calculation of the input filter. The noise bandwidth of the OPA320 (BW_{n_OPA320}) can be calculated using Equation **(9)**.

$$BW_{n\_OPA320} = K_n \times f_c \quad (9)$$

Where K_n is the brickwall filter multiplier.

The broadband noise (e_{n_bb}) can be calculated using Equation **(10)**.

$$e_{n\_bb\_OPA320} = e_{bb} \times \sqrt{BW_{n\_OPA320}} \quad (10)$$

To calculate the noise due to the 1/f region ($e_{n\_1/f}$) , the noise must be normalized ($e_{n\_normalized}$) . This is done using Equation **(11)**.

$$e_{n\_normalized\_OPA320} = e_{1/f} \times \sqrt{f_{1/f}} \quad (11)$$

Where : $f_{1/f}$ = the frequency at which the 1/f noise is measured at.

$e_{1/f}$ = the noise spectral density measured in the 1/f region.

The noise due to the 1/f region is then calculated using Equation **(12)**.

$$e_{n\_1/f\_OPA320} = e_{n\_normalized\_OPA320} \times \sqrt{\ln\left(\frac{BW_{n\_OPA320}}{f_{1/f}}\right)} \quad (12)$$

The total input referred noise of the input filter ($e_{n\_Total\_OPA320}$) can then be calculated by taking the root sum square (RSS) of the 1/f noise and the broadband noise as shown in Equation **(13)**.

$$e_{n\_Total\_OPA320} = \sqrt{e_{n\_bb}{}^2 + e_{n\_1/f}{}^2} \quad (13)$$

The input referred noise due to the SAR ADC driver circuitry ($e_{n\_Total\_SAR\_Drive}$) can be calculated in a similar manner as used for the input filter. However, the calculation must also include the noise due to the current noise of the amplifier and noise due to resistors.

The cut off frequency used to calculate the noise bandwidth of the SAR ADC driver circuit (BW_{n_OPA625}) should be used as the bandwidth of the anti-aliasing filter calculated in Equation **(8)**. The same process can then be used to calculate the broadband ($e_{n\_bb\_OPA625}$) and 1/f noise (e_{n_1/f_OPA625}) as described above using the newly calculated noise bandwidth.

The noise due to the current noise of the SAR ADC driver (e_{n_I}) can be calculated using Equation **(14)**.

$$e_{n\_I} = I_{n\_OPA625} \times \sqrt{R_f \,//\, R_g} \quad (14)$$

To calculate the current noise in units of Vrms, Equation 14 must be multiplied by the noise bandwidth of the SAR ADC driver circuit as shown in Equation **(15)**.

$$E_{n\_I} = e_{n\_I} \times \sqrt{BW_{n\_OPA625}} \quad (15)$$

The thermal noise due to the resistors in the gain network (e_{n_R}) can be calculated using Equation **(16)**.

$$e_{n\_R} = \sqrt{4 \times k \times T \times BW_{n\_OPA625} \times \left(R_f \,//\, R_g\right)} \quad (16)$$

Where: k = Boltzmann's constant

T = Temperature in Kelvin

The total noise at the input of the SAR ADC driver circuitry can be calculated by taking the RSS of the broadband noise, 1/f noise, current noise, thermal noise, and the total noise of the input filter as shown in Equation **(17)**.

$$e_{n\_Total\_OPA625} = \sqrt{e_{n\_bb\_OPA625}^{\ 2} + e_{n\_1/f\_OPA625}^{\ 2} + E_{n\_I}^{\ 2} + e_{n\_R}^{\ 2} + e_{n\_Total\_OPA320}^{\ 2}} \quad (17)$$

The total input referred noise, shown in Equation **(17)**, can be multiplied by the gain of the SAR ADC driver to give the total output-referred noise ($e_{n\_Total\_Out}$) as shown in Equation **(18)**.

$$e_{n\_Total\_Out} = e_{n\_Total\_OPA625} \times \frac{R_f + R_g}{R_g} \quad (18)$$

To calculate the total RMS noise of the system, the ADC noise must also be considered. The noise of the ADC can be calculated using Equation **(19)**.

$$e_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{\frac{SNR(dB)}{20}} \quad (19)$$

The total noise of the system ($e_{n\_Total\_System}$) can then be calculated using Equation **(20)**.

$$e_{n\_Total\_System} = \sqrt{e_{n\_ADC\_RMS}^{\ 2} + e_{n\_Total\_Out}^{\ 2}} \quad (20)$$

To prevent degrading the THD performance of the ADC each device should be chosen such that it is at least 10dB lower than the THD performance of the ADC. It is important to check the THD specification for the load that the device will have. It is also important to choose C0G or NP0 capacitors where applicable as these capacitors have stable electrical characteristics under varying voltages, frequencies, time, and temperature.

2.7 Reference Driver Circuitry

The reference driver circuit, shown in Figure 7, uses the composite amplifier topology with a high precision low drift and low noise reference to provide a high bandwidth low noise circuit with high dc precision. For more details on the composite amplifier reference driver, please refer to TIPD115.

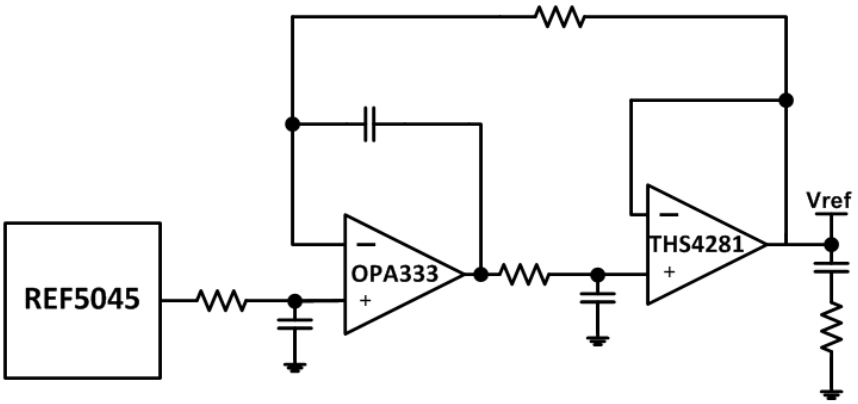


Figure 7: Reference Driver Circuitry

3 Component Selection

3.1 ADC Selection

The ADC is selected to be the ADS8860. This single ended SAR ADC has 16-bit resolution and can sample at 1 MSPS, therefore meeting the resolution and sampling rate requirement of the design. Table 2 lists the parameter of the ADS8860 relevant to this design.

Table 2: ADS8860 Specifications

Parameter	Value
Resolution	16-bit
Sampling Rate	1 MSPS
t_{acq}	290 ns
t_{conv}	710 ns
Reference Voltage	2.5 V – 5 V
AVDD	2.7 V – 3.6 V
DVDD	2.7V – 3.6V
SNR	93 dB
THD	-108 dB

As stated in section 2.3.1, the total time the system has to settle is dependent on the acquisition and conversion times of the ADC. Using Equation **(6)**, with a time delay of 10 ns, the total time the system has to settle is 990 ns. However, for a robust design, the system should settle in less than half of the combined acquisition and conversion time. Therefore, this system must settle in less than 500 ns.

3.2 Multiplexer

The multiplexer is selected to be the TS5A3159. This multiplexer was chosen for the low on resistance (R_{on}), R_{on} flatness, excellent R_{on} matching between channels, and fast transition between channels. Table 3 lists the parameter of the TS5A3159 relevant to this design.

Table 3: TS5A3159 Specifications

Parameter	Value
ON Resistance (R_{on})	1 Ω
R_{on} Flatness	0.233 Ω
R_{on} Matching	0.1 Ω
Drain Capacitance (C_D)	84 pF
Source Capacitance ($C_{S)}$	23 pF
Supply Voltage	1.65 V – 5.5 V
Transition Time	69.5 ns

3.3 Input Low Pass Filter Passive Component Selection

Using Equation **(1)**, the minimum value for C_{FLT} is calculated as 733 pF. C_{FLT} is chosen to be 22 µF to supply enough charge for the increased current when the back-to-back diodes of the SAR ADC driver turn on to reduce the voltage droop on C_{FLT}. The resistor R_{FLT} is chosen to be 10 Ω to stabilize to output of the amplifier and will be discussed in 4.1. The bandwidth of the input to the multiplexer is calculated to be 723.43 Hz using Equation **(2)**.

3.4 Multiplexer Input Buffer

The multiplexer input buffer was chosen as the OPA320 for its high bandwidth, low noise, low offset, fast settling, and capacitive load drive capability. Table 4 lists the parameters of the OPA320 relevant to this design.

Table 4: OPA320 Specifications

Parameter	Value
V_{os}(max)	150 µV
Bandwidth	20 MHz
Noise @ 1 kHz	8.5 nV/√Hz
2V Step Settling to 0.0015%	0.5 µs
Supply Voltage	1.8V – 5.5V

3.5 SAR ADC Driver

As discussed in Section 2.4, the amplifier that drives the SAR ADC must have low THD, low noise, high slew rate, fast settling, and high bandwidth. Therefore, the OPA625 was chosen as the SAR ADC driver. Table 5 lists the parameters of the OPA625 relevant to this design.

Table 5: OPA625 Specifications

Parameter	Value
THD @ 10 kHz	-135 dB
Noise @ 10kHz	2.5 nV/√Hz
Slew Rate	115 V/µs
16-bit Settling with 4 V Step	280 ns
Gain Bandwidth (G=100)	120 MHz
Supply Voltage	2.7 V – 5.5 V

3.6 SAR ADC Driver Gain Network

The components, R_f and R_g, in the gain network of the OPA625 are chosen as 5 kΩ to limit the current through the back-to-back diodes to 520 µA, using Equation **(7)**. Setting $R_f = R_g$ also sets the amplifier in a gain of 2 V/V, resulting in a full scale step of 4 V on the output of the OPA625. The component C_f is chosen to be 1 pF to increase the phase margin of the OPA625.

3.7 Anti-Aliasing Filter

As recommended by the ADS8860 datasheet, the capacitor in the anti-aliasing filter must be greater than 590 pF and should be a C0G or NP0 type capacitor. The resistor must be less than 22 Ω. The capacitor for this design was chosen to be a 1.2 nF C0G capacitor and the resistor was chosen as 12 Ω which will be discussed in 4.2.

3.8 Total Calculated Settling Time

The total settling time calculation is shown below using Equation **(5)**.

$$t_{System} = \sqrt{t_{Multiplexer}^{\ 2} + t_{OPA}^{\ 2} + t_{ADC\_Driver}^{\ 2} + t_{Filter\_ADC}^{\ 2}}$$

$$t_{System} = \sqrt{69.5ns^2 + 500ns^2 + 280ns^2 + 28.8ns^2} = 578ns$$

However, since the output of the OPA320 is not a 2 V step, the settling time is expected to be less than what is calculated.

3.9 Noise Analysis

Using the process shown in 2.6, the total noise of the input driver circuitry is calculated to be 61.746 µVrms and the total noise of the system is calculated to be 71.28 µVrms. For a full noise analysis, please see Appendix B.

3.10 Reference Driver Amplifier and Passive Component Selection

The amplifiers for the reference driver circuitry were chosen to be the OPA333 for its low drift and high dc precision and the THS4281 for its high bandwidth and low output impedance. For more details about designing the reference driver circuitry, refer to TIPD115.

4 Simulation

4.1 Multiplexer Input Buffer Stability

Driving a capacitive load can cause the amplifier to become unstable and oscillate due to the degraded phase margin; therefore, the stability must be checked in simulation. Figure 8 and Figure 9 shows the circuit used to check the phase margin of the multiplexer input buffer and the phase margin measurement using TINA-TI™. The simulation shows a phase margin of 87°.

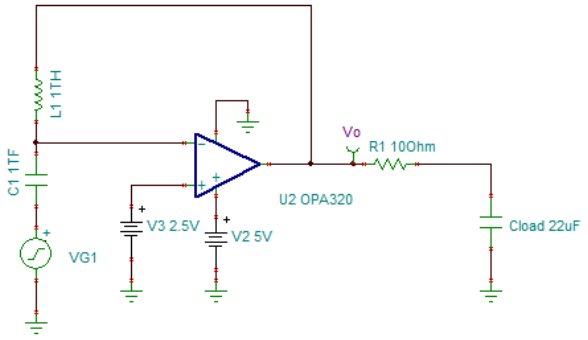


Figure 8: Multiplexer Input Buffer Stability Simulation Circuit

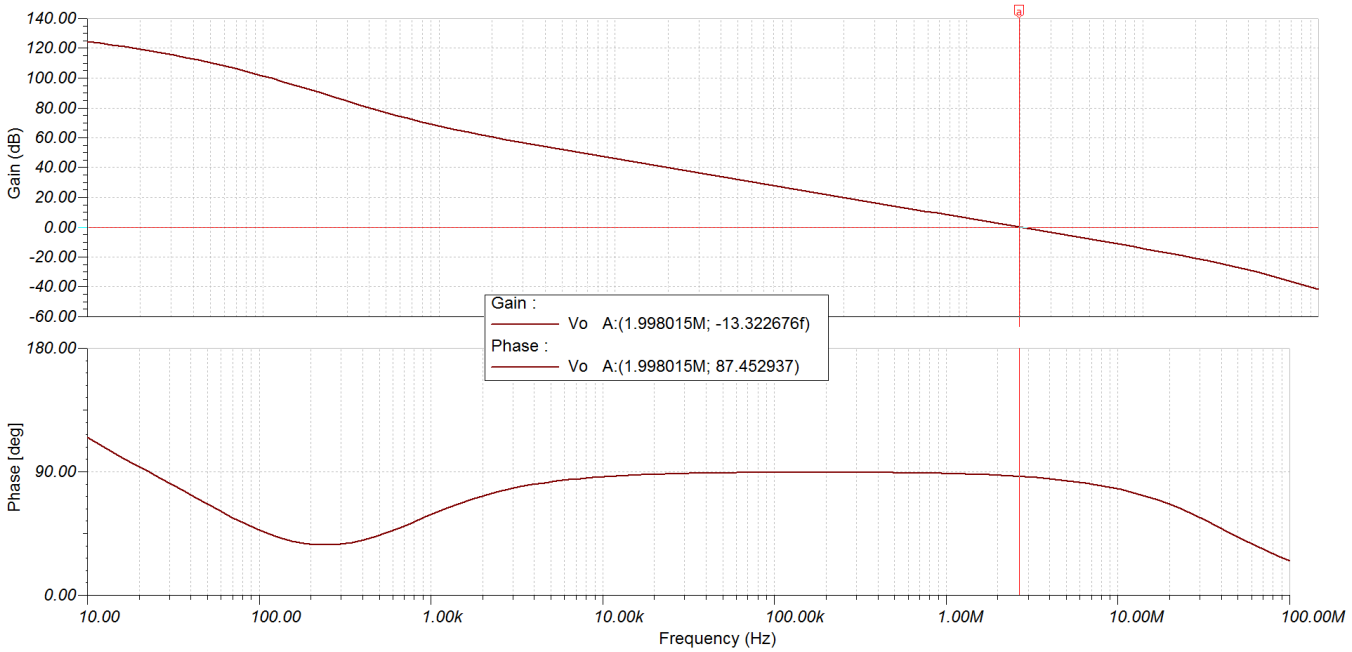


Figure 9: Phase Margin Simulation Result of Multiplexer Input Buffer

4.2 SAR ADC Driver Stability

Figure 10 shows the circuit used to simulate the phase margin of the SAR ADC driver. The simulated phase margin of the SAR ADC driver is 54° as shown in Figure 11.

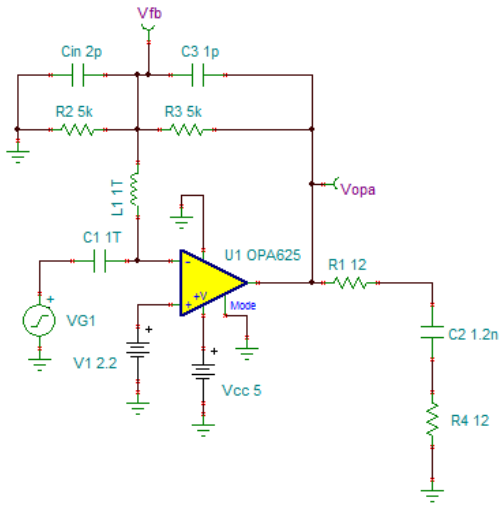


Figure 10: SAR ADC Driver Stability Simulation Circuit

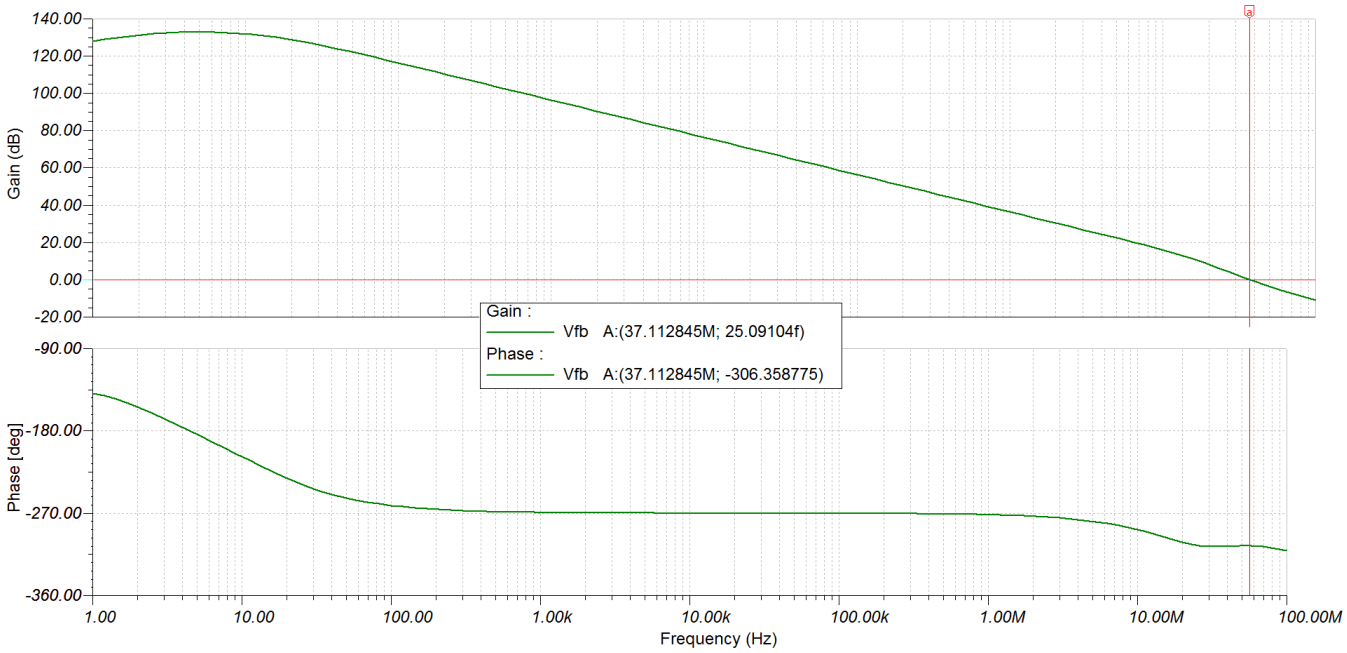


Figure 11: Phase Margin Simulation Result of SAR ADC Driver

4.3 System Settling Time

The system settling time can be simulated using the circuit shown in Figure 12. Since the differential input clamp diodes of an amplifier are not modeled, two diodes have been added across the input of the OPA625. The switch on resistance is set to 1 Ω and a capacitor of 84 pF is added to simulate the effects of the multiplexer. The simulation shows that the system settles in 341 ns as shown in Figure 13.

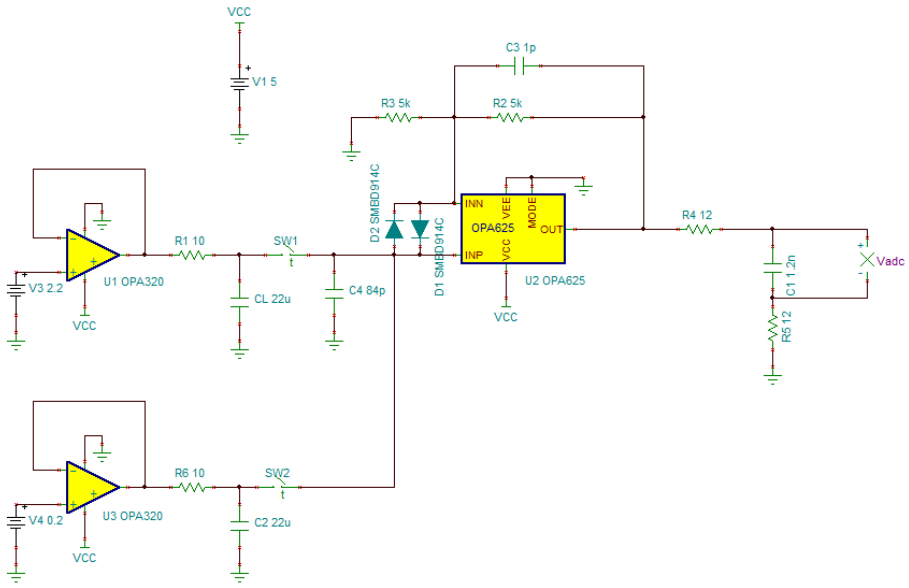


Figure 12: System Settling Time Simulation Circuit

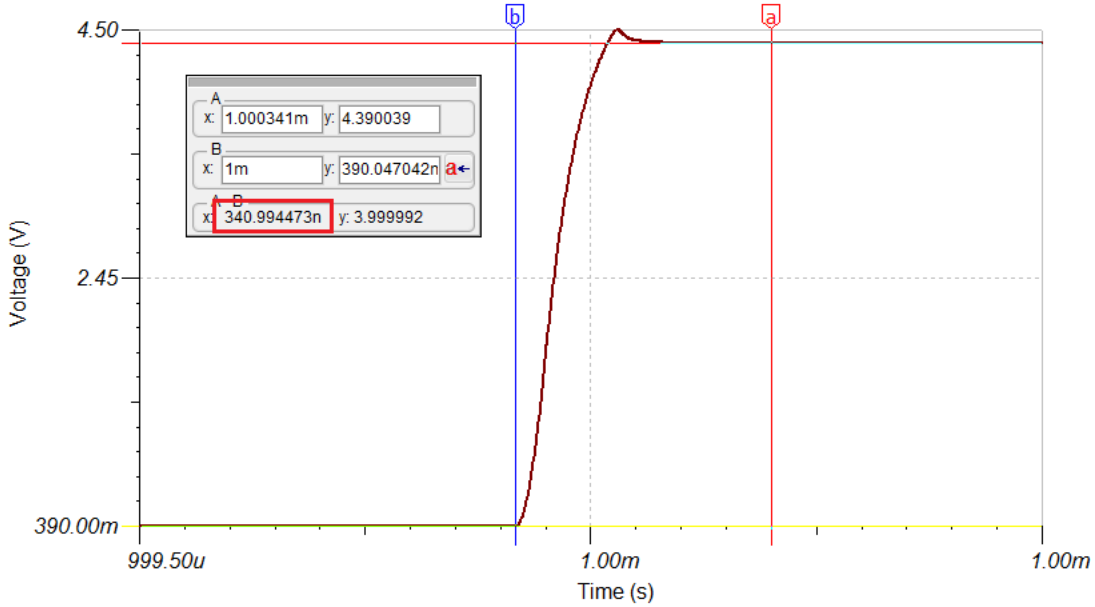


Figure 13: System Settling Time Simulation Measurement

4.4 Noise Analysis

The noise of the input drive circuitry is simulated using the circuit shown in Figure 14. The simulated noise of the input drive circuitry is 45.68 µVrms as shown in Figure 15.

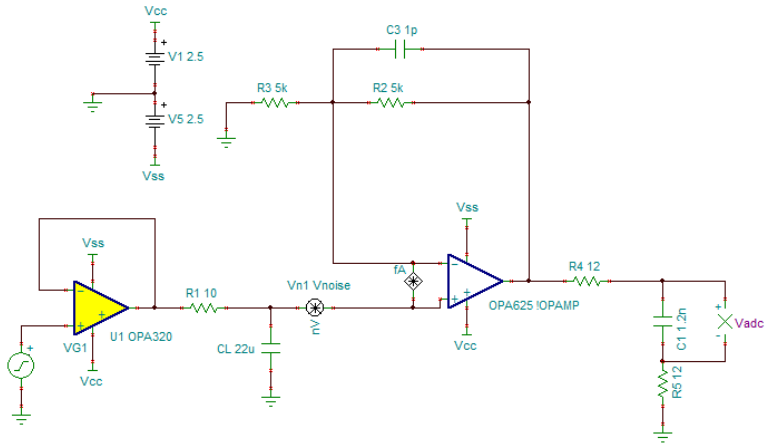


Figure 14: System Noise Simulation Circuit

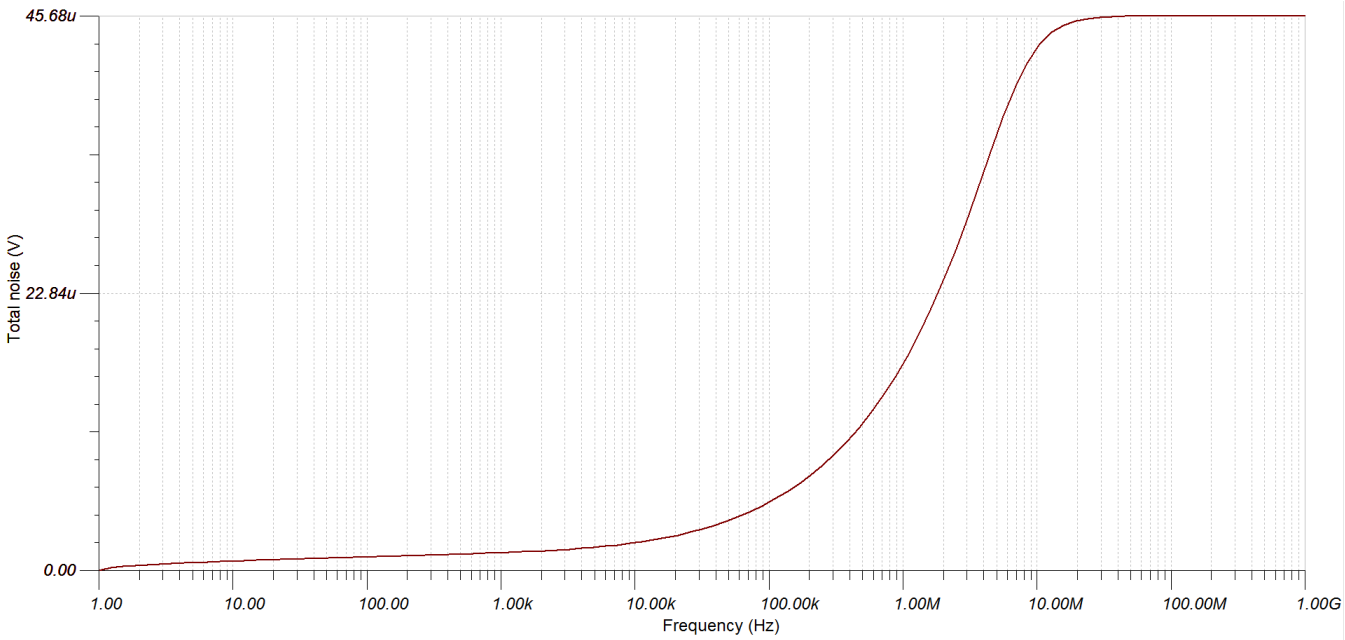


Figure 15: System Noise Simulation Measurement

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB shown in Figure 16 is composed of four layers with signals were routed on the top and bottom layers while power and ground layers were in the middle layers. Basic good layout techniques were used in this design such as keeping traces as short as possible and placing decoupling capacitors close to the pin of the device. Special attention was given to the layout of the reference driver. The reference driver circuitry was placed as close to the ADC reference pin to minimize trace inductance and potential issues with settling of the reference voltage.

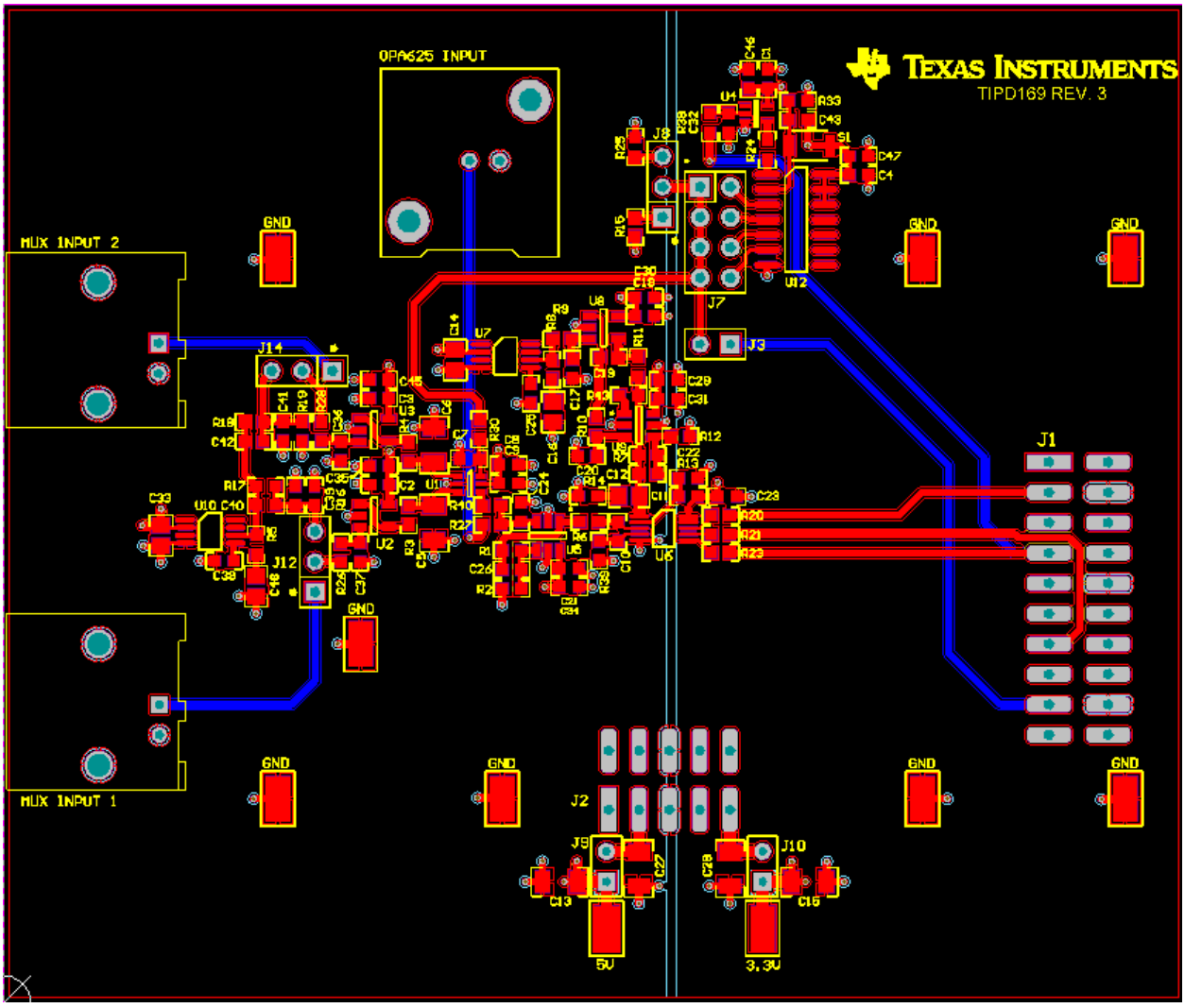


Figure 16: PCB Layout

6 Verification & Measured Performance

6.1 Settling Time Measurement

Figure 17 and Figure 18 show the settling time of the rising and falling edge, respectively. Each data point taken is an average of 1000 points to average out the noise. The rising and falling edge settles within the desired error band in 390 ns and 360 ns respectively.

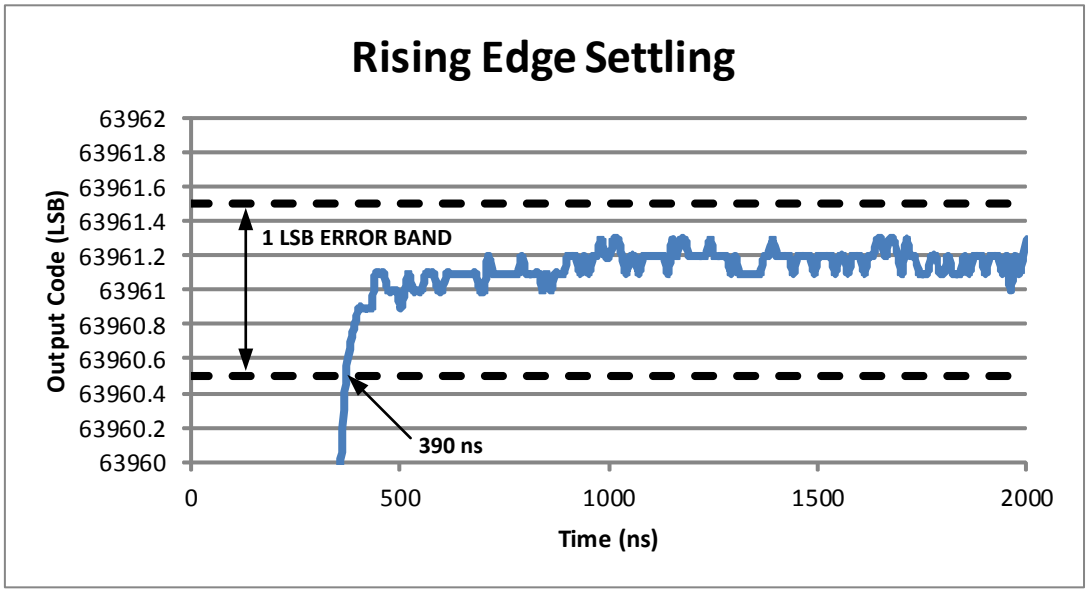


Figure 17: Rising Edge Settling Time Measurement

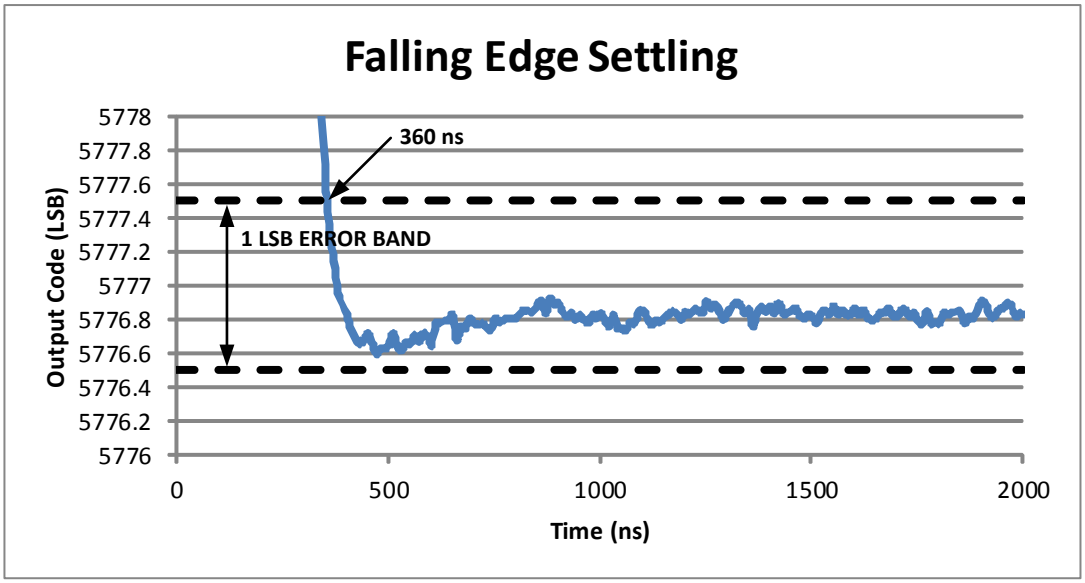


Figure 18: Falling Edge Settling Time Measurement

6.2 AC Performance

The ac performance of the system is determined by measuring the SNR and THD. Figure 19 shows an Fast-Fourier Transform (FFT) of the system with a full-scale 10 kHz sine wave input to the SAR ADC driver. The system performance has an SNR of 83.51 dB and a THD of -102.99 dB. The ENOB of the system is calculated as 13.57 bits.

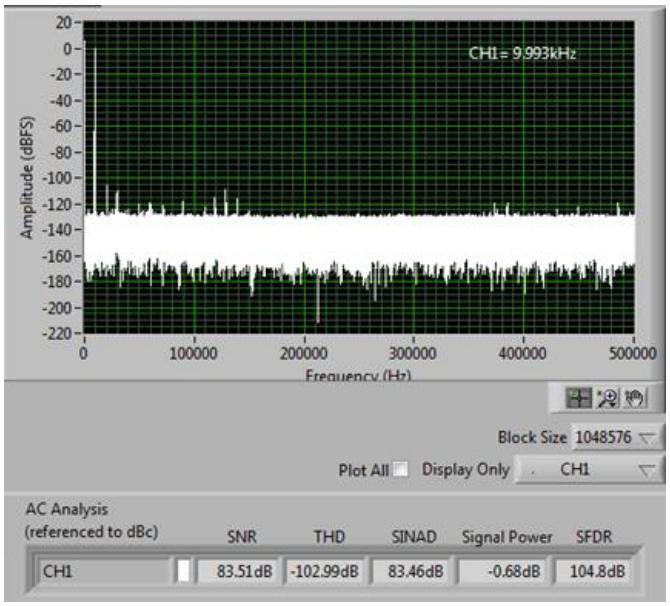


Figure 19: AC Performance of the System

6.3 DC Performance

The dc performance of the system is determined by measuring the effective resolution. Figure 19 shows the dc performance of the system. The measurement was taken with a dc input to the OPA625. The voltage input to the OPA625 was 1/4th the voltage of the reference voltage of the ADC. This set the output of the OPA625 to be mid-scale of the ADC. Figure 20 shows the effective resolution as 15.72 bits.

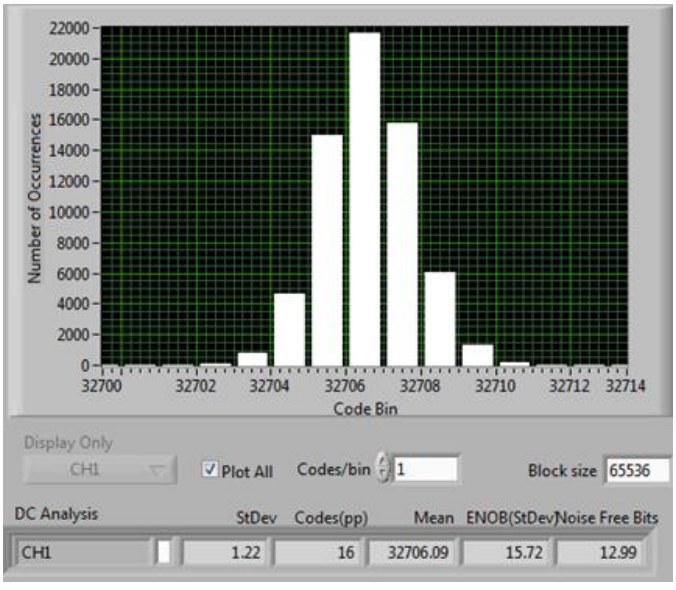


Figure 20: DC Performance of the System

7 Modifications

To improve the ac performance of the system, the gain network resistors, R_f and R_g, can be reduced to reduce the overall noise of the system. This will improve the SNR of the system, which gives a higher ENOB and effective resolution. Due to the decrease in resistors, the current through the differential input clamp diodes of the SAR ADC driver will increase which results in a larger voltage droop on C_{FLT}. Table 6 shows the system performance using 3.48 kΩ resistors in the gain network.

Table 6: System Performance with Modifications

	Measured
Settling Time	1330 ns
Effective Resolution	16-bits
Signal-to-Noise Ration$_{SYS}$(SNR$_{SYS}$)	88.03 dB
Total Harmonic Distortion$_{SYS}$(THD$_{SYS}$)	-106.45 dB
Effective Number of Bits$_{SYS}$(ENOB$_{SYS}$)	14.33 bits

8 About the Author

Timothy Claycomb is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He earned his B.S. in Electrical Engineering from Michigan State University in 2013.

Alice Mun is a field applications engineer based in Korea. Before working as a field applications engineer, she performed a six-month rotation with the Precision Linear group in Tucson, Arizona. She received her BSEE from Kyung-Hee University where she majored in biomedical engineering and electronics engineering.

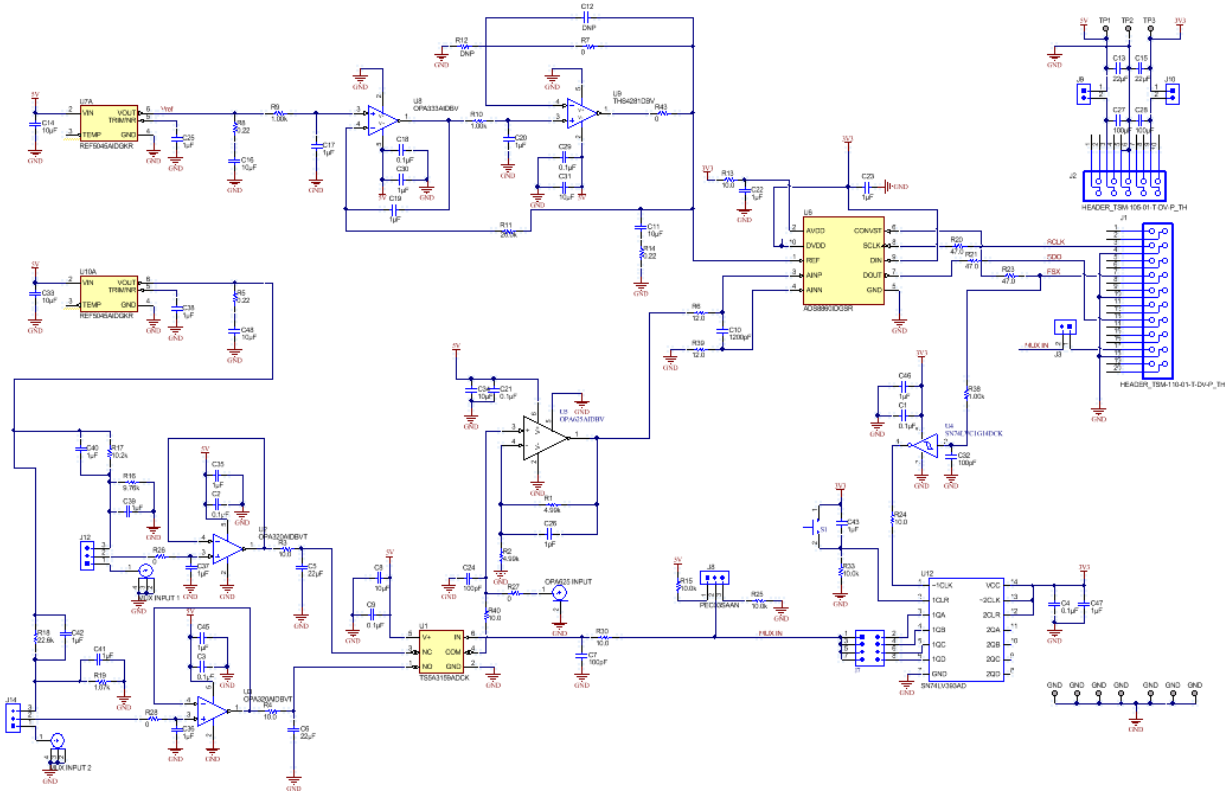
9 Acknowledgements & References

1. *A. Kay, Operational Amplifier Noise: Techniques and Tips for Analyzing and Reducing Noise. Elsevier, 2012.*
2. *16-Bit 1MSPS Data Acquisition Reference Design for Single-Ended Multiplexed Applications (TIDU504)*
3. *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise (SLAU515)*
4. *16-Bit, 100KSPS, 4-Channel Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion (TIDU181)*

The authors would like to thank Collin Wells and Rafael Ordonez for their technical contributions during this design.

Appendix A.

A.1 Electrical Schematic



A.2 Bill of Materials

Quantity	Designator	Value	Description	Manufacturer	PartNumber
8	C1, C2, C3, C4, C9, C18, C21, C29	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Kemet	C0603X104K3RACTU
2	C5, C6	22uF	CAP, CERM, 22 µF, 10 V, +/- 10%, X7R, 1206	MuRata	GRM31CR71A226KE15L
3	C7, C24, C32	100pF	CAP, CERM, 100pF, 50V, +/-1%, C0G/NP0, 0603	AVX	06035A101FAT2A
3	C8, C31, C34	10uF	CAP, CERM, 10 µF, 25 V, +/- 20%, X5R, 0603	TDK	C1608X5R1E106M080AC
1	C10	1200pF	CAP, CERM, 1200 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H122JA01D
5	C11, C14, C16, C33, C48	10uF	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	MuRata	GRM21BR71A106KE51L
0	C12	DNP	CAP, CERM, 4.7 pF, 50 V, +/- 5%, C0G/NP0, 0603	AVX	06035A4R7CAT2A
2	C13, C15	22uF	CAP, CERM, 22 µF, 16 V, +/- 20%, X5R, 1206	AVX	1206YD226MAT2A
19	C17, C19, C20, C22, C23, C25, C30, C35, C36, C37, C38, C39, C40, C41, C42, C43, C45, C46, C47	1uF	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D
1	C26	1pF	CAP, CERM, 1 pF, 50 V, +/- 25%, C0G/NP0, 0603	AVX	06035A1R0CAT2A
2	C27, C28	100uF	CAP, CERM, 100 µF, 6.3 V, +/- 20%, X5R, 1206	MuRata	GRM31CR60J107ME39L
1	J1 (Top)		Header 20 Pin SMT Plug, .100" Gold (2x10)	Samtec	TSM-110-01-L-DV-P
	J1 (Bottom)		Header 20 Pin SMT Socket, .100" Gold (2x10)	Samtec	SSW-110-22-F-D-VS-K
1	J2 (Top)		Header 10 Pin SMT Plug, .100" Gold (2x5)	Samtec	TSM-105-01-L-DV-P
	J2 (Bottom)		Header 10 Pin SMT Socket, .100" Gold (2x5)	Samtec	SSW-105-22-F-D-VS-K
3	J3, J9, J10		Header, 100mil, 2x1, TH	Mill-Max	800-10-002-10-001000
1	J7		Header, 100mil, 4x2, Gold, TH	Samtec	TSW-104-07-G-D
3	J8, J12, J14		Header, 100mil, 3x1, Tin, TH	Sullins Connector Solutions	PEC03SAAN
1	J13		BNC female, 50 ohm, std profile, white	TE Connectivity	1-1337543-0
1	J15		BNC female, 50 ohm, std profile, white	TE Connectivity	1-1337543-0
1	J16		Conn Socket BNC straight 50 ohm PCB mount	AMP	1-1634505-0
2	R1, R2	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-4991-B-T5
0	R12	DNP	RES, 511, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603511RFKEA
4	R3, R4, R13, R40	10.0	RES, 10.0 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0710RL
3	R5, R8, R14	0.22	RES, 0.22 ohm, 1%, 0.1W, 0603	Panasonic	ERJ-3RQFR22V
2	R6, R39	12.0	RES, 12.0, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0712RL
1	R7	249	RES, 249, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603249RFKEA
2	R9, R10	1.00k	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA
1	R11	20.0k	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA
3	R15, R25, R33	10.0k	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0710KL
1	R16	9.76k	RES, 9.76 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-9761-B-T5
1	R17	10.2k	RES, 10.2 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-1022-B-T5
1	R18	22.6k	RES, 22.9k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0722K9L
1	R19	1.07k	RES, 1.07 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-1071-B-T5
3	R20, R21, R23	47.0	RES, 47.0, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-470-B-T5
2	R24, R30	10.0	RES, 10.0, 0.1%, 0.1 W, 0603	Vishay-Dale	TNPW060310R0BEEA
4	R26, R27, R28, R43	0	RES, 0 ohm, 5%, 0.1W, 0603	Yageo America	RC0603JR-070RL
1	R38	1.00k	RES, 1.00k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-102-B-T5
1	S1		SWITCH TACTILE SPST-NO 0.05A 12V	Omron Electronic Components	B3U-1000P
1	U1		SINGLE-CHANNEL 2:1 MULTIPLEXER	Texas Instruments	TS5A3159ADCK
2	U2, U3		Precision, 20 MHz, RRIO, CMOS Operational Amplifier	Texas Instruments	OPA320AIDBVT
1	U4		IC, Single Schmitt-Trigger Inverter	Texas Instruments	SN74LVC1G14DCK
1	U5		High Bandwidth, High-Precision, Low THD+N, 16-Bit ADC Driver	Texas Instruments	OPA625IDBVR
1	U6		16-Bit, 1-MSPS, Single-Ended Input, SAR Analog-to-Digital Converter	Texas Instruments	ADS8860IDGSR
2	U7, U10		Low Noise, Very Low Drift, Precision Voltage Reference	Texas Instruments	REF5045AIDGKR
1	U8		1.8-V, microPower, CMOS Operational Amplifiers, Zero-Drift Series	Texas Instruments	OPA333AIDBV
1	U9		VERY LOW-POWER, HIGH-SPEED, OPERATIONAL AMPLIFIER	Texas Instruments	THS4281IDBV
1	U12		IC, Dual 4 bit binary Counters	Texas Instruments	SN74LV393AD

Figure A-2: Bill of Materials

Appendix B.

B.1 Noise Calculations

$$BW_{n\_OPA320} = 1.357kHz$$

$$e_{n\_bb\_OPA320} = 235.901nVrms$$

$$e_{n\_normalized\_OPA320} = 173.93nV$$

$$e_{n\_1/f\_OPA320} = 823.1nVrms$$

$$e_{n\_Total\_OPA320} = 856.23nVrms$$

$$BW_{n\_OPA625} = 8.676MHz$$

$$e_{n\_bb\_OPA625} = 7.363\mu Vrms$$

$$e_{n\_normalized\_OPA625} = 31.6nV$$

$$e_{n\_\_1/f\_OPA625} = 135.198nVrms$$

$$e_{n\_I} = 7\frac{nV}{\sqrt{Hz}}$$

$$E_{n\_I} = 20.618\mu Vrms$$

$$e_{n\_R} = 21.75\mu Vrms$$

$$e_{n\_Total\_OPA625} = 30.873\mu Vrms$$

$$e_{n\_Total\_Out} = 61.746\mu Vrms$$

$$e_{n\_ADC\_RMS} = 35.61\mu Vrms$$

$$e_{n\_Total\_System} = 71.28\mu Vrms$$

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