3.6V – 6V VIN

J1
1
2

VIN

C2
1uF

J2
1
2
GND

U1
TPS71701DCK
1 IN   OUT 5
2 GND
3 EN   NR/FB 4

R1
162K

R2
324K

1.2V_RTC
1.2V @ 60mA

C1
1uF

SYNC

U2
TPS62353YZG
C2 EN   SYNC B2
D2 VSEL   SW   A2
A3 PVIN   FB   D1
B3 AVIN   AGND C1
C3 SDA   PGND B1
D3 SCL   PGND A1

R3
1M

L1
1uH

1.2V
1.2V @ 600mA

C3
10uF

J4
1
2
3
4
5   GND
6
7
8   SCL
9
10
SDA

C4
10uF

C5
47uF

R4
10k

R5
10k

U3
TPS62200DBV
1 VIN   SW 5
2 GND
3 EN   FB 4

L2
10uH
1   2

3.3V
3.3V @ 165mA

C6
4.7uF

R6
562k

C7
27pF

R8
100k

C9
180pF

C8
22uF

R7
100k

U4
TPS3808G12
6 VDD   RST 1
5 SNS/NC GND 2
4 CT   MR 3

1.2V

1.2V Detect from
TPS 62353

C10
100pF
/1\

1.2V Power Good

1.2V_PGD

3.3V

3.3 VIN from
TPS 62200

C11
1uF

U5
TPS73218DBV
1 IN   OUT 5
2 GND
3 EN   NR 4

1.8V
1.8V @ 50mA

C12
1uF

C13
0.01uF

/1\ The TPS3808G12 supply voltage supervisor has been used to monitor the 1.2–V rail.
The threshold voltage for this device is 1.12–V, which is outside the published
tolerance for the OMAP–L137 1.2–V rail (5%). This has been deemed acceptable for
those customers who wish to avoid unnecessary system resets due to short–term
transient events. Alternatively, the TPS3808G125 supervisor may be substituted
for the δG12δ; the threshold voltage for the δG125δ is 1.16–V, which is closer to
the OMAP–L137 (–5%) limit of 1.164–V

Title	TSP 71710, TPS62353. TPS62200, TPS73218	
Size B	Number PMP4080	Rev B
Date	02/15/2010	Drawn by T. Olabumuyi
Filename PMP4080_REVB.SCH	Sheet	of

Filename: PMP4080_REVB_bom.xls
Date: 02/15/2010

PMP4080_REVB BOM

COUNT	RefDes	Value	Description	Size	Part Number	Mfr	Area
4	C1, C2, C11, C12	1uF	Capacitor, Ceramic, 6.3V, X5R, +/-15%	0603	Std	Std	
1	C10	100pF	Capacitor, Ceramic, 100-pF, 50-V, C0G, 10%	0603	C1608C0G1H101J	TDK	
1	C13	0.01uF	Capacitor, Ceramic, 6.3V, X5R, +/-15%	0603	Std	Std	
2	C3, C4	10uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J106KT	TDK	
1	C5	47uF	Capacitor, Ceramic, 10V, X5R, 20%	1812	C4532X5R1A476M	TDK	
1	C6	4.7uF	Capacitor, Ceramic, 4.7-uF, 6.3-V, X5R, 20%	0805	Std	TDK	
1	C7	27pF	Capacitor, Ceramic, 27pF, 50-V, X7R, 5%	0603	Std	Std	
1	C8	22uF	Capacitor, Ceramic, 22-uF, 6.3-V, X5R, 20%	0805	C2012X5R0J226M	TDK	
1	C9	180pF	Capacitor, Ceramic, 180pF, 50-V, COG, 5%	0603	Std	Std	
2	J1, J2	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN		
1	J4	2510-6002UB	Connector, Male Straight 2x10 pin, 100mil spacing, 4 Wall	0.338 x 0.788	2510-6002UB	3M	
1	L1	1uH	Inductor, SMT, 1.6A, ±30%	0.118 x 0.118	LPS3010-102NLC	Coilcraft	
1	L2	10uH	Inductor, SMT, 1840mA, 85-milliohm	0.250 x 0.250 in	MSS6132-103MLB	Coilcraft	
1	R1	162k	Resistor, Chip, 162K, 1/16W, 1%	0603	Std	Std	
1	R2	324k	Resistor, Chip, 324K, 1/16W, 1%	0603	Std	Std	
1	R3	1M	Resistor, Chip, 1/16W, 1%	0603	Std	Std	
2	R4, R5	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	
1	R6	562k	Resistor, Chip,562k-Ohms, 1/16-W, 1%	0603	Std	Std	
1	R7	100k	Resistor, Chip, 100k-Ohms, 1/16W, 5%	0603	Std	Std	
1	R8	100k	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std	
1	U1	TPS71701DCK	IC, 150mA, Low Iq, Wide Bandwdth, LDO Linear Regulators	SC70	TPS71701DCK	TI	
1	U2	TPS62353YZG	IC, 3MHz Synchronous Step Down Converter with I²C, 800mA	CSP-12	TPS62353YZG	TI	
1	U3	TPS62200DBV	IC, Switching Buck Converter, 1.8-V, 300-mA	SOT23-5	TPS62200DBV	Texas Instruments	
1	U4	TPS3808G12	IC, Low Quiescent Current Programmable, 1.2-V, Delay Time 1ms to10s	SOT23-6	TPS3808G12DBVR	TI	
1	U5	TPS73218DBV	IC, 250mA, Low Iq, Wide Bandwdth, LDO Linear Regulators	SOT23-5	TPS73218DBV	TI	

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS
INSTRUMENTS

TEXAS INSTRUMENTS

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73128
– (PMP4080)
Updated 3/24/2010

The following test report includes measurements for the following output voltage rails using a **5V input**:

This design meets the power sequencing requirements required by OMAP-L137 / C6747 / C6745 / C6743.

Contents
Start Up Waveform

TPS 71701 – LDO (1.2V @ 0.06A)
-output ripple
-load transient response

TPS62353 – DCDC (1.2V @ 0.6A)
-output ripple
-load transient response
-switch node
-efficiency
-load regulation

TPS 62200 – DCDC (3.3V @ 0.165A)
-output ripple
-load transient response
-switch node
-efficiency
-load regulation

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS INSTRUMENTS

START UP WAVEFORM

Ch 1: 1.2V LDO (unloaded);   TPS71701
Ch 2: 1.2V DCDC (unloaded); TPS62353
Ch 3: 3.3V DCDC (unloaded); TPS62200
Ch 4: 1.8V LDO (unloaded); TPS 73218

| 1 | 2 ms 2.00 V | 2 | 2 ms 2.00 V | 3 | 2 ms 2.00 V | 4 | 2 ms 2.00 V | □ | STOPPED |
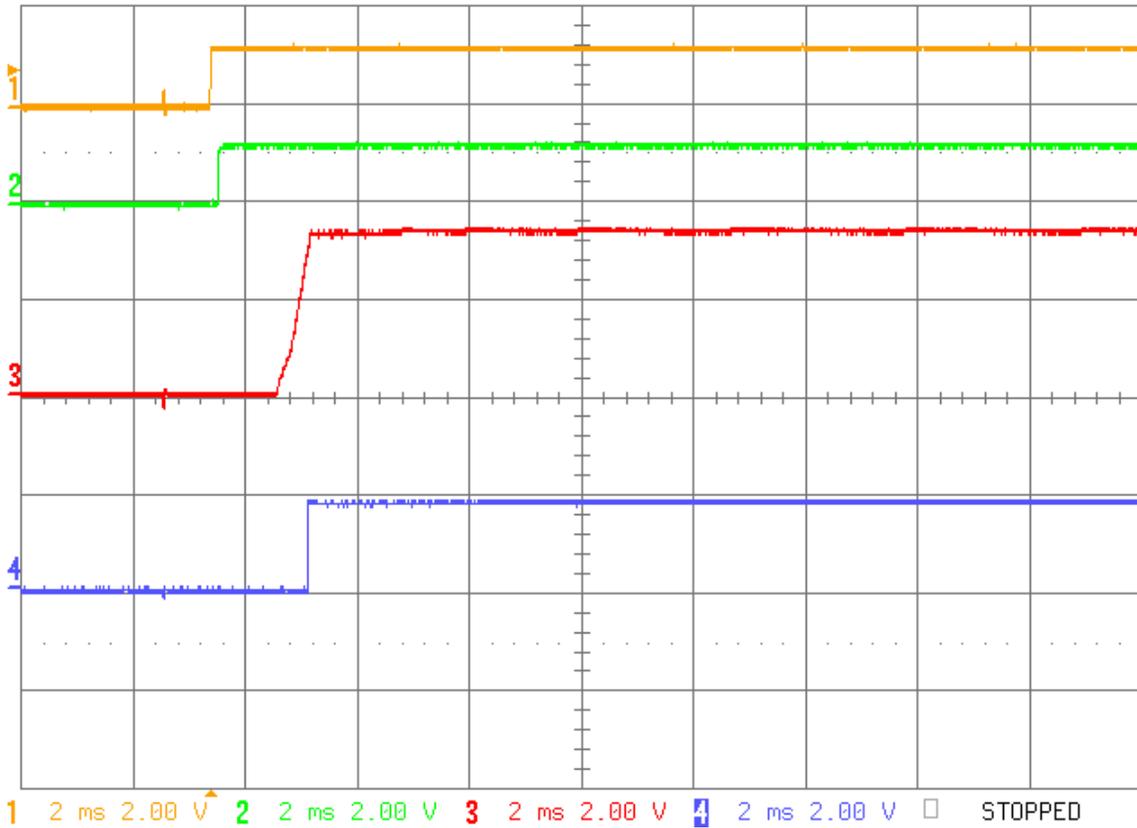
Fig 1: Start Up waveform with outputs unloaded

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS INSTRUMENTS

Ch 1: 1.2V @ 0.06A LDO;   TPS71701
Ch 2: 1.2V @ 0.6A DCDC; TPS62353
Ch 3: 3.3V @ 0.165A DCDC; TPS62200
Ch 4: 1.8V @ 0.05A LDO; TPS73218

| 1 | 2 ms 2.00 V | 2 | 2 ms 2.00 V | 3 | 2 ms 2.00 V | 4 | 2 ms 2.00 V | ☐ STOPPED |
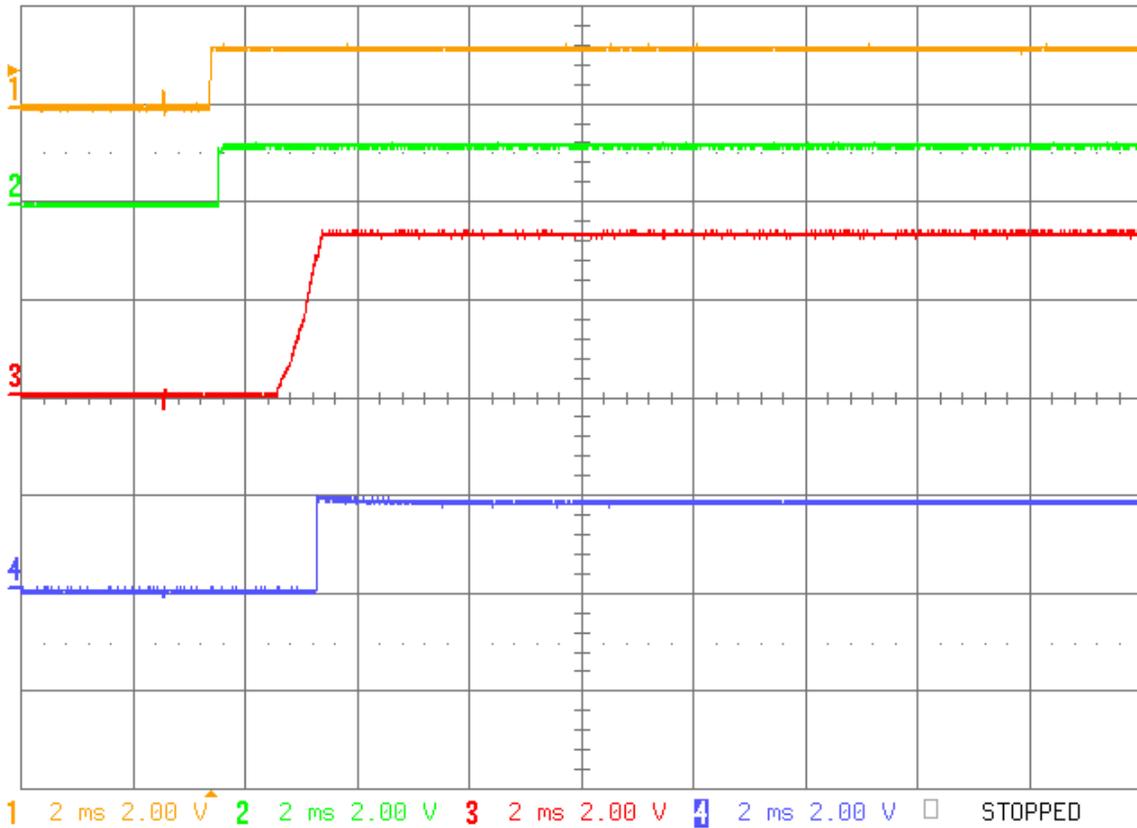
Fig 2: Start Up waveform with outputs fully loaded

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
TPS 71701 – LDO (1.2V @ 0.06A)

OUTPUT RIPPLE (TPS 71701)
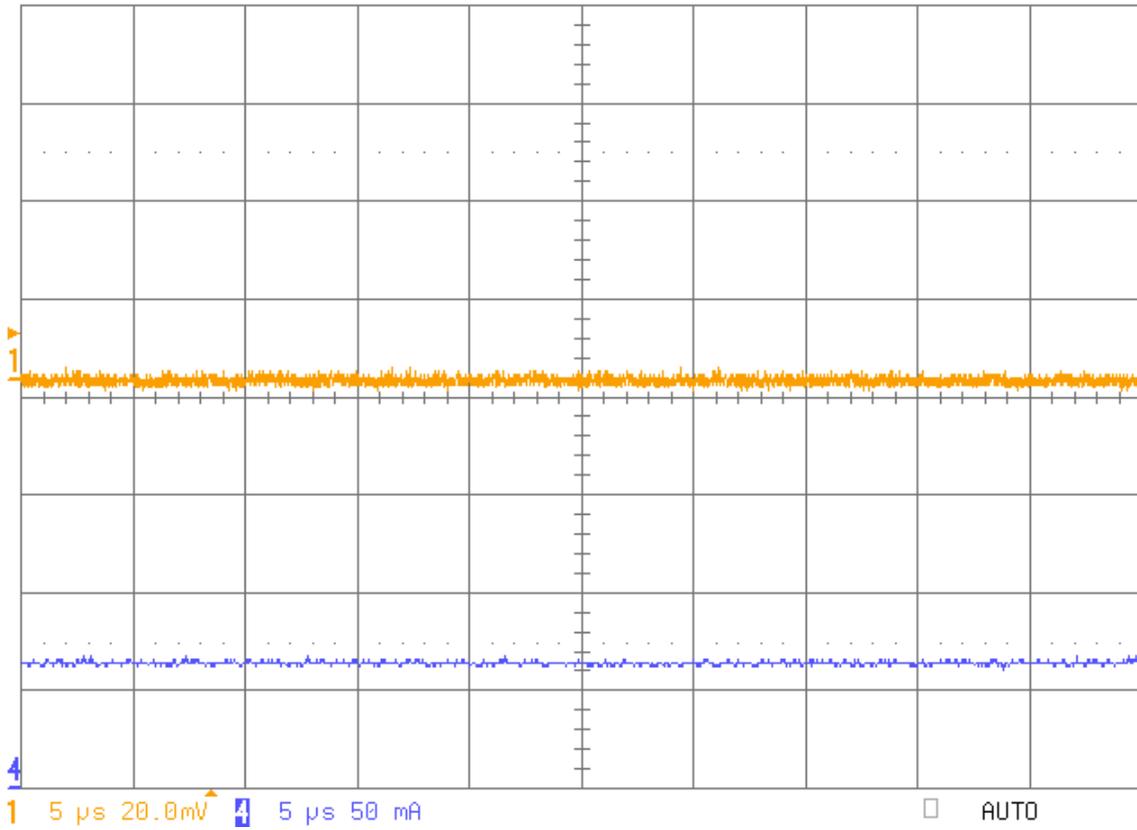
Fig 3: Output Ripple 1.2V @ 0.06A TPS 71701 LDO, 5Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

LOAD TRANSIENT RESPONSE (TPS 71701)

1 50 ms 20.0mV 4 50 ms 50 mA   □ AUTO
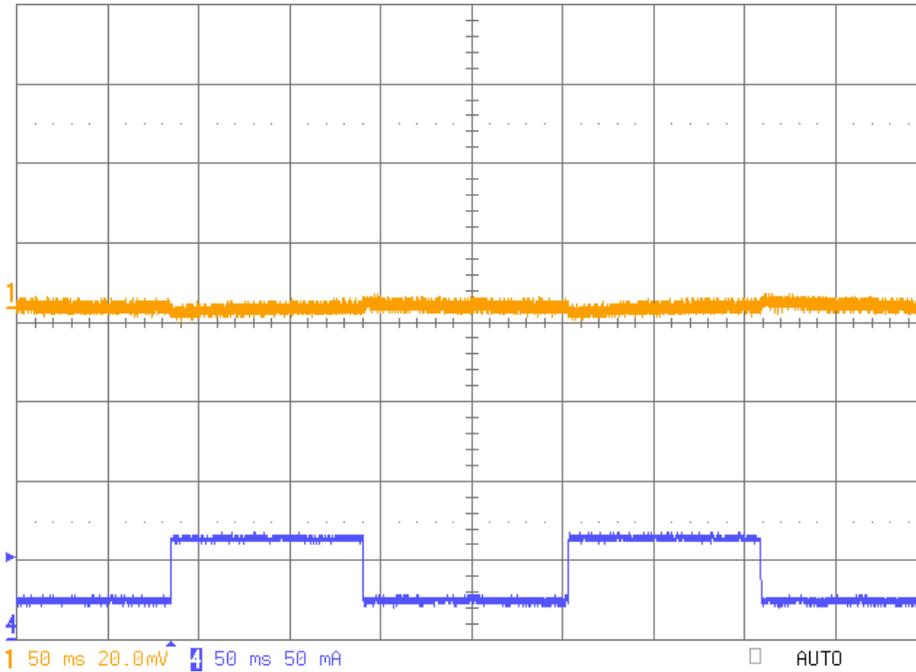
Fig 4: Load transient response on TPS71701, 1.2V output (Ch1) for load step 20mA to 60mA (Ch4 -33% to 100%), at low line 3.6Vin

1 50 ms 20.0mV 4 50 ms 50 mA   □ AUTO
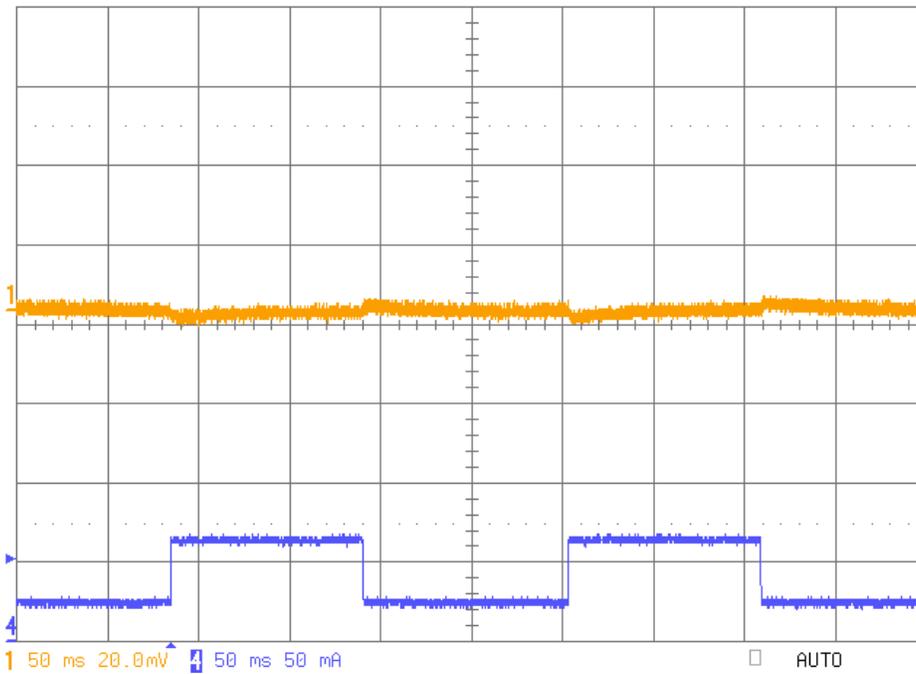
Fig 5: Load transient response on TPS71701, 1.2V output (Ch1) for load step 20mA to 60mA (Ch4 -33% to 100%), at high line 6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TPS 62353 – DCDC (1.2V @ 0.06A)

Set to operate in fixed PWM mode in all test cases with 3 MHz. TPS 6235x in fixed PWM mode gives best load and line response, and reduced ripple at the expense of reduced light load efficiency. This default mode is used in these tests.

Using the I2C interface, the control registers can be configured for fast or light pulse frequency modulation mode to increase efficiency at very light load and to reduce quiescent current. Using the control registers, the TPS 6235x is also reconfigurable for adjustable slew rate of the start up ramp; synchronization with external clock; and for active discharge of output capacitor in shutdown, as well as dynamic voltage scaling between active and sleep mode.

OUTPUT RIPPLE (TPS 62353)

Full load, high line

Fig 6: Output Ripple 1.2V (Ch1) @ 0.6A (Ch4) TPS 62353 DCDC, Highline 6Vin

OMAP-L137 / C6747 / C6745 / C6743
## TPS62353, TPS62200, TPS71701, TPS73218 Test Report

Light load, high line

1   5 μs   20.0mV   4   5 μs   200 mA   AUTO
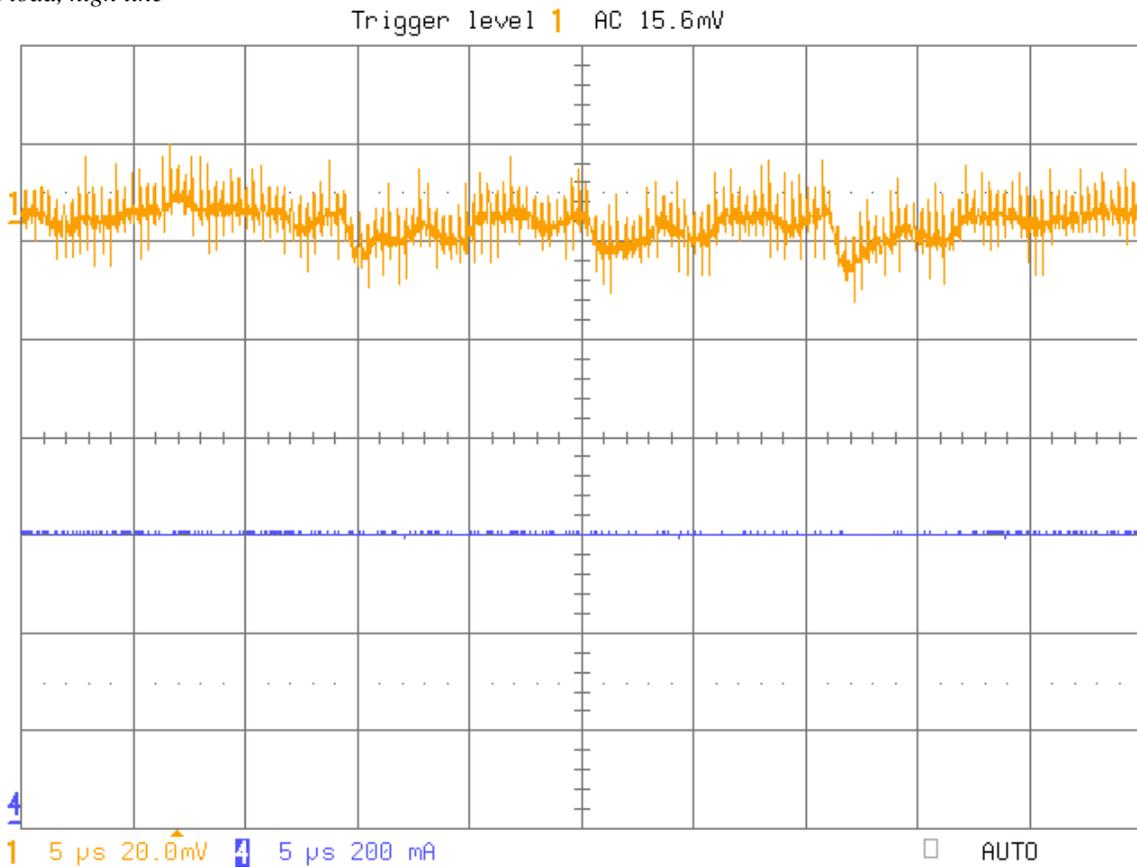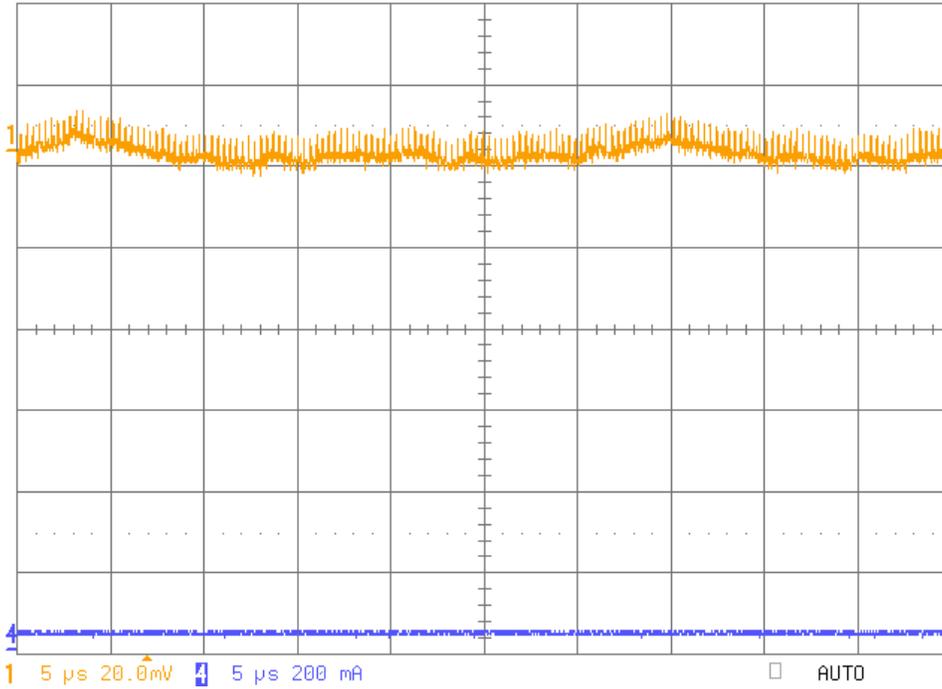
Fig 7: Output Ripple 1.2V (Ch1) @ 0.05A (Ch4) TPS 62353 DCDC, Highline 6Vin

Full load, low line

1   5 μs   20.0mV   4   5 μs   200 mA   AUTO

Fig 8: Output Ripple 1.2V (Ch1) @ 0.6A (Ch4) TPS 62353 DCDC, Lowline 3.6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

Light load, low line

1 5 µs 20.0mV 4 5 µs 200 mA AUTO
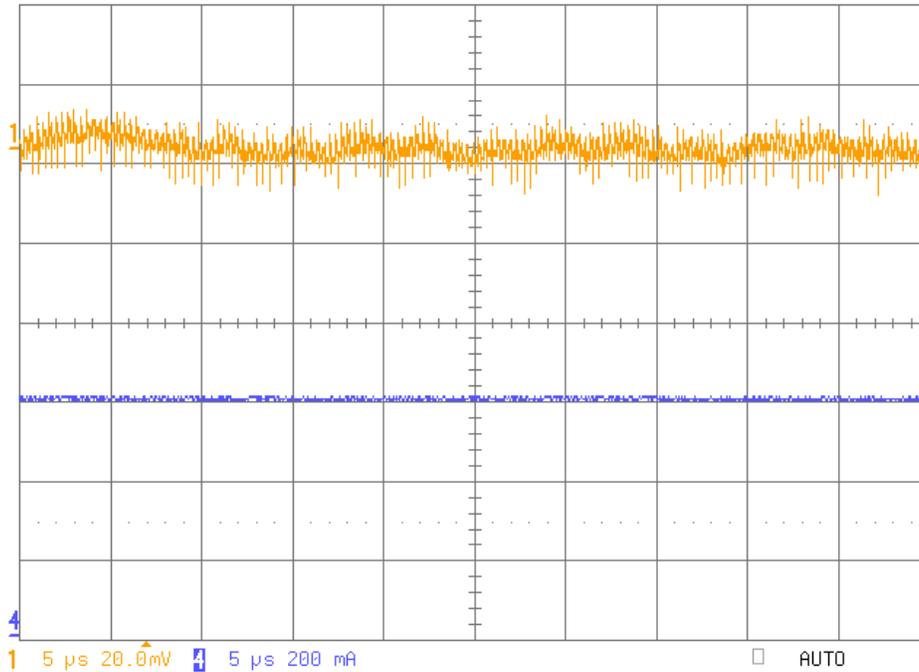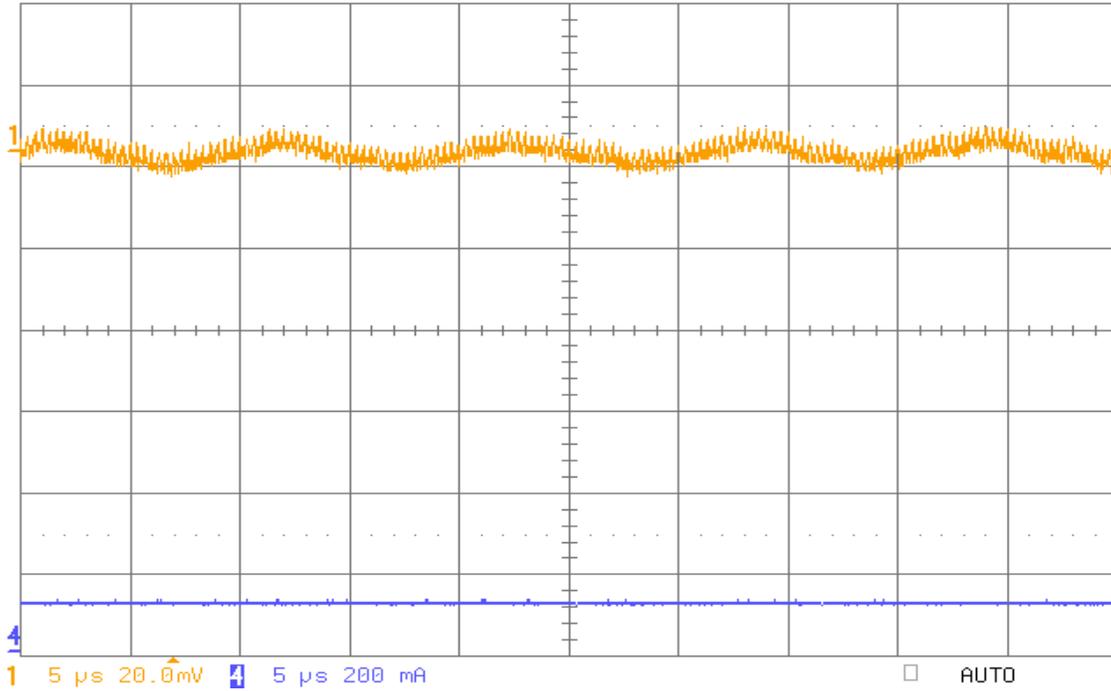
Fig 9: Output Ripple 1.2V (Ch1) @ 0.14A (Ch4) TPS 62353 DCDC, low line 3.6Vin
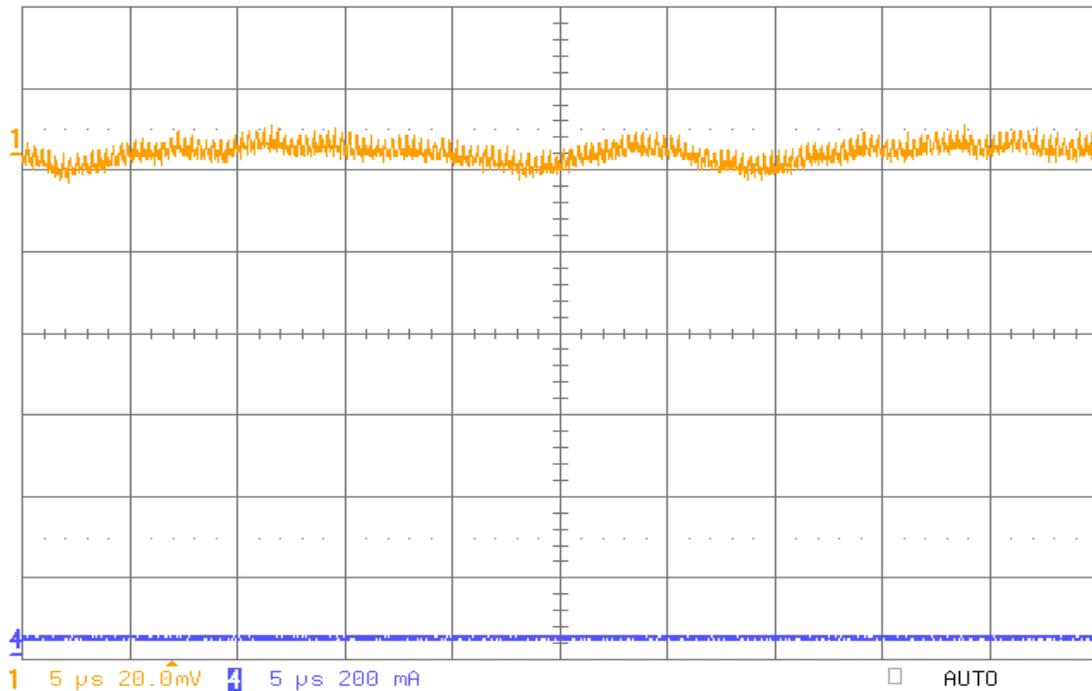
1 5 µs 20.0mV 4 5 µs 200 mA AUTO

Fig 10: Output Ripple 1.2V (Ch1) @ 0.05A (Ch4) TPS 62353 DCDC, low line 3.6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
LOAD TRANSIENT RESPONSE (TPS 62353)
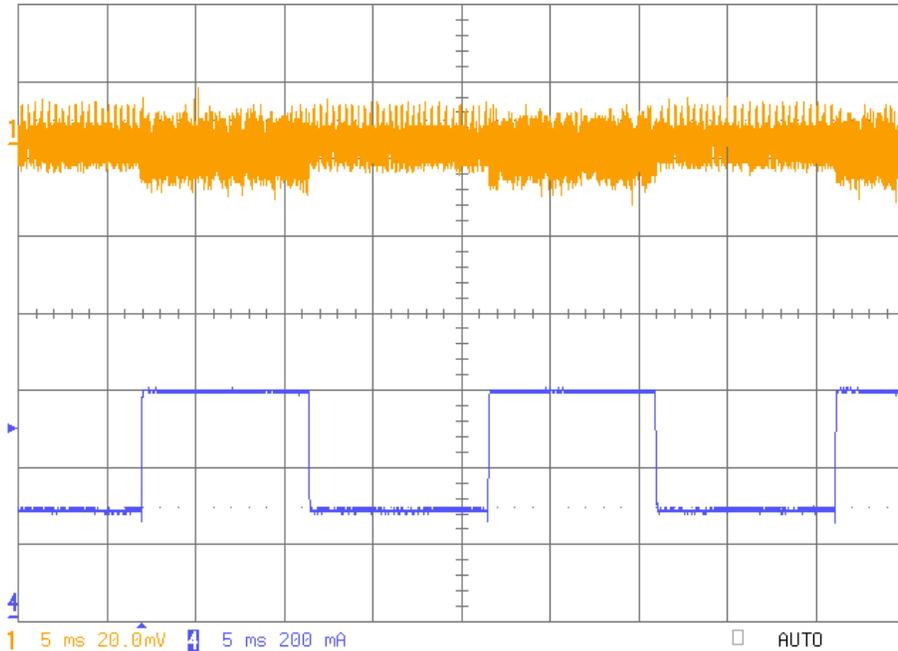
Highline

Fig 11: Load transient response on TPS62353, 1.2V output (Ch1) for load step 300mA to 600mA (Ch4 - 50% to 100%), at high line 6Vin
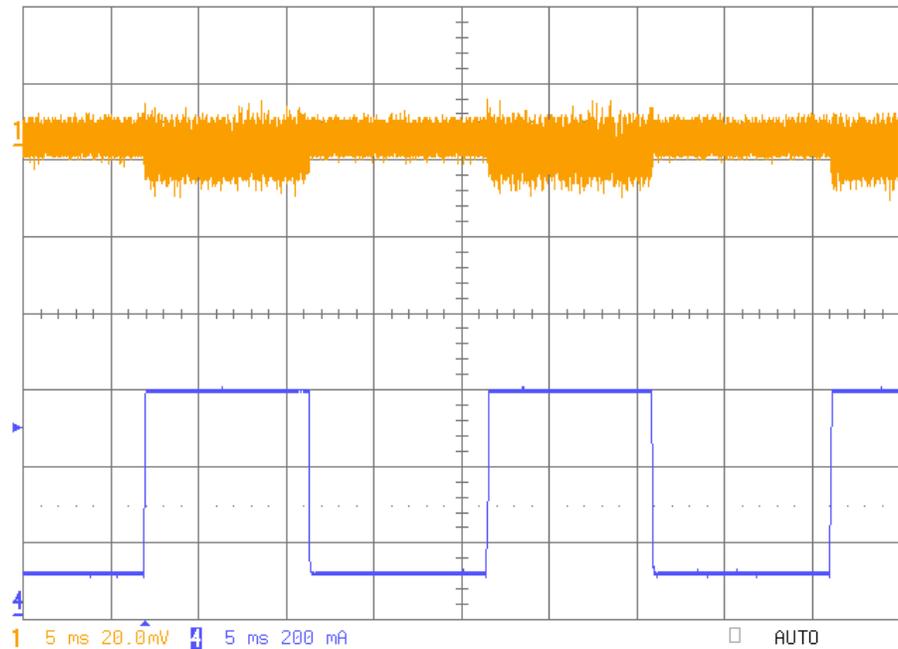
Fig 12: Load transient response on TPS62353, 1.2V output (Ch1) for load step 150mA to 600mA (Ch4 - 25% to 100%), at high line 6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
Low line
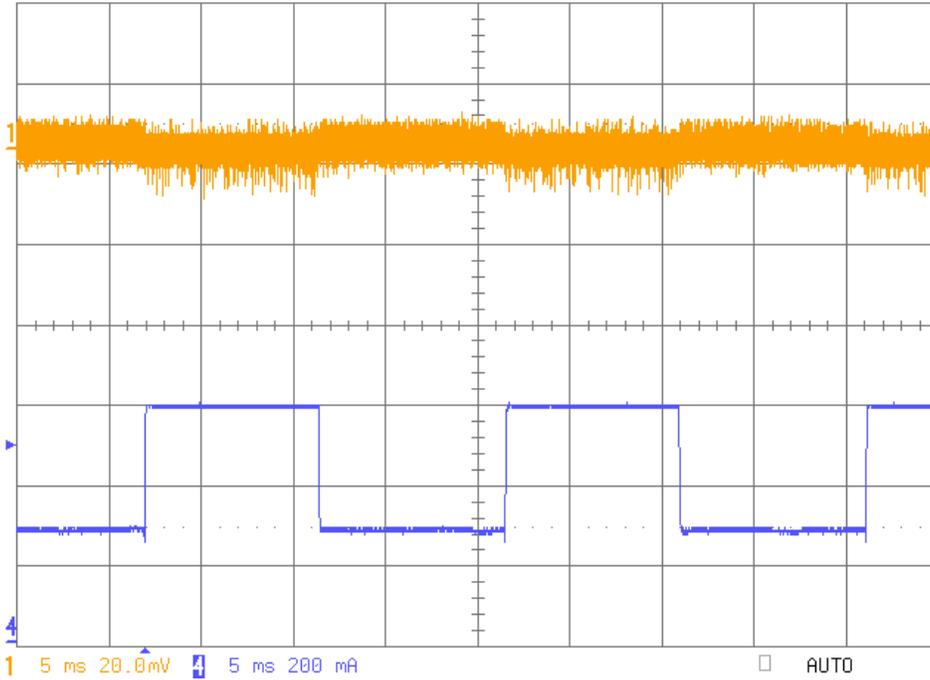
Fig 13: Load transient response on TPS62353, 1.2V output (Ch1) for load step 300mA to 600mA (Ch4 - 50% to 100%), at low line 3.6Vin
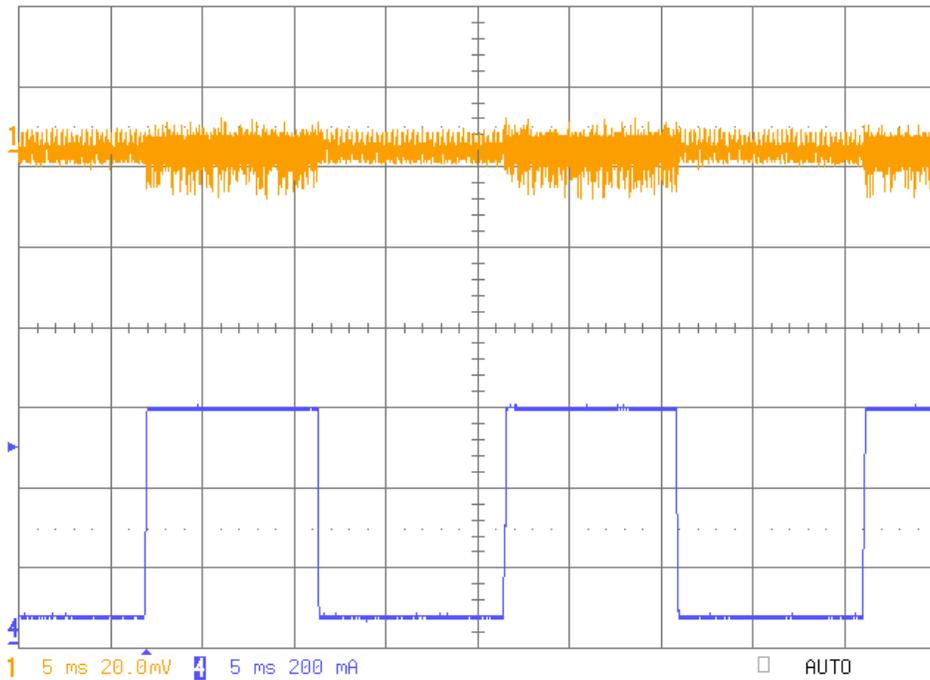
Fig 14: Load transient response on TPS62353, 1.2V output (Ch1) for load step 80mA to 600mA (Ch4 - 15% to 100%), at low line 3.6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
SWITCH NODE (TPS 62353)

TPS62353 exhibits a characteristic duty cycle jitter. It operates in fixed PWM mode.

.1 µs 2.00 V   4 .1 µs 200 mA   ☐ AUTO
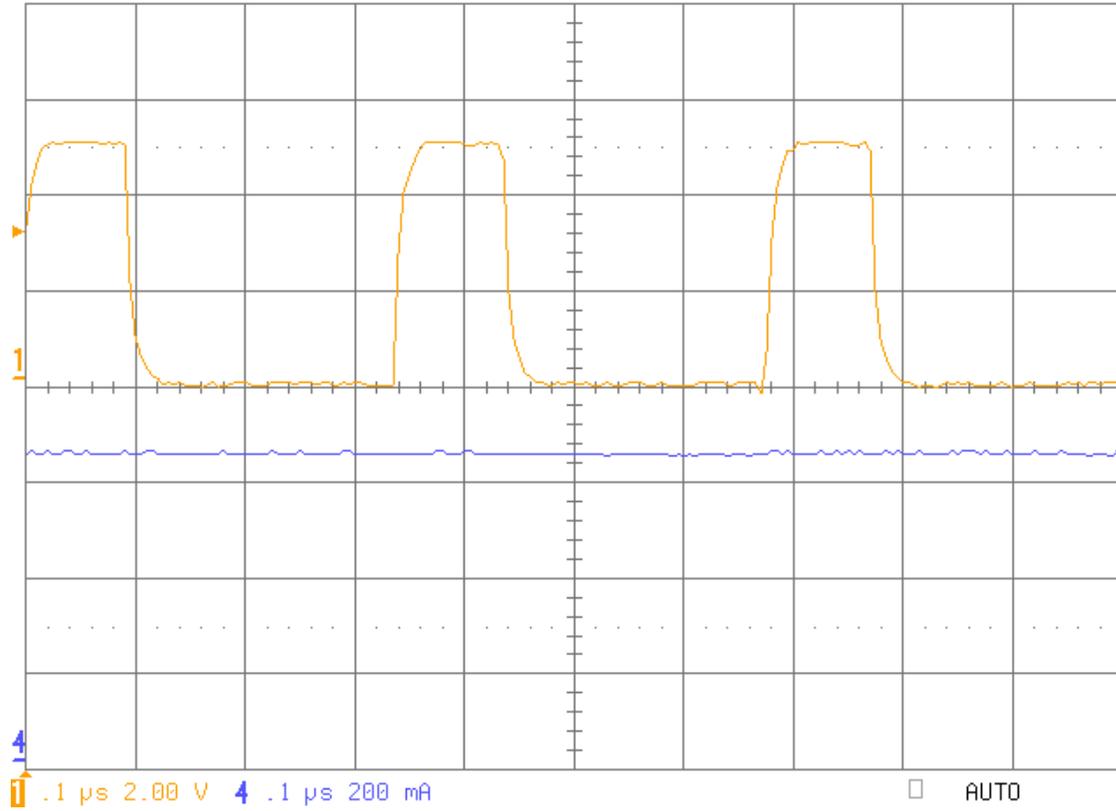
Fig 15: Switch node 1.2V @ 0.6A with 5Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

EFFICIENCY (TPS62353)

1.2V@0.6A Efficiency vs. Load Current
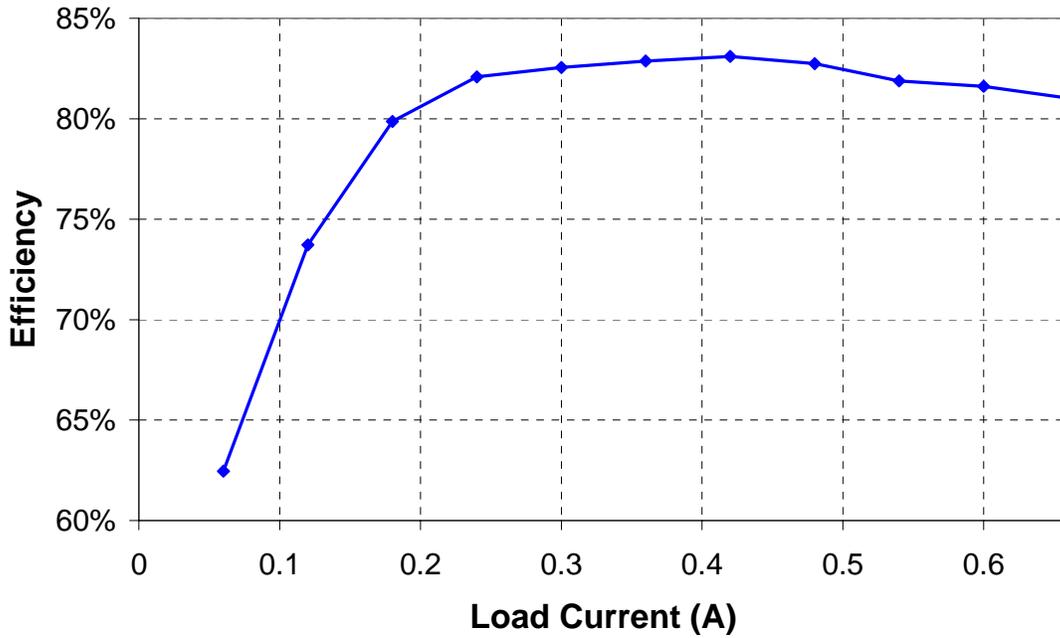
Fig 15: Efficiency of TPS62353 in Fixed PWM mode with 5Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS INSTRUMENTS

LOAD REGULATION (TPS 62353)

1.2V@0.66A Output Voltage vs. Load Current
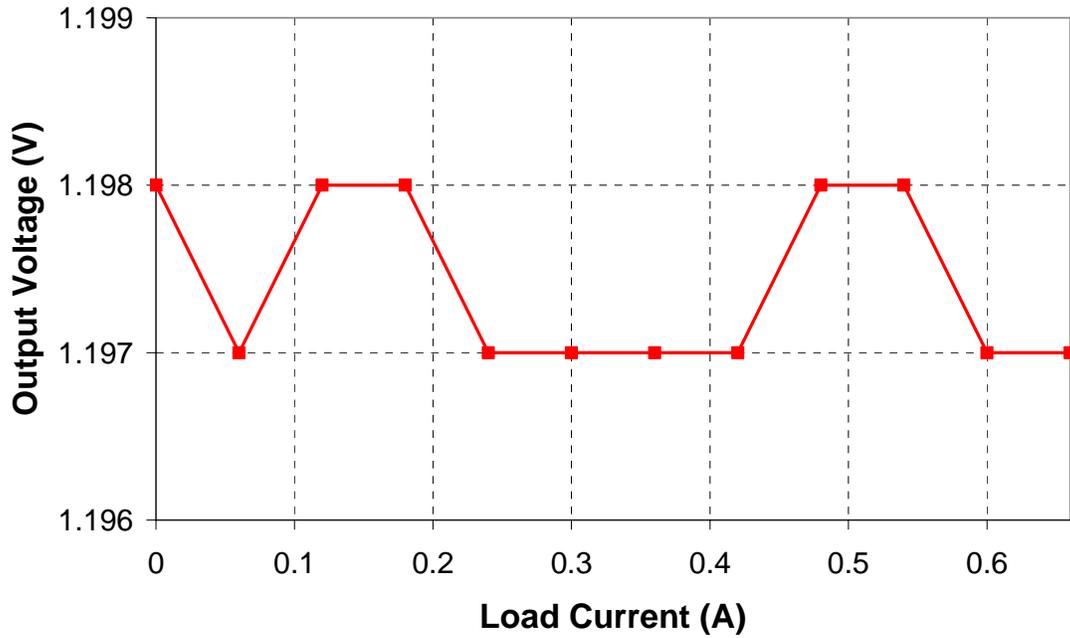
Fig 16: Load Regulation of TPS 62353 running in fixed PWM mode with 5Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS INSTRUMENTS

TPS 62200 – DCDC (3.3V @ 0.165A)

TPS 62200 has a 1-Mhz fixed frequency pulse width modulation (PWM) at moderate to heavy loads. For light loads, it automatically switches to the pulse frequency modulation (PFM) to increase efficiency. The current threshold for which the converter changes operation mode depends on input voltage and also if discontinuous conduction is detected.

OUTPUT RIPPLE (TPS 62200)

No load
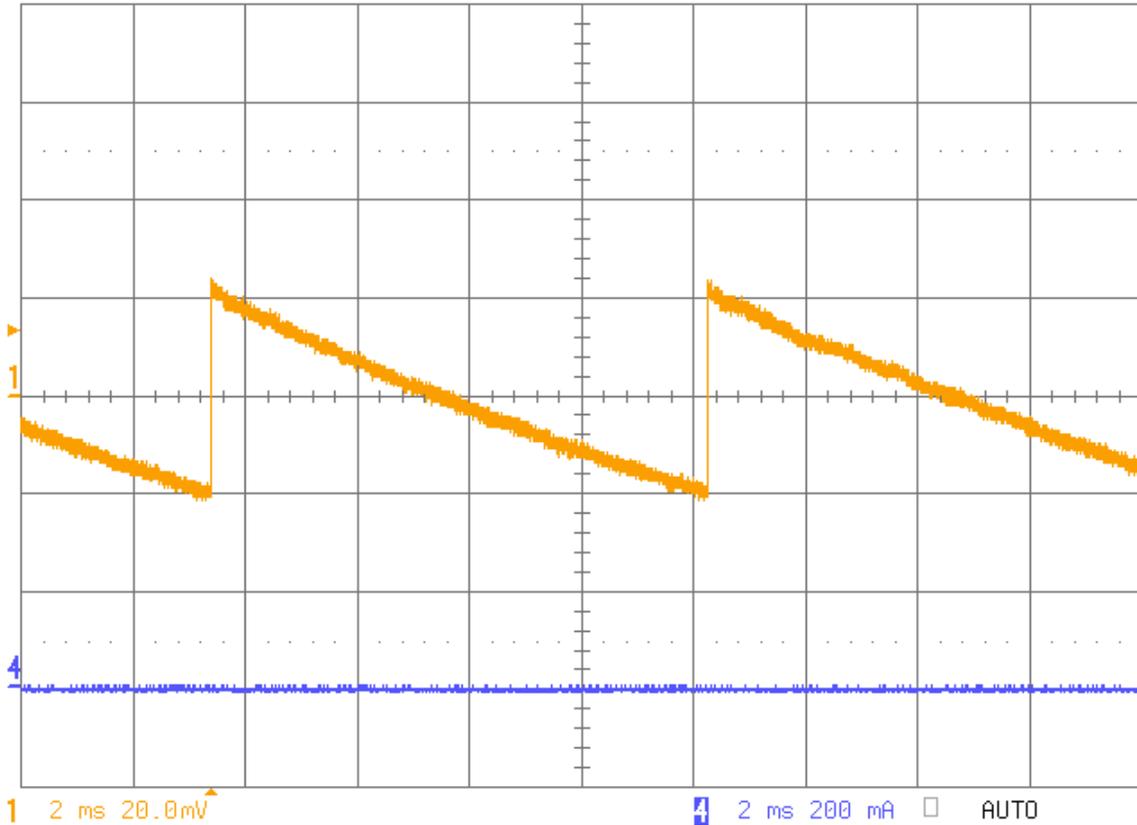
Fig 18: Output Ripple 3.3V (Ch1) @ no load (Ch4) TPS 62200 DCDC, Highline 5Vin, converter in PFM mode

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
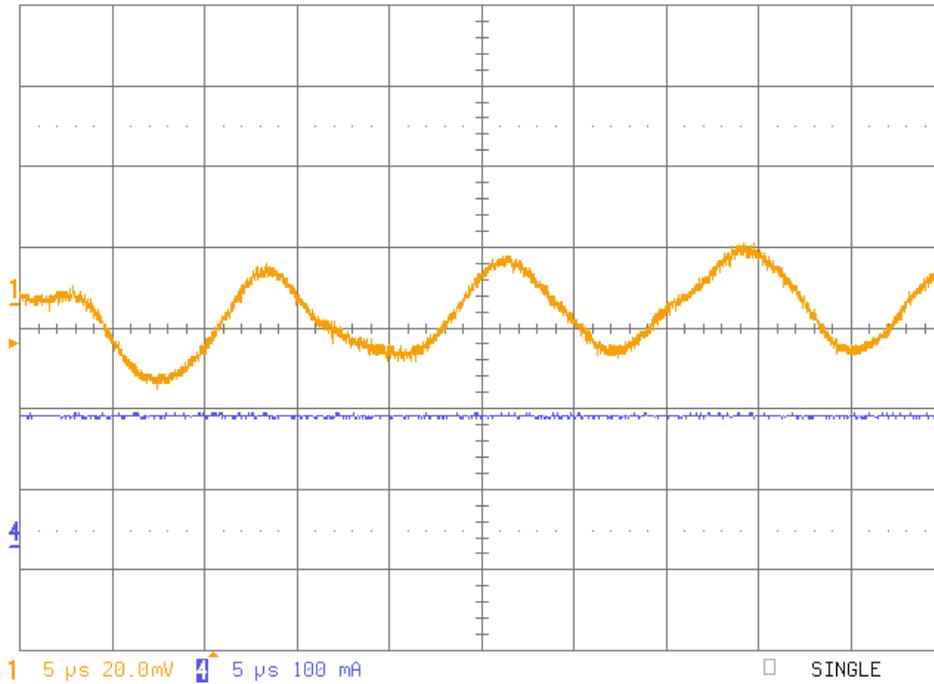
Full load, high line

Fig 17: Output Ripple 3.3V (Ch1) @ 0.165A (Ch4) TPS 62200 DCDC, Highline 6Vin, converted in PWM mode

Light load, high line
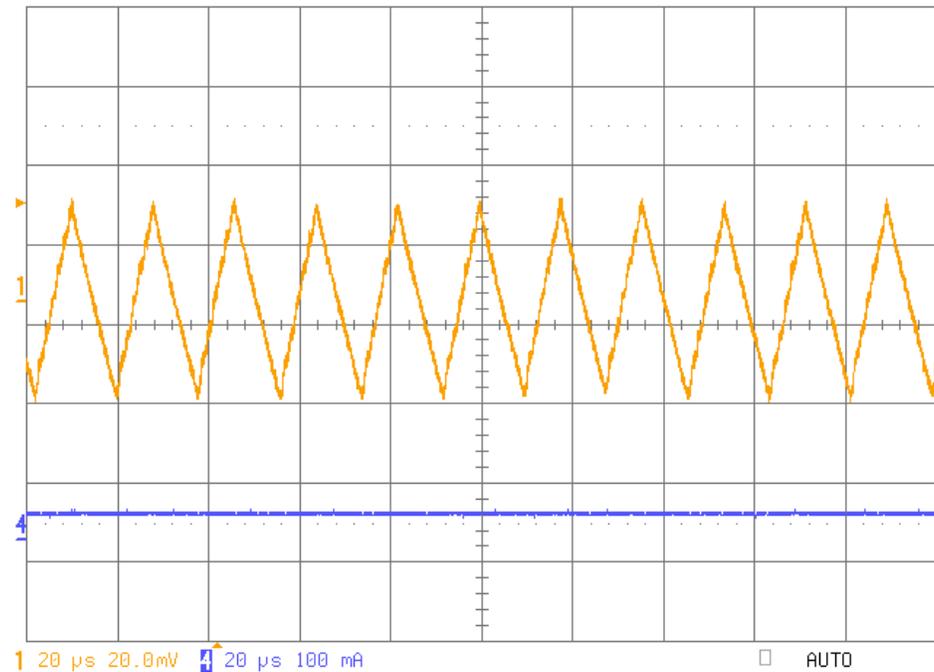
Fig 19: Output Ripple 3.3V (Ch1) @ 0.05 (Ch4) TPS 62200 DCDC, Highline 6Vin, converter in PFM mode

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
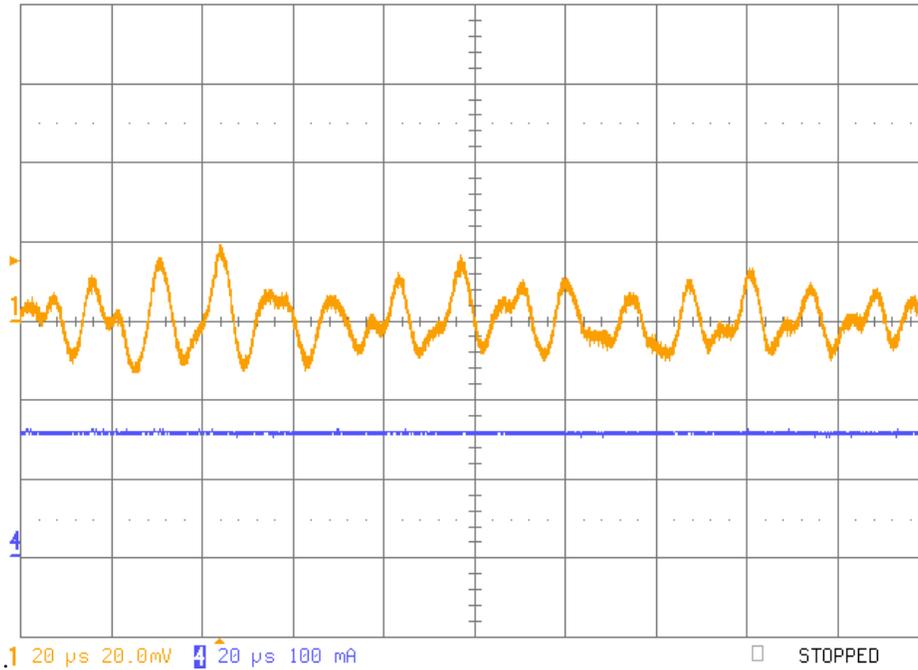
Heavy load, low line

Fig 20: Output Ripple 3.3V (Ch1) @ 0.165 (Ch4) TPS 62200 DCDC, Low Line 3.6Vin, converter in PWM mode

Light load, low line, worse case
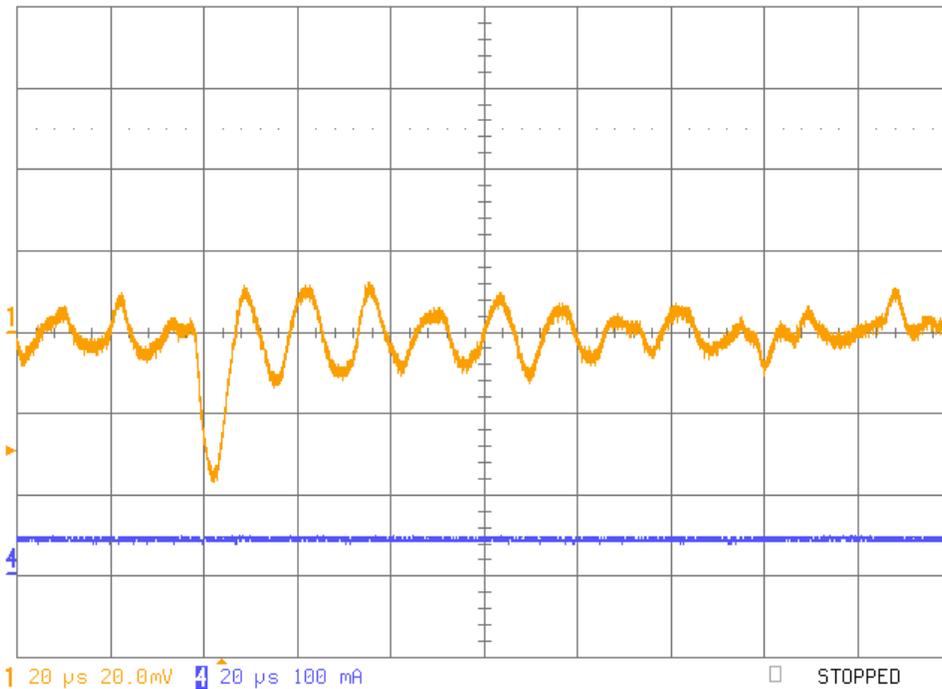
Fig 21: Output Ripple 3.3V (Ch1) @ 0.04 (Ch4) TPS 62200 DCDC, Low Line 3.6Vin, converter in PFM mode
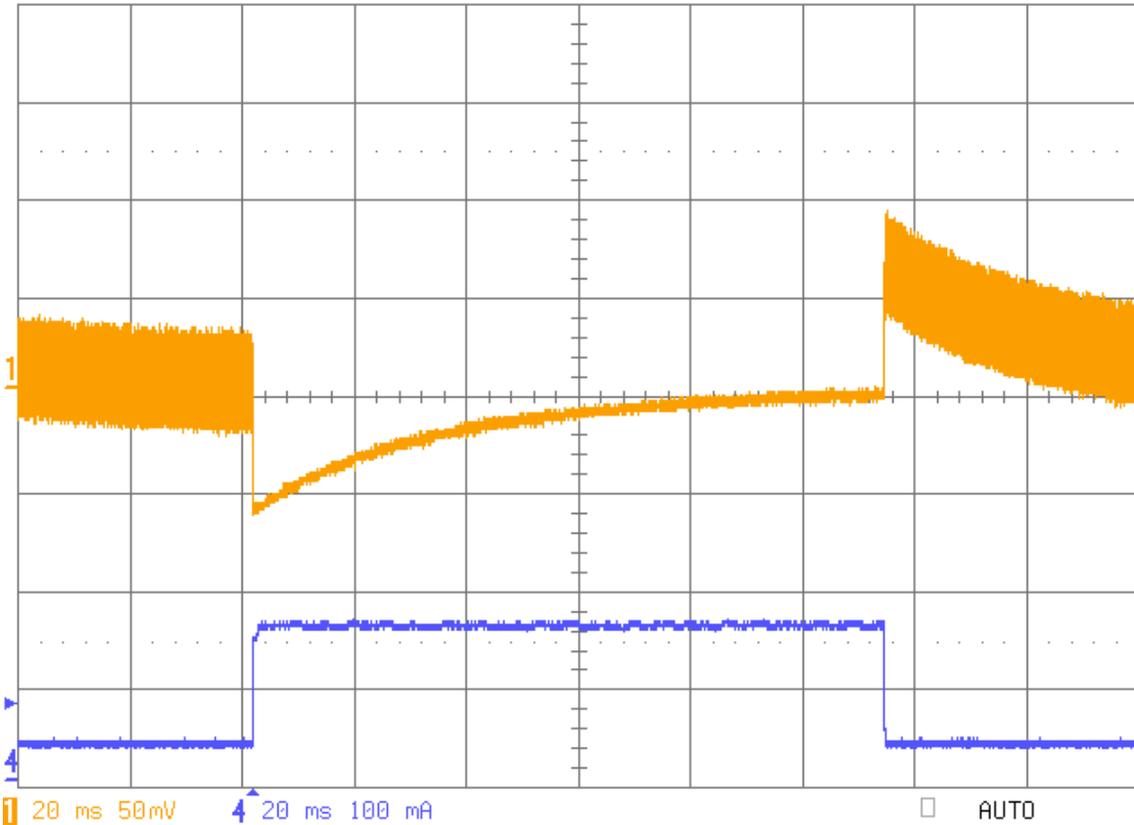
OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
LOAD TRANSIENT RESPONSE (TPS 62353)

Highline

Fig 22: Load transient response on TPS62200, 3.3V output (Ch1) for load step 40mA to 165mA (Ch4 - 25% to 100%), at high line 6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
4Vin
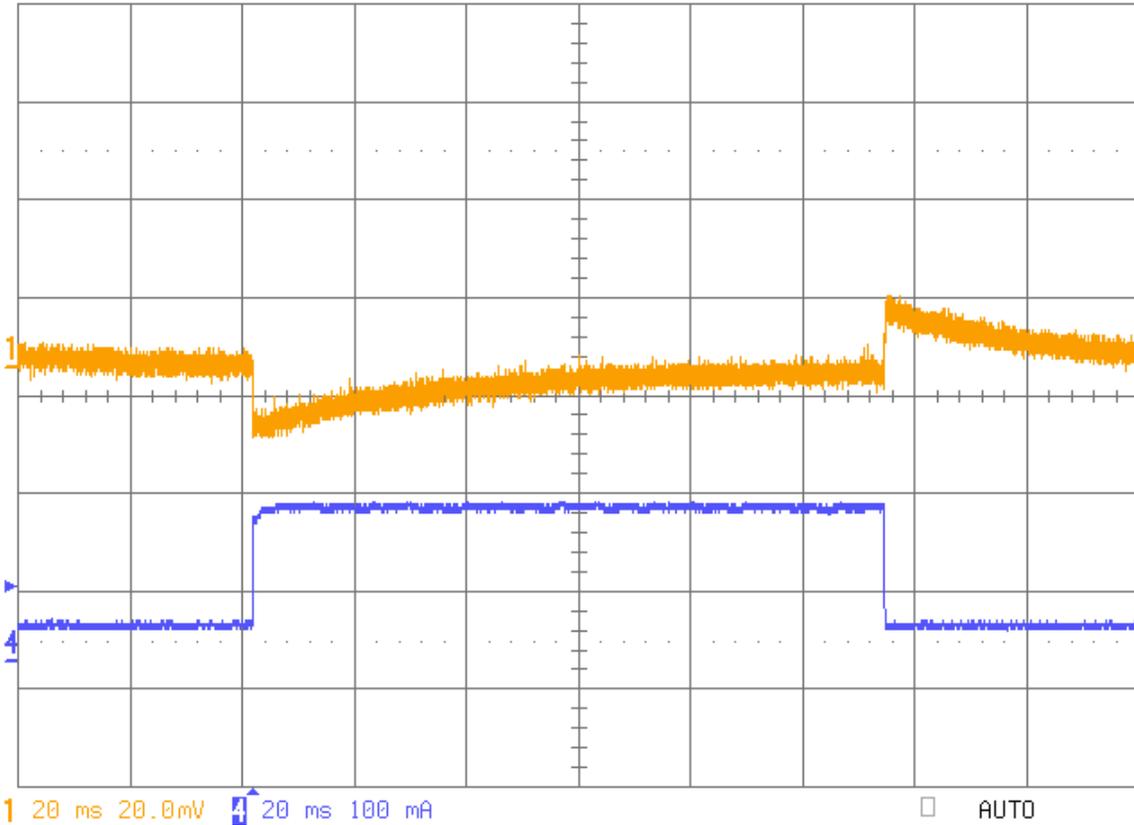
Fig 23: Load transient response on TPS62200, 3.3V output (Ch1) for load step 40mA to 165mA (Ch4 - 25% to 100%), at high line 4Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
Low Line
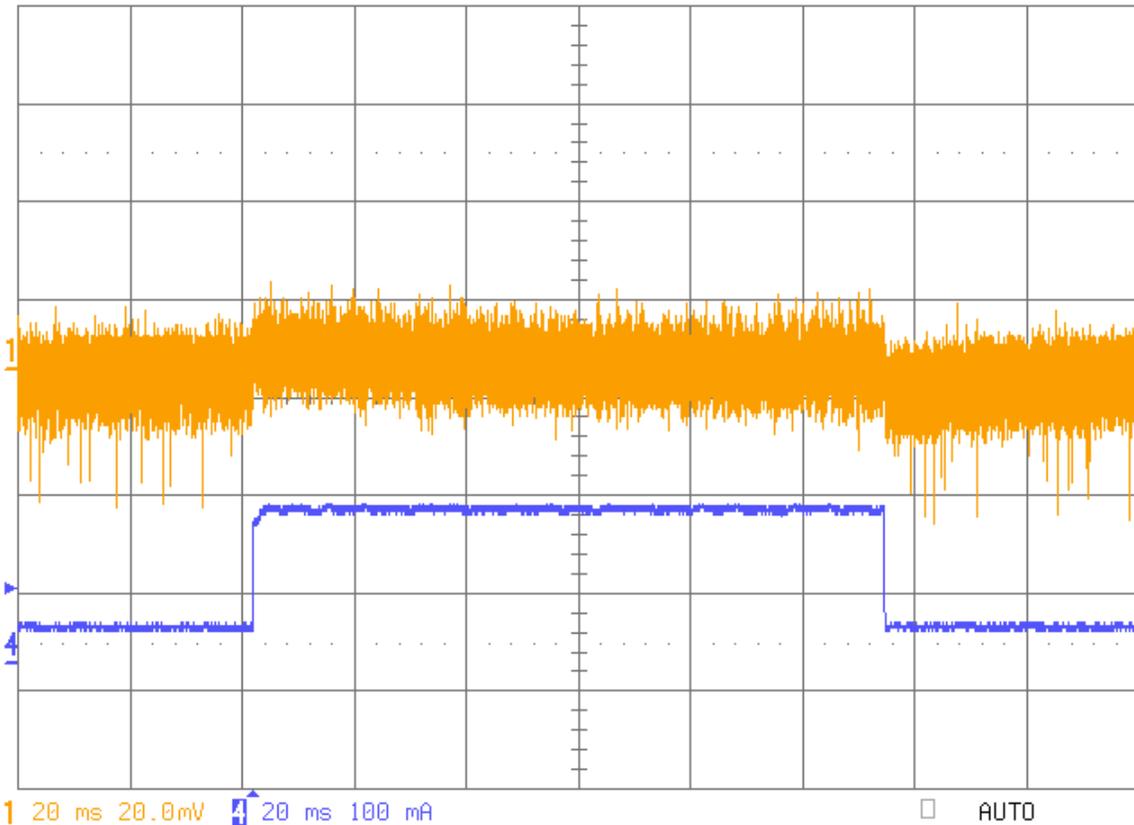
Fig 24: Load transient response on TPS62200, 3.3V output (Ch1) for load step 40mA to 165mA (Ch4 - 25% to 100%), at high line 3.6Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report
SWITCH NODE (TPS 62200)
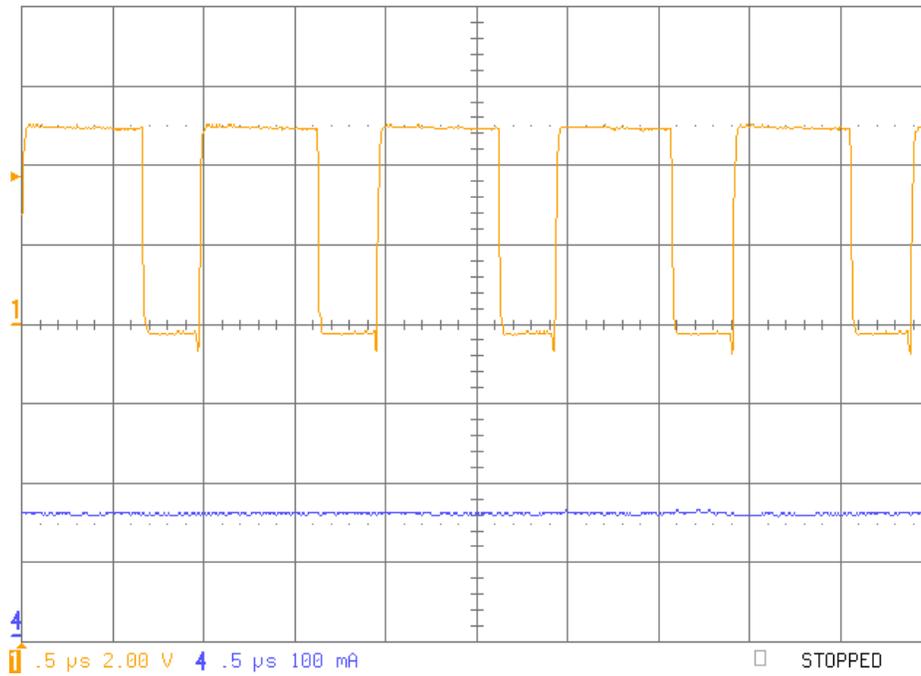
Fig 25: Switch node, PWM mode 5 V input, 3.3V@0.165A

Power Save Mode, No load
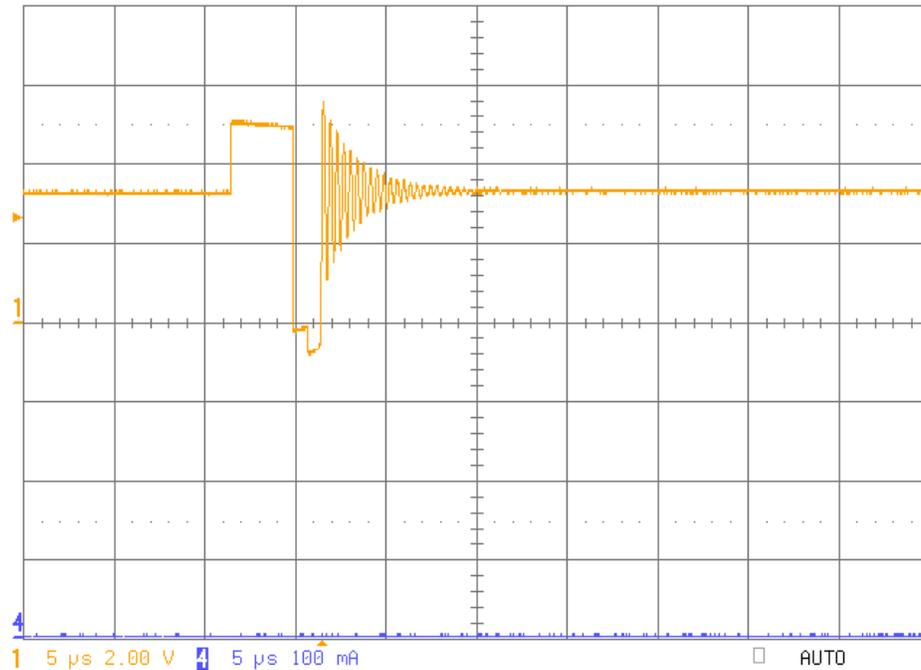
Fig 26: Switch node 5 Vin, 3.3V with no load

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

TEXAS INSTRUMENTS

EFFICIENCY (TPS62200)

### 3.3V @ 0.165A Efficiency vs. Load Current 5V in
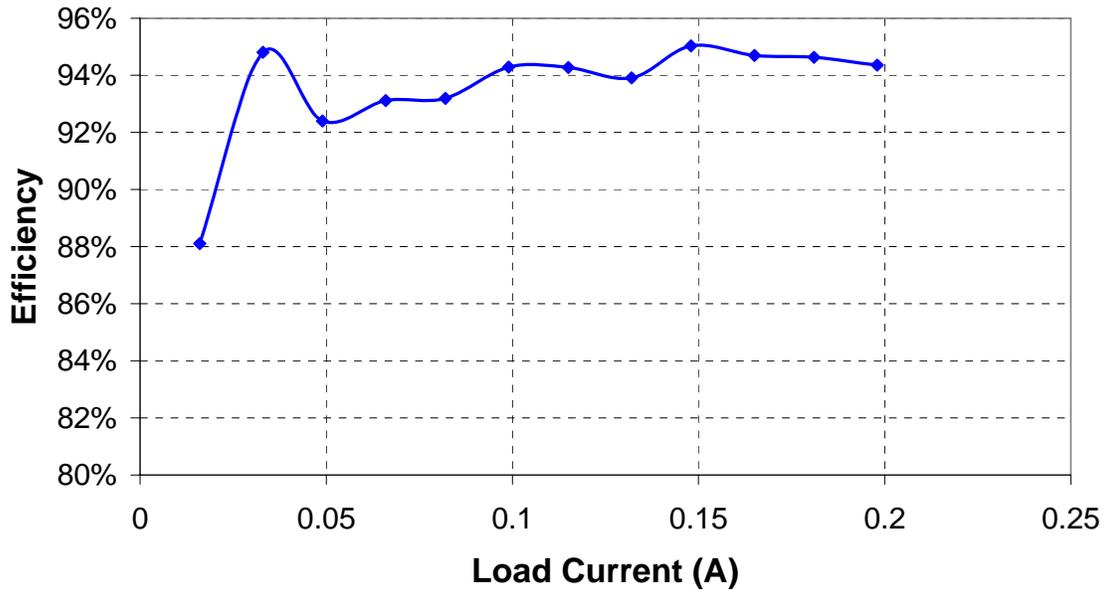
Fig 27: Efficiency of TPS62200 with 5Vin

OMAP-L137 / C6747 / C6745 / C6743
TPS62353, TPS62200, TPS71701, TPS73218 Test Report

LOAD REGULATION (TPS62200)

At light load, TPS 62200 implements dynamic voltage positioning by increasing the ouput voltage by about 0.8% above its nominal value to mitigate against the voltage drop that may occur during a load transient from light load to full load..

**3.3V @ 0.165A Output Voltage vs. Load Current
5V in**
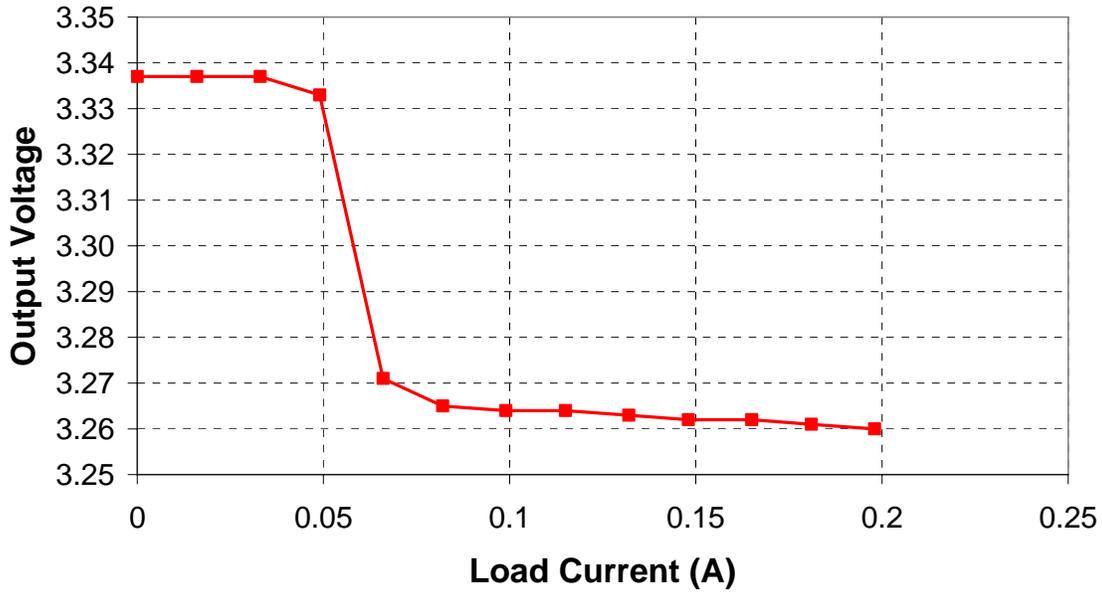
Fig 28: Load Regulation of TPS 62200 5Vin

重要声明

德州仪器 (TI) 及其下属子公司有权在不事先通知的情况下，随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改，并有权随时中止提供任何产品和服务。 客户在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。 所有产品的销售都遵循在订单确认时所提供的 TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合 TI 标准保修的适用规范。 仅在 TI 保修的范围内，且 TI 认为有必要时才会使用测试或其它质量控制技术。 除非政府做出了硬性规定，否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。 客户应对其使用 TI 组件的产品和应用自行负责。 为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 产品或服务的组合设备、机器、流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。 TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。 使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的数据手册或数据表，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。 在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。 TI 对此类篡改过的文件不承担任何责任。

在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示授权，且这是非法的、欺诈性商业行为。 TI 对此类虚假陈述不承担任何责任。

可访问以下 URL 地址以获取有关其它 TI 产品和应用解决方案的信息：

产品

放大器	http://www.ti.com.cn/amplifiers
数据转换器	http://www.ti.com.cn/dataconverters
DSP	http://www.ti.com.cn/dsp
接口	http://www.ti.com.cn/interface
逻辑	http://www.ti.com.cn/logic
电源管理	http://www.ti.com.cn/power
微控制器	http://www.ti.com.cn/microcontrollers

应用

音频	http://www.ti.com.cn/audio
汽车	http://www.ti.com.cn/automotive
宽带	http://www.ti.com.cn/broadband
数字控制	http://www.ti.com.cn/control
光纤网络	http://www.ti.com.cn/opticalnetwork
安全	http://www.ti.com.cn/security
电话	http://www.ti.com.cn/telecom
视频与成像	http://www.ti.com.cn/video
无线	http://www.ti.com.cn/wireless