

# 支持 USB 电池充电规范版本 1.2 检测功能的 BQ24392 双路 SPST USB 2.0 高速开关

## 1 特性

- USB 2.0 高速开关
- 检测符合 USB 电池充电规范版本 1.2 (BCv1.2) 的充电器
- 兼容附件
  - 专用充电端口
  - 标准下行端口
  - 充电下行端口
- 非标准充电器
  - Apple™ 充电器
  - TomTom™ 充电器
  - 不符合电池充电规范版本 1.2 (BCv1.2) 的 USB 充电器
- -2V 至 28V VBUS 电压范围
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
  - 4000V 人体放电模式
  - 1500V 组件充电模式 (C101)
- 至接地 (GND) 的 ESD 性能 DP\_CON/DM\_CON
  - ±8kV 接触放电 (IEC 61000-4-2)

## 2 应用

- 移动电话
- 智能手机
- 摄像机
- GPS 系统

## 3 说明

BQ24392 是一款具有充电器检测功能的双路单刀单掷 (SPST) USB 2.0 高速隔离开关, 可与 micro-USB 和 mini-USB 端口搭配使用。凭借这款 USB 开关, 移动电话、平板电脑和其它电池供电型电子设备可通过不同适配器充电, 并且系统软件需求最低。该器件的充电器检测电路可支持符合 USB 电池充电规范版本 1.2 (BCv1.2) 的 Apple™、TomTom™ 以及其它非标准充电器。

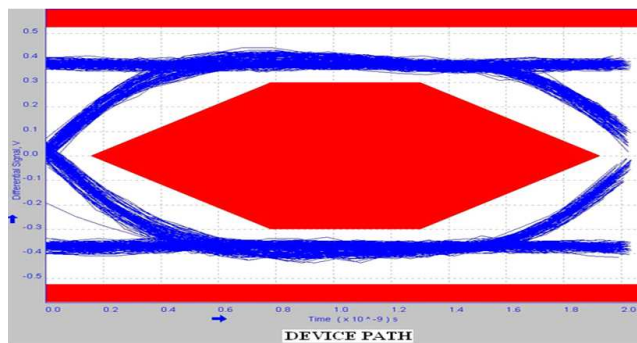
当 micro-USB 或 mini-USB 端口连接充电器时, BQ24392 器件由 VBUS 供电, 可承受 28V 电压, 无需外部保护。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
BQ24392	UQFN (10)	2.05mm x 1.55mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

### USB 开关的 480Mbps USB 2.0 眼图



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## 4 修订历史记录

<b>Changes from Revision F (July 2017) to Revision G</b>	<b>Page</b>
• Changed $R_{ON}$ From: 8 $\Omega$ TYP To: 3.5 $\Omega$ TYP, 6.9 $\Omega$ MAX in the <i>Electrical Characteristic</i> table .....	<b>5</b>

<b>Changes from Revision E (February 2017) to Revision F</b>	<b>Page</b>
• Changed CHG_DET diode direction from right facing to left facing in <i>Application Schematic</i> . .....	<b>10</b>

<b>Changes from Revision D (January 2016) to Revision E</b>	<b>Page</b>
• 从 BQ24932 更改为 BQ24392 (在说明) .....	<b>1</b>
• Changed From: BQ24932 To: BQ24392 in the <i>Overview</i> .....	<b>6</b>
• Changed title From: <i>Using the BQ24932 GPIOs</i> To: <i>Using the BQ24392 GPIOs</i> .....	<b>9</b>

<b>Changes from Revision C (January 2015) to Revision D</b>	<b>Page</b>
• Changed diode direction from left facing to right facing in <i>Application Schematic</i> . .....	<b>10</b>

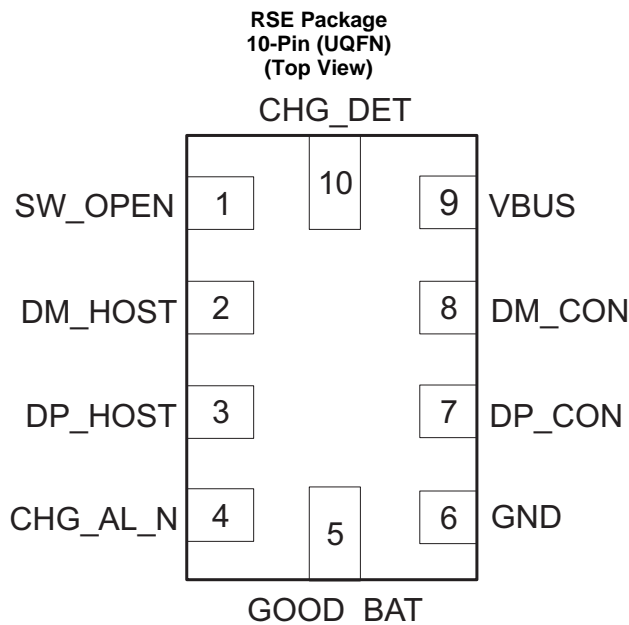
  

<b>Changes from Revision B (October 2014) to Revision C</b>	<b>Page</b>
• 更新了 特性。 .....	<b>1</b>

<b>Changes from Revision A (June 2012) to Revision B</b>	<b>Page</b>
• 添加了 <i>ESD</i> 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 .....	<b>1</b>

## 5 Pin Configuration and Functions



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### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SW_OPEN	O	USB switch status indicator Open-drain output. 10kΩ external pull-up resistor required SW_OPEN = LOW indicates when switch is connected SW_OPEN = HIGH-Z indicates when then switch is not connected
2	DM_HOST	I/O	D– signal to transceiver
3	DP_HOST	I/O	D+ signal to transceiver
4	CHG_AL_N	O	Charging status indicator Open-drain output. 10kΩ external pull-up resistor required CHG_AL_N = LOW indicates when charging is allowed CHG_AL_N = HIGH-Z indicates when charging is not allowed
5	GOOD_BAT	I	Battery status indication from system GOOD_BAT = LOW indicates a dead battery GOOD_BAT = HIGH indicates a good battery
6	GND	-	Ground
7	DP_CON	I/O	D+ signal from USB connector
8	DM_CON	I/O	D– signal from USB connector
9	VBUS	I	Supply pin from USB connector
10	CHG_DET	O	Charger detection indicator Push-Pull output to system CHG_DET = LOW indicates when a charger is not detected CHG_DET = HIGH indicates when a charger detected

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over –40°C to 85°C temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VBUS	–2	28	V
	CHG_AL_N	–2	28	V
	DM_HOST	–0.3	7	V
	DP_HOST	–0.3	7	
	GOOD_BAT	–0.3	7	
	DP_CON	–0.3	7	
	DM_CON	–0.3	7	
	CHG_DET	–0.3	7	
T <sub>stg</sub>	Storage temperature range	65	150	°C

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	
	IEC Contact discharge pins DP_CON and DM_CON to GND	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VBUS		4.75	5.25	V
GOOD_BAT		0	VBUS	
DM_HOST		0	3.6	
DP_HOST		0	3.6	
DM_CON		0	3.6	
DP_CON		0	3.6	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq24392	UNIT
		RSE	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	167.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	78.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	95.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	95.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

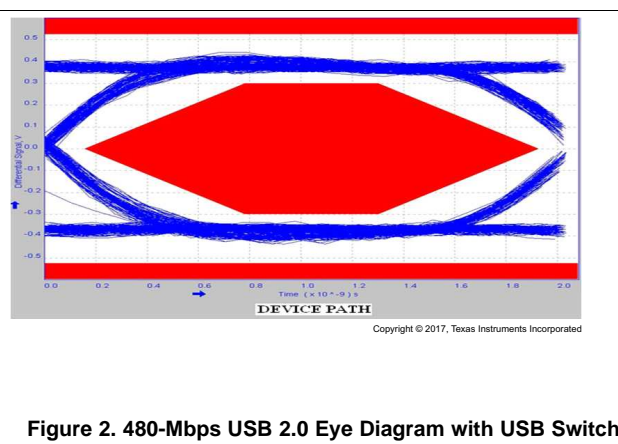
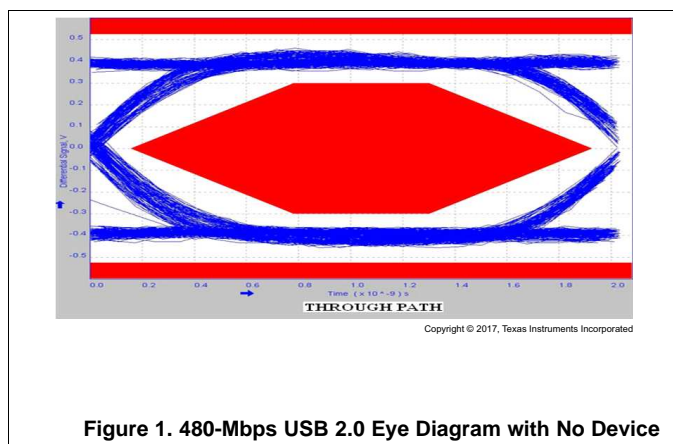
### 6.5 Electrical Characteristics

V<sub>BUS</sub> = 4.5 V to 5.5 V, T<sub>A</sub> = -40°C to 85°C (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V <sub>VBUS_VALID</sub>	VBUS Valid threshold	Rising VBUS threshold			3.5		V	
V <sub>OH</sub>	CHG_DET	CHG_DET	I <sub>OH</sub> = -2 mA	3.5		VBUS	V	
V <sub>OL</sub>	CHG_DET, SW_OPEN, CHG_AL_N	CHG_DET, SW_OPEN, CHG_AL_N	I <sub>OL</sub> = 2 mA			0.4	V	
V <sub>IH</sub>	High-level input voltage	GOOD_BAT		1.1			V	
V <sub>IL</sub>	Low-level input voltage					0.5	V	
R <sub>PD</sub>	Internal pull-down resistance					950	kΩ	
t <sub>DBP</sub>	Dead battery provision timer				32	45	Mins	
V <sub>USBIO</sub>	ON- state resistance match between	DM_CON, DP_CON, DM_HOST, DP_HOST	V <sub>DM_HOST</sub> and V <sub>DP_HOST</sub> = 0 to 3.6 V, I <sub>DP_CON</sub> and I <sub>DM_CON</sub> = -2 mA	0		3.6	V	
R <sub>ON</sub>	ON-state resistance					3.5	6.9	Ω
R <sub>ON(flat)</sub>	ON-state resistance flatness					1.1		Ω
ΔR <sub>ON</sub>	ON- state resistance match between channels					0.5		Ω
I <sub>CC-SW (ON)</sub>	Current consumption	V <sub>VBUS</sub> = 5V, V <sub>IH(GOOD_BAT)</sub> = 1.1 V			250		μA	
		V <sub>VBUS</sub> = 5 V, V <sub>IH(GOOD_BAT)</sub> = 2.5 V			80		μA	
I <sub>CC-SW (OFF)</sub>	Current consumption with USB switch off	V <sub>VBUS</sub> = 5 V; USB Switch OFF			45		μA	
I <sub>USBI/O (ON)</sub>	Leakage current with USB switch on	V <sub>DM_HOST</sub> and V <sub>DP_HOST</sub> = 0 to 3.6 V, I <sub>DP_CON</sub> and I <sub>DM_CON</sub> = -2 mA			50		nA	
I <sub>USBI/O (OFF)</sub>	Leakage current with USB switch off				45		nA	
C <sub>I(OFF)</sub>	Capacitance with USB switch off	DP_HOST, DM_HOST	DC bias = 0 V or 3.6 V, f = 10 MHz		2		pF	
C <sub>O(OFF)</sub>	Capacitance with USB switch off	DP_CON, DM_CON				10		pF
C <sub>I(ON)</sub>	Capacitance with USB switch on	DP_HOST, DM_HOST				11		pF
C <sub>O(ON)</sub>	Capacitance with USB switch on	DP_CON, DM_CON				11		pF
BW	Bandwidth	R <sub>L</sub> = 50 Ω, Switch ON			920		MHz	
O <sub>ISO</sub>	Isolation with USB switch off	f = 240 MHz, R <sub>L</sub> = 50 Ω, Switch OFF			-26		dB	
X <sub>TALK</sub>	Crosstalk	f = 240 MHz, R <sub>L</sub> = 50 Ω			-30.5		dB	

(1) CHG\_DET max value will be clamped at 7 V when V<sub>VBUS</sub> > 7 V

### 6.6 Typical Characteristics



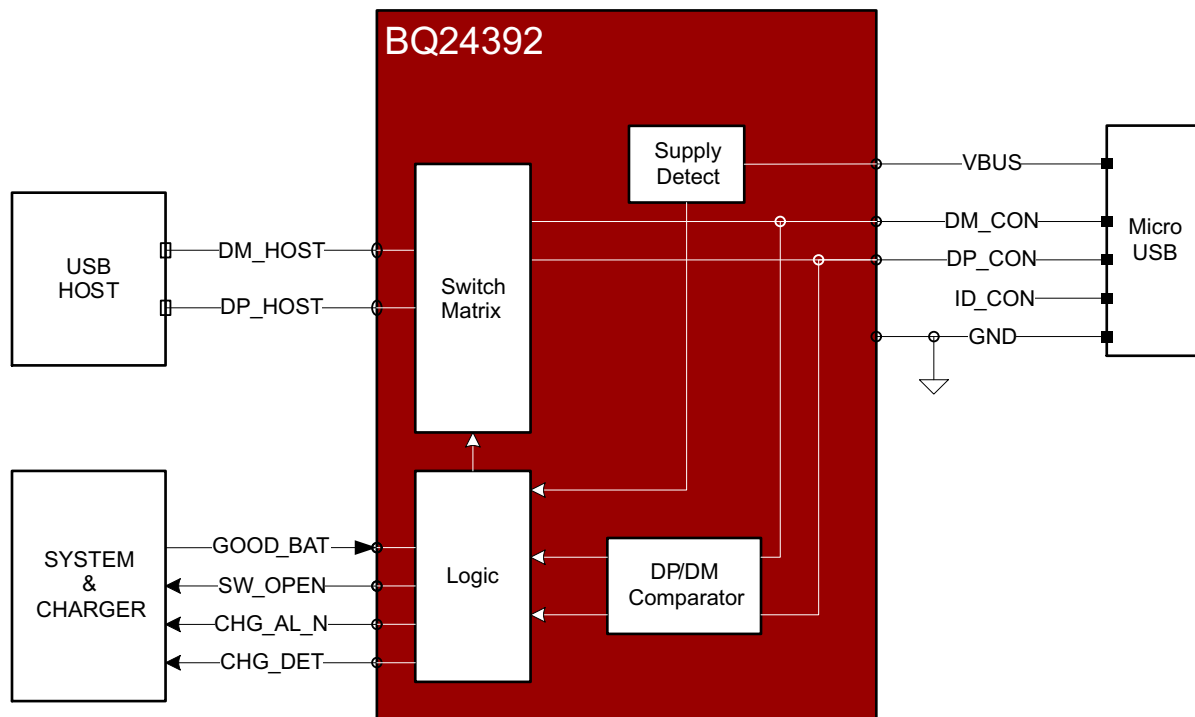
## 7 Detailed Description

### 7.1 Overview

The BQ24392 is a USB 2.0 high-speed isolation switch with charger detection capabilities for use with micro and mini-USB ports. Upon plugin of a Battery Charging Specification 1.2 (BCv1.2) compliant, Apple™, TomTom™, or other USB charger into a micro or mini-USB connector, the device will automatically detect the charger and operate the USB 2.0 high-speed isolation switch.

The BQ24392 device is powered through VBUS when a charger is attached to the micro or mini-USB port and has a 28-V tolerance to avoid the need for external protection.

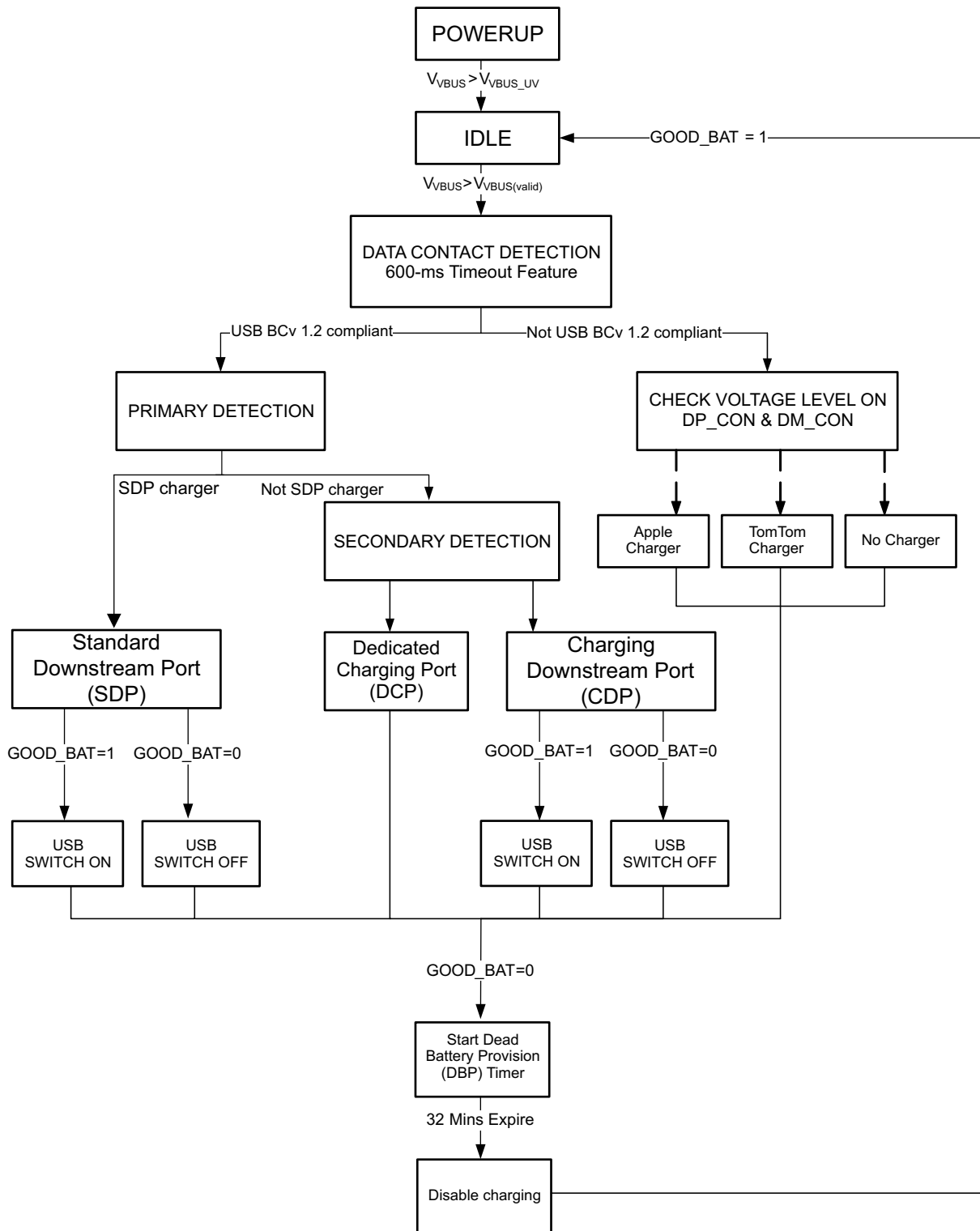
### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 Charger Detection



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Figure 3. Charge Detection Block Diagram

## Feature Description (continued)

When a micro or mini-USB accessory is inserted into the connector and once VBUS is greater than  $V_{VBUS\_VALID}$  threshold, the BQ24392 will enter into the Data Contact Detection (DCD) state which includes a 600-ms timeout feature that is prescribed in the USB Battery Charging Specification version 1.2 (BCv1.2). If the micro or mini-USB accessory is determined to be USB BCv1.2 compliant, a 130-ms debounce period will initiate and the BQ24392 will proceed to its primary detection and then secondary detection states to determine if a Dedicated Charging Port (DCP), Standard Downstream Port (SDP), or Charging Downstream Port (CDP) is attached to the USB-port. The minimum detection time for a DCP, SDP, and CDP is 130 ms, but can be as long as 600 ms due to the slow plug in effect.

If the GOOD\_BAT pin is high, the USB 2.0 switches are automatically closed to enable data transfer after the device detects a Standard Downstream Port (SDP) or Charging Downstream Port (CDP) was connected.

If Data Contact Detection (DCD) fails, the BQ24392 proceeds to detect whether an Apple or TomTom charger was inserted by checking the voltage level on DP\_CON and DM\_CON. Thus, for Apple and TomTom chargers, detection time typically takes ~600 ms.

The 3 output pins CHG\_AL\_N, CHG\_DET, and SW\_OPEN change their status at the end of detection. [Table 1](#) is the detection table with the GPIO status for each type of supported charger. More information on how to use the GPIOs is available in [Using the BQ24392 GPIOs](#).

**Table 1. Detection Table**

Device Type	VBUS	DP_CON (D+)	DM_CON (D-)	GOOD_BAT (Input)	CHG_AL_N (Output)	CHG_DET (Output)	SW_OPEN (Output)	Switch Status	Charge Current
Standard Downstream Port	> 3.5 V	Pull-down R to GND	Pull-down R to GND	HIGH	LOW	LOW	LOW	Connected	Charge with 100 mA/ Change the input current based on enumeration
				LOW	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Charging Downstream Port	> 3.5 V	Pull-down R to GND	$V_{DM\_SRC}$	HIGH	LOW	HIGH	LOW	Connected	Charge with full current
				LOW	LOW	HIGH	High-Z	Not Connected	Charge with 100 mA
Dedicated Charging Port	> 3.5 V	Short to D-	Short to D+	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
Apple Charger	> 3.5 V	$2.0 < V_{DP\_CON} < 2.8$	$2.0 < V_{DM\_CON} < 2.8$	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
TomTom Charger	> 3.5 V	$2.0 < V_{DP\_CON} < 3.1$	$2.0 < V_{DM\_CON} < 3.1$	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
PS/2 Charger	> 3.5 V	Pull-up R to $V_{VBUS}$	Pull-up R to $V_{VBUS}$	X	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Non-compliant USB Charger	> 3.5 V	Open	Open	X	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Any Device	< 3.5 V	Open	Open	X	High-Z	LOW	High-Z	Not Connected	No Charge
Any Device DBP Timer Expired	> 3.5 V	X	X	LOW	High-Z	LOW	High-Z	Not Connected	No Charge

If a charge has been detected and the GOOD\_BAT pin is low, a Dead Battery Provision (DBP) timer is initiated. If the GOOD\_BAT continues to be low for 30 minutes (maximum of 45 minutes), charging is disabled and CHG\_AL\_N goes into the High-Z state to indicate this. Toggling GOOD\_BAT high after the DBP timer expires re-starts detection and the DBP timer.

## 7.4 Device Functional Modes

The BQ24392 has two functional modes USB switch ON and USB switch OFF.



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Using the BQ24392 GPIOs

##### 8.1.1.1 CHG\_AL and CHG\_DET

The BQ24392 has 2 charger indicators, CHG\_AL\_N and CHG\_DET, that the host can use to determine whether it can charge and if it can charge at a low or high current. [Table 2](#) demonstrates how these outputs should be interpreted. CHG\_AL\_N is an open drain output and is active when the output of the pin is low. CHG\_DET is a push-pull output and is high in the active state.

**Table 2. bq24392 Outputs**

CHG_AL_N	CHG_DET	
High-Z	X	Charging is not allowed
Low	Low	Low-current charging is allowed
Low	High	High-current charging is allowed

The system must define what is meant by low-current and high-current charging. If CHG\_DET is high, a system could try to draw 2 A, 1.5 A, or 1.0 A. If the system is trying to support > 1.5-A chargers, then the system has to use a charger IC that is capable of monitoring the VBUS voltage as it tries to pull the higher current values. If the voltage on VBUS starts to drop because that high of a current is supported then the system has to reduce the amount of current it is trying to draw until it finds a stable state with VBUS not dropping.

##### 8.1.1.2 SW\_OPEN

SW\_OPEN is an open drain output that indicates whether the USB switches are opened or closed. In the High-Z state the switches are open and in the active, or low state, the switches are closed. The host should monitor this pin to know when the switches are closed or open.

##### 8.1.1.3 GOOD\_BAT

GOOD\_BAT is used by the host controller to indicate the status of the battery to the BQ24392. This pin affects the switch status for a SDP or CDP, and it also affects the Dead Battery Provision (DBP) timer as discussed in the [Charger Detection](#) section.

##### 8.1.1.4 Slow Plug-in Event

As you insert a charger into the USB receptacle, the pins are configured so that the VBUS and GND pins make contact first. This presents a problem as the BQ24392 (or any other charger detection IC) requires access to the D+ and D– lines to run detection. This is why the BQ24392 has a standard 130-ms debounce time after VBUS valid to run the detection algorithm. This delay helps minimize the effects of the D+ and D– lines making contact after VBUS and GND.

[Figure 4](#) is from the datasheet of a standard male micro-USB connector and shows how the data connections (red line) are slightly recessed from the power connections (blue line).

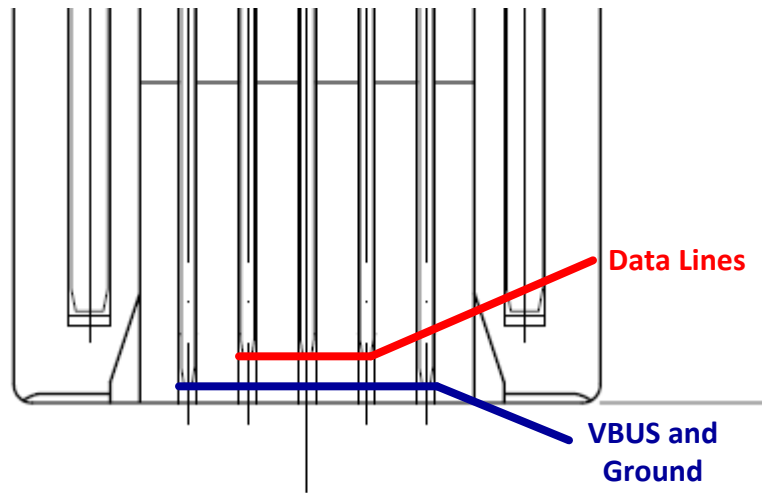
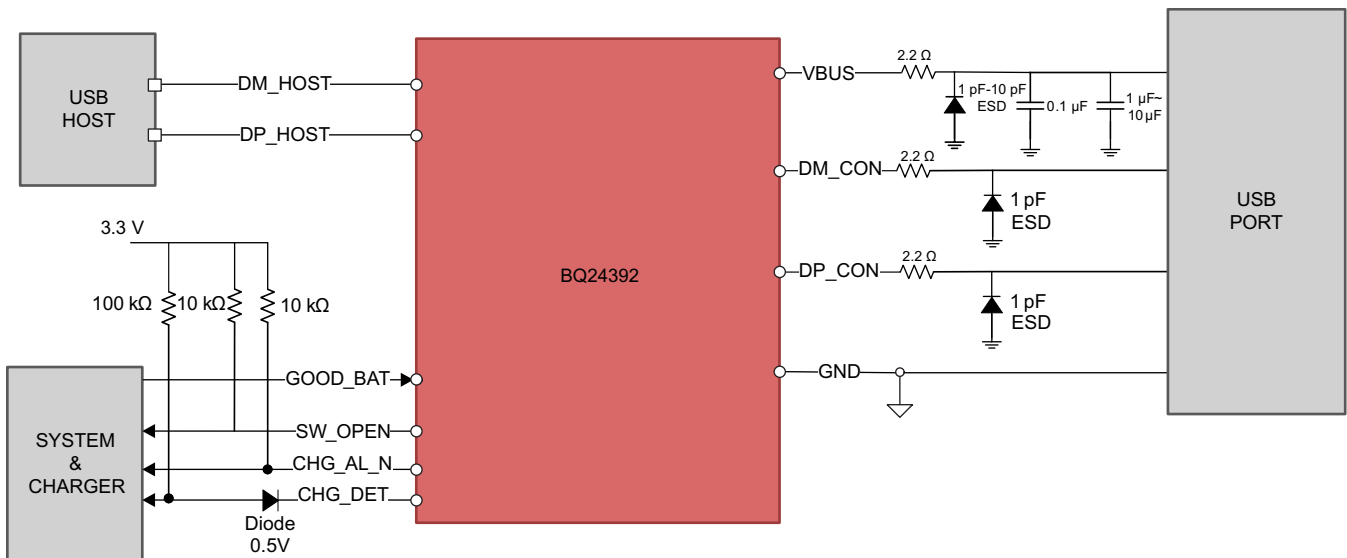


Figure 4. Data Connections Recessed from Power Connections

However, in some cases the charger is inserted very slowly, causing the VBUS and GND to make contact long before D+ and D-. Due to this effect, there is no guaranteed detection time as the detection time can vary based on how long it takes to insert the charger. If longer than 600 ms is taken to insert the charger into the USB receptacle, the detection algorithm of the BQ24392 will timeout and instead of the charger being detected as a DCP, it is now detected as a nonstandard charger (D+ and D- floating).

### 8.2 Typical Application

The BQ24392 device is used between the micro or mini-USB connector port and USB host to enable and disable the USB data path and detect chargers that are inserted into the micro or mini-USB connector.



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Figure 5. Application Schematic

## Typical Application (continued)

### 8.2.1 Design Requirements

VBUS requires 1µF - 10µF and 0.1-µF bypass capacitors to reduce noise from circuit elements by providing a low impedance path to ground for the unwanted high frequency content. The 0.1-µF capacitor filters out higher frequencies and has a lower series inductance while the 1µF ~1 0µF capacitor filters out the lower frequencies and has a much higher series inductance. Using both capacitors will provide better load regulation across the frequency spectrum.

SW\_OPEN and CHG\_AL\_N are open-drain outputs that require a 10-kΩ pull-up resistor to VDDIO.

VBUS, DM\_CON, and DP\_CON are recommended to have an external resistor of 2.2-Ω to provide extra ballasting to protect the chip and internal circuitry.

DM\_CON and DP\_CON are recommended to have a 1-pF external ESD protection diode rated for 8-kV IEC protection to prevent failure in case of an 8-kV IEC contact discharge.

VBUS is recommended to have a 1-pF ~ 10-pF external ESD Protection Diode rated for 8-kV IEC protection to prevent failure in case of an 8-kV IEC contact discharge

CHG\_DET is a push-pull output pin. An external pull-up and diode are shown to depict a typical 3.3-V system. The pull-up resistor and diode are optional. The pull-up range on the CHG\_DET pin is from 3.5 V to V<sub>VBUS</sub>. When V<sub>VBUS</sub> > 7 V, CHG\_DET will be clamped to 7 V.

### 8.2.2 Detailed Design Procedure

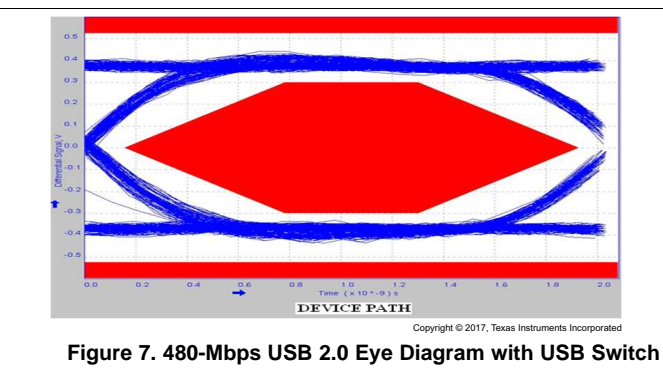
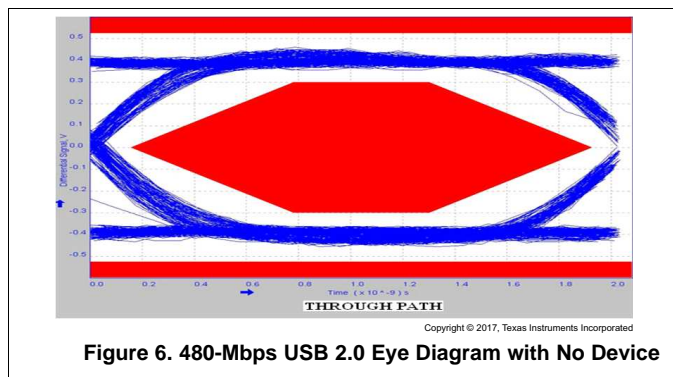
The minimum pull-up resistance for the open-drain data lines is a function of the pull-up voltage V<sub>PU</sub>, output logic LOW voltage V<sub>OL(max)</sub>, and Output logic LOW current I<sub>OL</sub>.

$$R_{PU(MIN)} = (V_{PU} - V_{OL(MAX)}) / I_{OL} \tag{1}$$

The maximum pull-up resistance for the open-drain data lines is a function of the maximum rise time of the desired signal, t<sub>r</sub>, and the bus capacitance, C<sub>b</sub>.

$$R_{PU(MAX)} = t_r / (0.8473 \times C_b) \tag{2}$$

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

Power to the device is supplied through the VBUS pin from the device that is inserted into the mini or micro-USB port. The power from the inserted devices should follow the USB 2.0 standard 5 V at 500 mA. VBUS also requires 1µF – 10µF and 0.1-µF bypass capacitors to reduce noise from circuit elements by providing a low impedance path to ground for the unwanted high frequency content.

## 10 Layout

### 10.1 Layout Guidelines

Place VBUS bypass capacitors as close to VBUS pin as possible and avoid placing the bypass caps near the DP/DM traces.

The high speed DP/DM traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of  $90 \Omega \pm 15\%$ . In layout, the impedance of DP and DM traces should match the cable characteristic differential 90- $\Omega$  impedance.

Route the high-speed USB signals on the plane closest to the ground plane, whenever possible.

Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

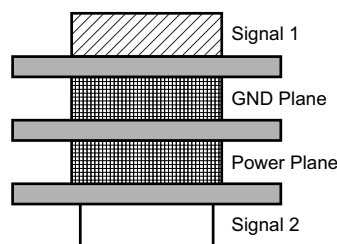
Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 8](#).



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**Figure 8. Four-Layer Board Stack-Up**

The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. Sufficient decoupling must be used when running signal traces across split planes is unavoidable. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

### 10.2 Layout Example

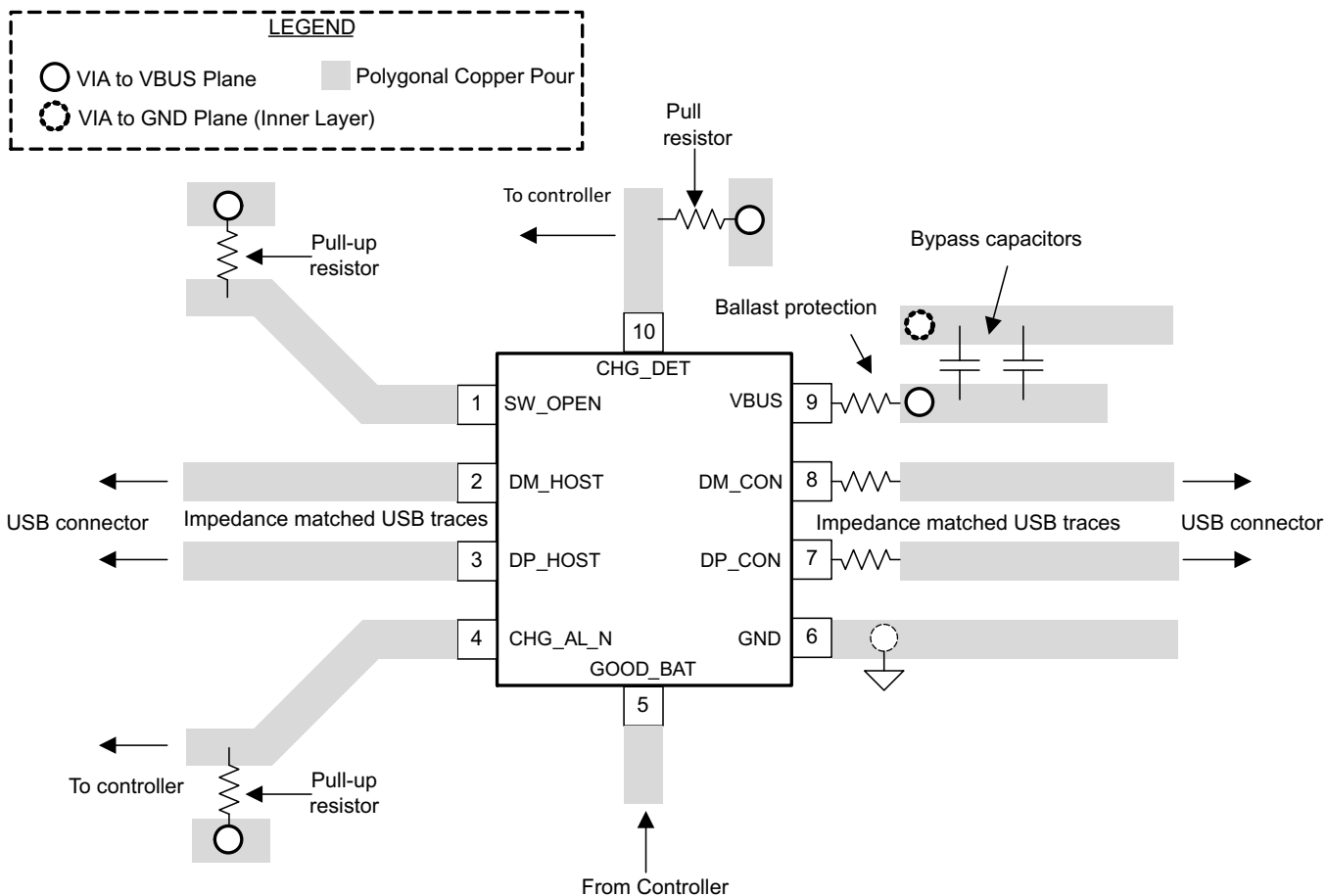


Figure 9. Package Layout Example

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.3 商标

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### 11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24392RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	APH	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF BQ24392 :**

- Automotive : [BQ24392-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

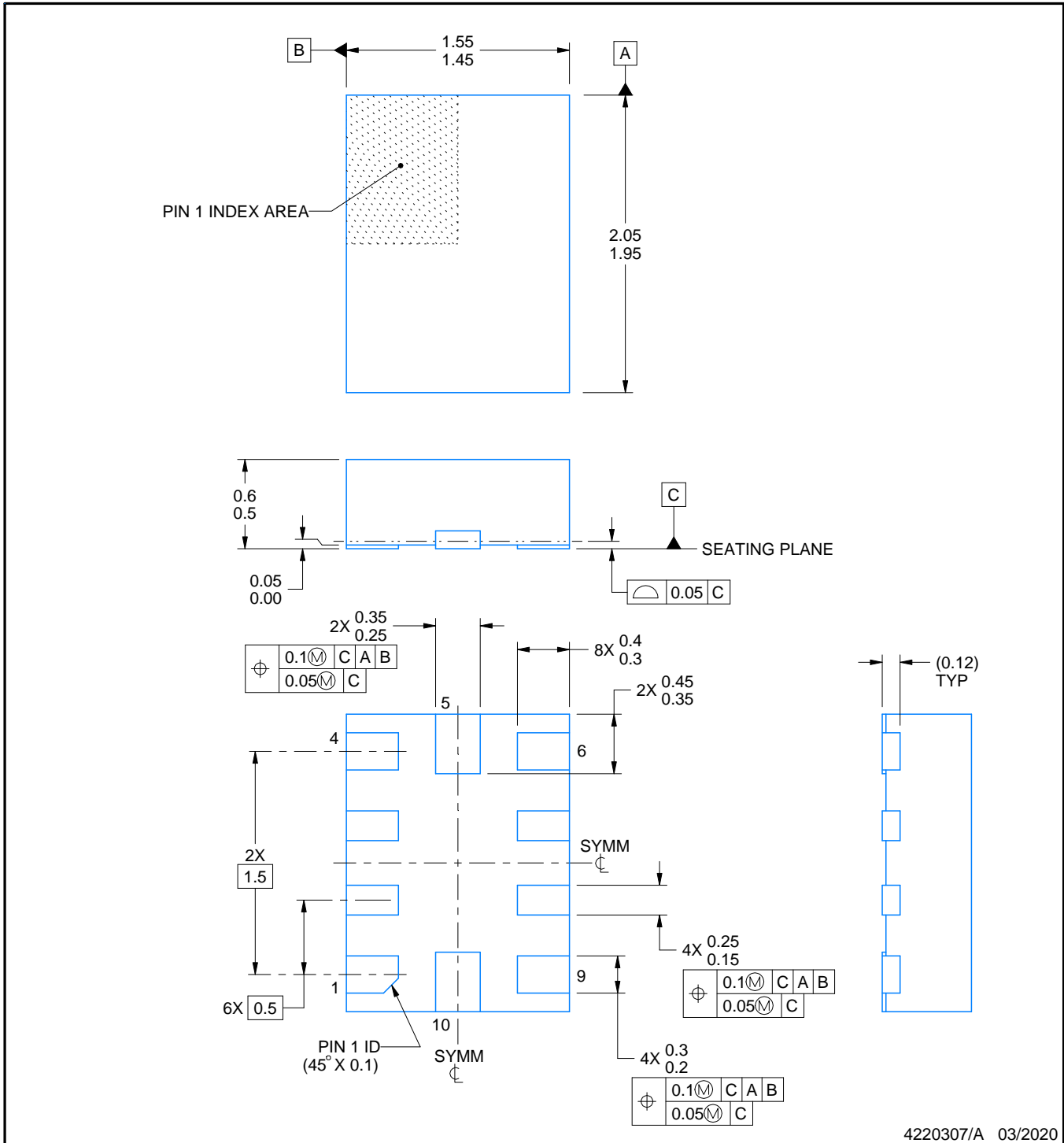
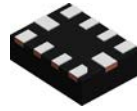
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24392RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24392RSER	UQFN	RSE	10	3000	202.0	201.0	28.0



4220307/A 03/2020

NOTES:

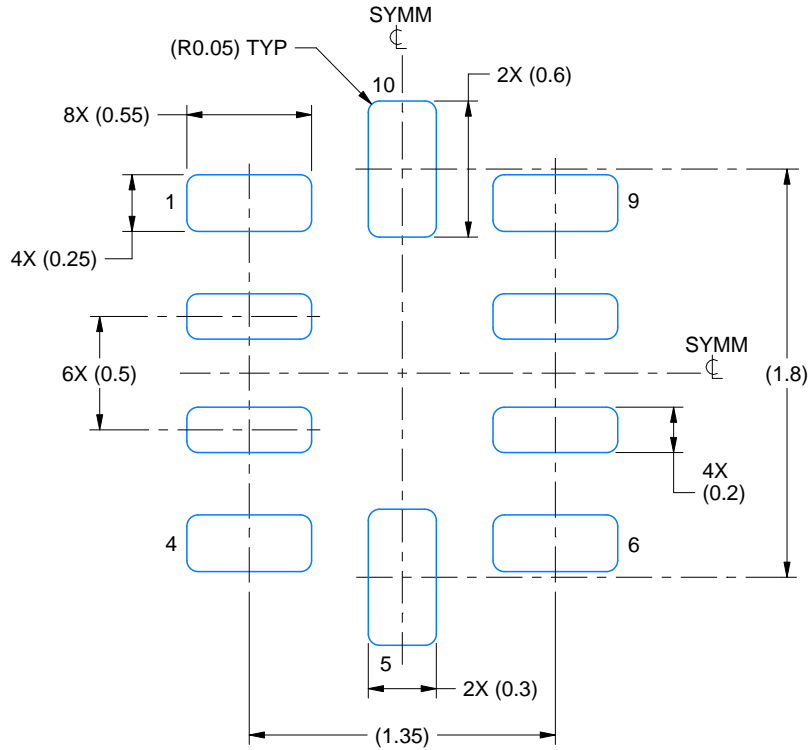
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

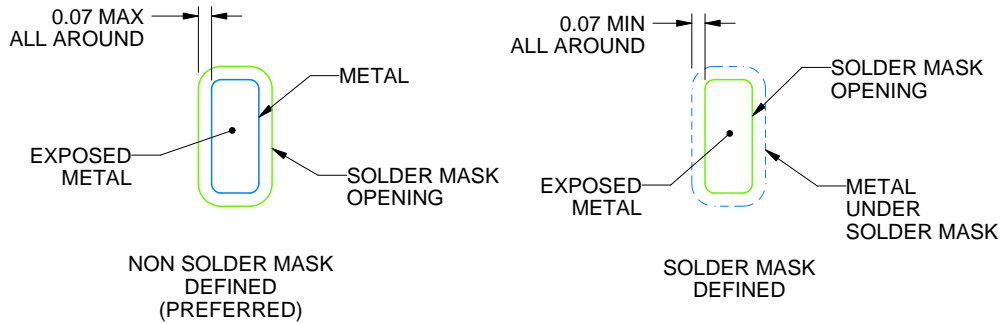
RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

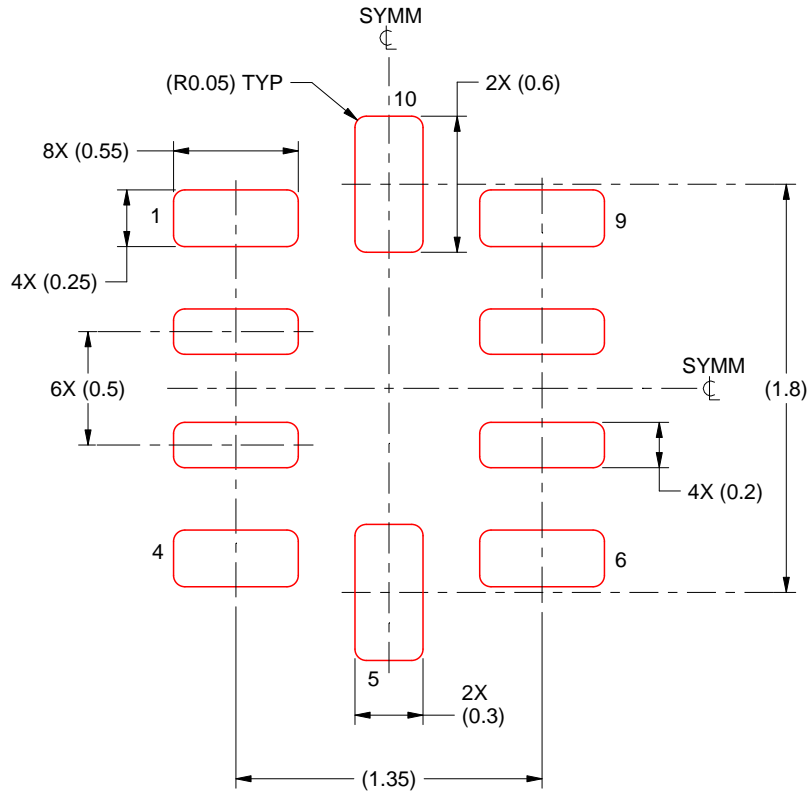
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICKNESS  
 SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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