HD3SS3212-Q1 双通道差分 2:1/1:2 USB3.2 多路复用器/多路信号分离器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 2：–40°C 至 +105°C，T_A
- 提供面向支持第 1 代和第 2 代 USB 3.2 数据速率的 USB Type-C™ 生态系统的多路复用器/多路信号分离器解决方案
- 与 MIPI DSI/CSI、FPD-Link III、LVDS 以及 PCIe 第 II 代、第 III 代兼容
- 运行速率高达 10Gbps
- -3dB 差动带宽宽达 8GHz 以上
- 出色的动态特性（5GHz 时）
  - 串扰 = –28dB
  - 关断隔离 = –19dB
  - 插入损耗 = –2dB
  - 回损 = –8dB
- 双向“多路复用器/多路信号分离器”差分开关
- 支持 0V 至 2V 的共模电压
- 3.3V 的单电源电压 V_{CC}
- 采用汽车友好型 QFN 封装（2.5mm x 4.5mm，间距为 0.5mm）

2 应用

- USB Type-C™ 生态系统
- 汽车媒体接口
- 音响主机
- 后座娱乐系统
- FPD-Link II 和 FPD-Link III 开关
- MIPI DSI/CSI-2 开关

3 说明

HD3SS3212-Q1 是一款采用多路复用器或多路信号分离器配置的高速双向无源开关。它适用于支持 USB 3.2 第 1 代和第 2 代数据速率的 USB Type-C™ 应用。SEL 控制引脚可在两个差动通道（端口 B 到端口 A 或端口 C 到端口 A）之间切换。

HD3SS3212-Q1 是一款通用的模拟差动无源开关。该器件适用于任何要求 0V 至 2V 共模电压范围和差动振幅高达 1800mVpp 的差动信号的高速接口应用。自适应跟踪功能可确保通道在整个共模电压范围内保持不变。

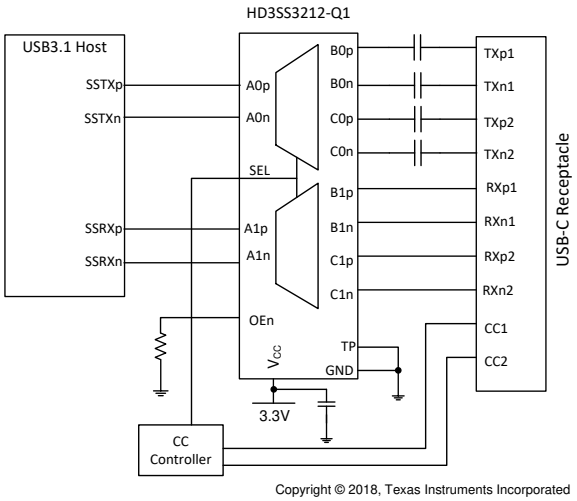
该器件的出色动态特性允许进行高速开关，使信号眼图具有最小的衰减，并且不会明显增加抖动。它在运行时消耗的功率低于 1.65mW。OEn 引脚具有关断模式，从而可实现低于 0.02µW 的功耗。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
HD3SS3212-Q1	VQFN (20)	2.50mm × 4.50mm × 0.5mm 间距

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

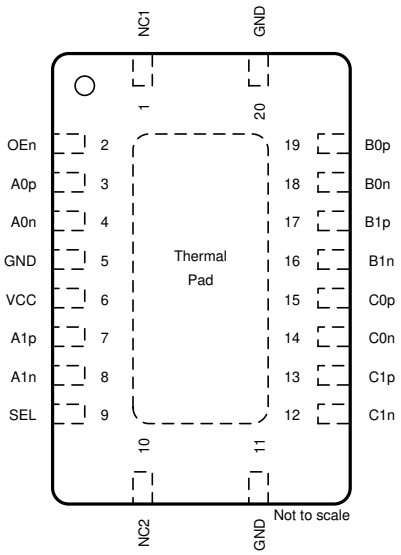
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2018) to Revision A	Page
• 将文档从*预告信息* 更改为*生产* 数据	1

5 Pin Configuration and Functions

RKS Package
20-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CC}	6	P	3.3-V power
OEn	2	I	Active-low chip enable L: Normal operation H: Shutdown
A0p	3	I/O	Port A, channel 0, high-speed positive signal
A0n	4	I/O	Port A, channel 0, high-speed negative signal
GND	5, 11, 20	G	Ground
A1p	7	I/O	Port A, channel 1, high-speed positive signal
A1n	8	I/O	Port A, channel 1, high-speed negative signal
SEL	9	I	Port select pin. L: Port A to Port B H: Port A to Port C
C1n	12	I/O	Port C, channel 1, high-speed negative signal (connector side)
C1p	13	I/O	Port C, channel 1, high-speed positive signal (connector side)
C0n	14	I/O	Port C, channel 0, high-speed negative signal (connector side)
C0p	15	I/O	Port C, channel 0, high-speed positive signal (connector side)
B1n	16	I/O	Port B, channel 1, high-speed negative signal (connector side)
B1p	17	I/O	Port B, channel 1, high-speed positive signal (connector side)
B0n	18	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	19	I/O	Port B, channel 0, high-speed positive signal (connector side)
NC1	1	NA	Can be left not connected or can be fed to V_{CC} or tied to GND.
NC2	10	NA	

(1) The high-speed data ports incorporate 20-kΩ pulldown resistors that are switched in when a port is not selected and switched out when the port is selected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4	V
	Voltage	Differential I/O	–0.5	2.5	V
		Control pins	–0.5	V_{CC}+ 0.5	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100- 011 CDM ESD Classification Level C6	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{ih}	Input high voltage (SEL, OEn pins)		1.7	V_{CC}	V
V_{il}	Input low voltage (SEL, OEn pins)		–0.1	0.8	V
V_{diff}	High-speed signal pins differential voltage		0	1.8	V_{pp}
V_{cm}	High speed signal pins common mode voltage		0	2	V
T_A	Operating free-air/ambient temperature	HD3SS3212-Q1	-40	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		HD3SS3212-Q1 RKS (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.7	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	V_{CC} = 3.3 V, OEn = 0		0.5	0.8	mA
I_{STDN}	Device shutdown current	V_{CC} = 3.3 V, OEn = V_{CC}		0.005	1	µA
C_{ON}	Output ON capacitance to GND			0.6		pF
C_{OFF}	Output OFF capacitance to GND			0.8		pF
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_{CM} = 0 to 2 V; I_O = –8 mA		5	8	Ω
ΔR_{ON}	On-resistance match between pairs of the same channel	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN)	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V			1	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, OEn)				1	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, OEn)				1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for selected port, A and B with SEL = 0, and A and C with SEL = V_{CC}			1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for non-selected port, C with SEL = 0, and B with SEL = V_{CC} (1)		100	140	µA
$I_{IL,HS}$	Input low current, high-speed pins [Ax/Bx/Cx][p/n]				1	µA

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 0.3 MHz		-0.4		dB
		f = 0.625 MHz		-0.4		
		f = 2.5 GHz		-1		
		f = 4 GHz		-1.8		
		f = 5 GHz		-2.0		
BW	–3-dB bandwidth			9		GHz
R_L	Differential return loss	f = 0.3 MHz		-25		dB
		f = 2.5 GHz		-11		
		f = 4 GHz		-9		
		f = 5 GHz		-8		
O_{IRR}	Differential OFF isolation	f = 0.3 MHz		-75		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		-21		
		f = 5 GHz		-19		
X_{TALK}	Differential crosstalk	f = 0.3 MHz		-70		dB
		f = 2.5 GHz		-35		
		f = 4 GHz		-30		
		f = 5 GHz		-28		

6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay (see 图 3)	f > 1 GHz			80	ps
t_{SW_ON}	Switching time SEL-to-Switch ON (see 图 2)				0.5	µs
t_{SW_OFF}	Switching time SEL-to-Switch OFF (see 图 2)				0.5	µs
$t_{SW\_OEn\_ON}$	Switching time OEn-to-Switch ON				2	µs
$t_{SW\_OEn\_OFF}$	Switching time OEn-to-Switch OFF				0.1	µs
$t_{SK\_INTRA\_A0B0}$	Intra-pair output skew for path A0 to B0. (see 图 3)	Intra-pair Skew = P - N		4.5		ps
$t_{SK\_INTRA\_A0C0}$	Intra-pair output skew for path A0 to C0. (see 图 3)	Intra-pair Skew = P - N		1.25		ps
$t_{SK\_INTRA\_A1B1}$	Intra-pair output skew for path A1 to B1. (see 图 3)	Intra-pair Skew = P - N		-0.75		ps
$t_{SK\_INTRA\_A1C1}$	Intra-pair output skew for path A1 to C1. (see 图 3)	Intra-pair Skew = P - N		-4		ps
t_{SK_INTER}	Inter-pair output skew (see 图 3)				20	ps

7 Parameter Measurement Information

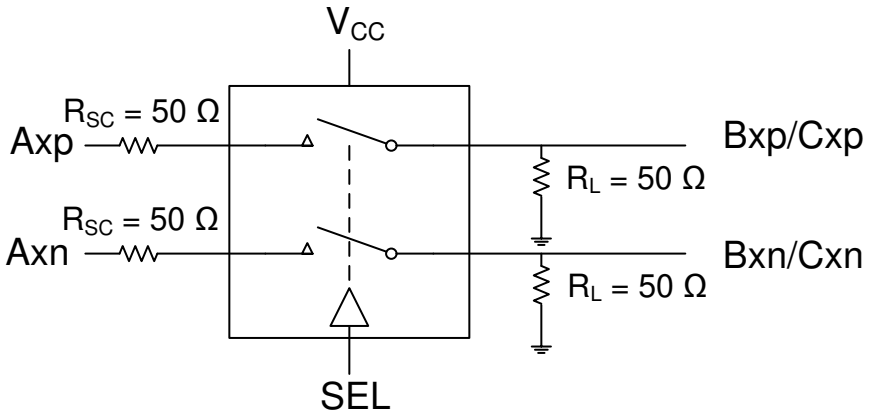


图 1. Test Setup

Parameter Measurement Information (接下页)

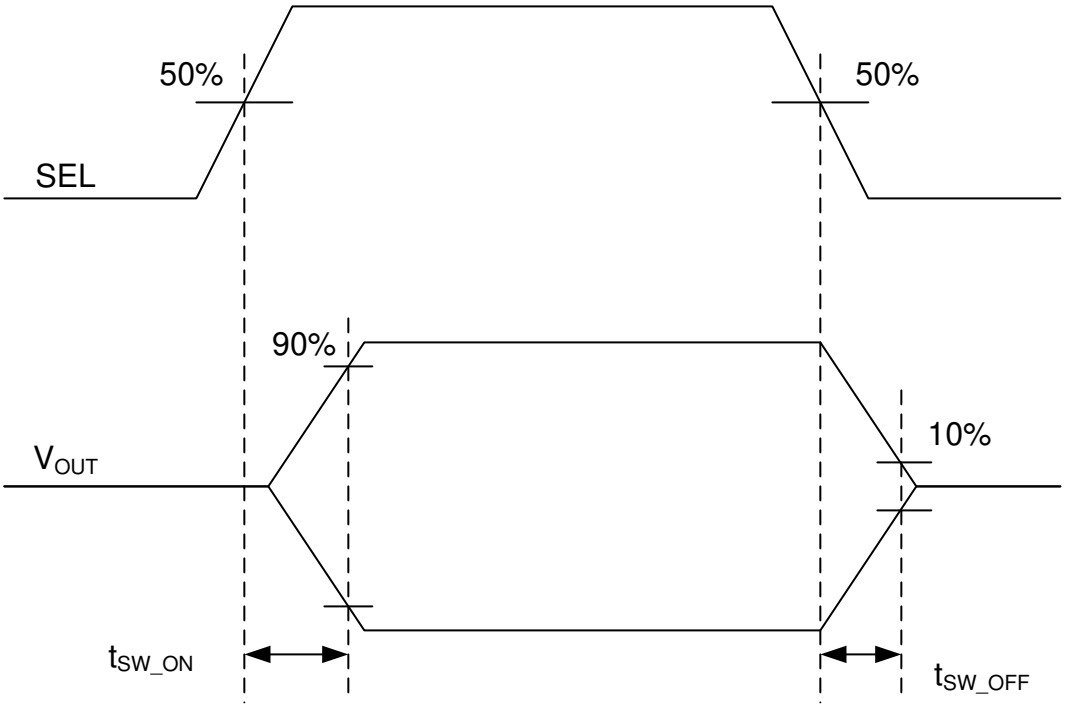


图 2. Switch On and Off Timing Diagram

Parameter Measurement Information (接下页)

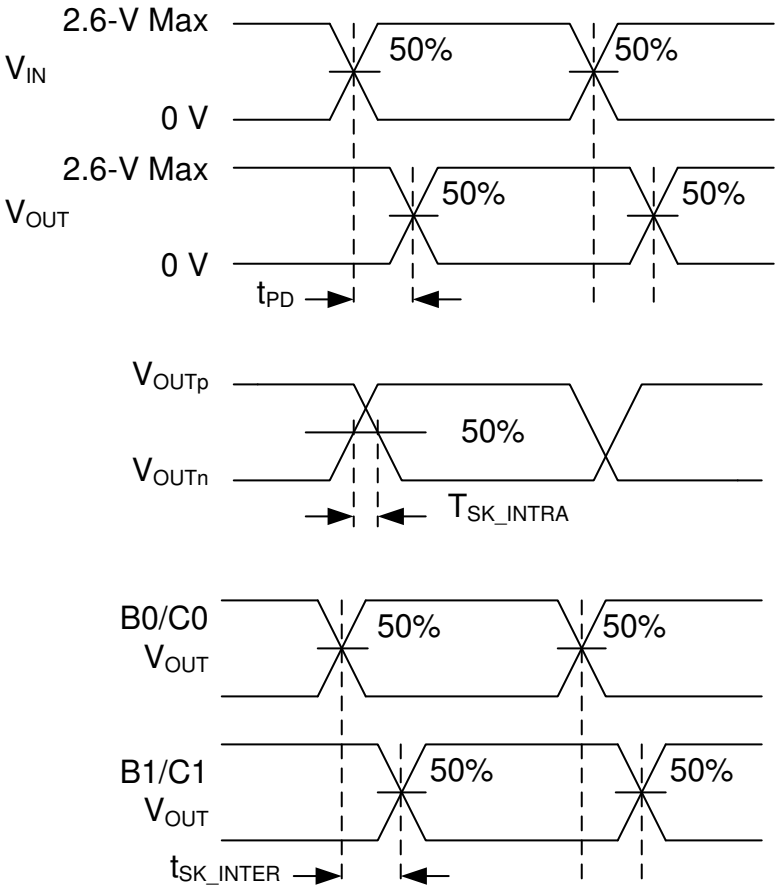


图 3. Timing Diagrams and Test Setup

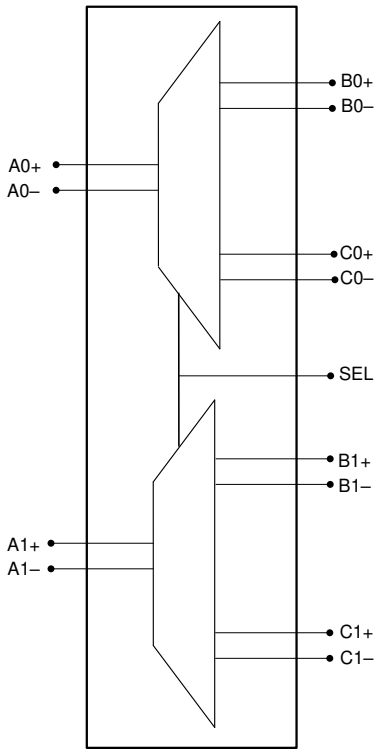
8 Detailed Description

8.1 Overview

The HD3SS3212-Q1 is a generic analog differential passive switch that can work for any high-speed interface applications requiring a common mode voltage range of 0 V to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range.

Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to the signal eye diagram with very little added jitter. It consumes less than 1.65 mW of power when operational and has a shutdown mode exercisable by OEn pin resulting less than 0.02 µW.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Enable and Power Savings

The HD3SS3212-Q1 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very-little current to save the maximum power. To enter standby mode, the OEn control pin is pulled high through a resistor and must remain high. For active/normal operation, the OEn control pin should be pulled low to GND or dynamically controlled to switch between H or L.

HD3SS3212-Q1 consumes < 1.65 mW of power when operational and has a shutdown mode exercisable by the EN pin resulting < 0.02 µW.

8.4 Device Functional Modes

表 1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

(1) The HD3SS3212 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Take care to ensure the same polarity is maintained on Port A versus Ports B/C.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The HD3SS3212-Q1 is a generic 2-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS3212-Q1 supports several high-speed data protocols with a differential amplitude of <1800 mVpp and a common mode voltage of <2.0 V, as with USB 3.2 and DisplayPort 1.4. The device's one select input (SEL) pin can easily be controlled by an available GPIO pin within a system or from a microcontroller.

The HD3SS3212-Q1 with its adaptive common mode tracking technology can support applications where the common mode is different between the RX and TX pair. The two USB 3.2 Type C connector applications show both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 capacitors are the preferred option to provide AC coupling; 0402 size capacitors also work. Avoid the 0603 or larger size capacitors and C-packs. When placing AC coupling capacitors, symmetric placement is best. The designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board.

The AC coupling capacitors have several placement options. Because the switch requires a bias voltage, the designer must place the capacitors on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. 图 4 shows a few placement options. The coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

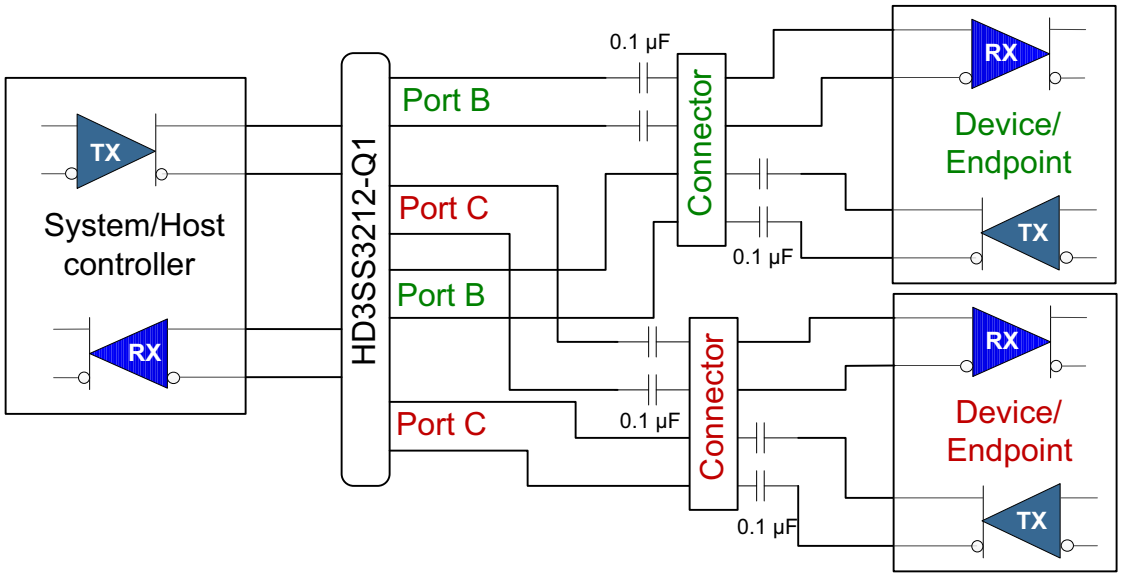


图 4. AC Coupling Capacitors between Switch TX and Endpoint TX

Application Information (接下页)

In 图 5, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on top is biased by the endpoint and the lower switch is biased by the host controller.

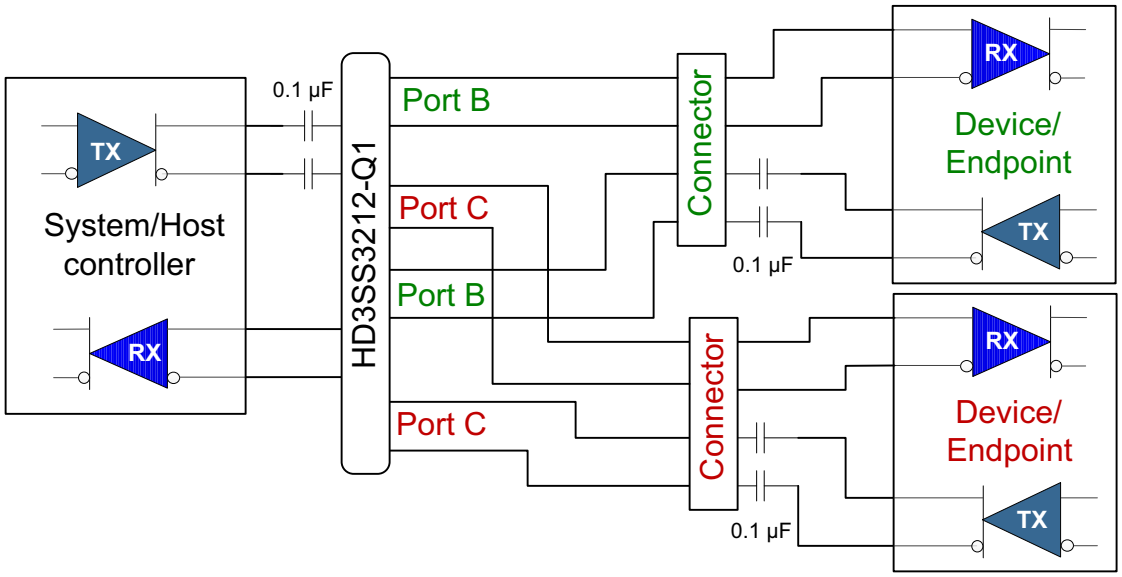
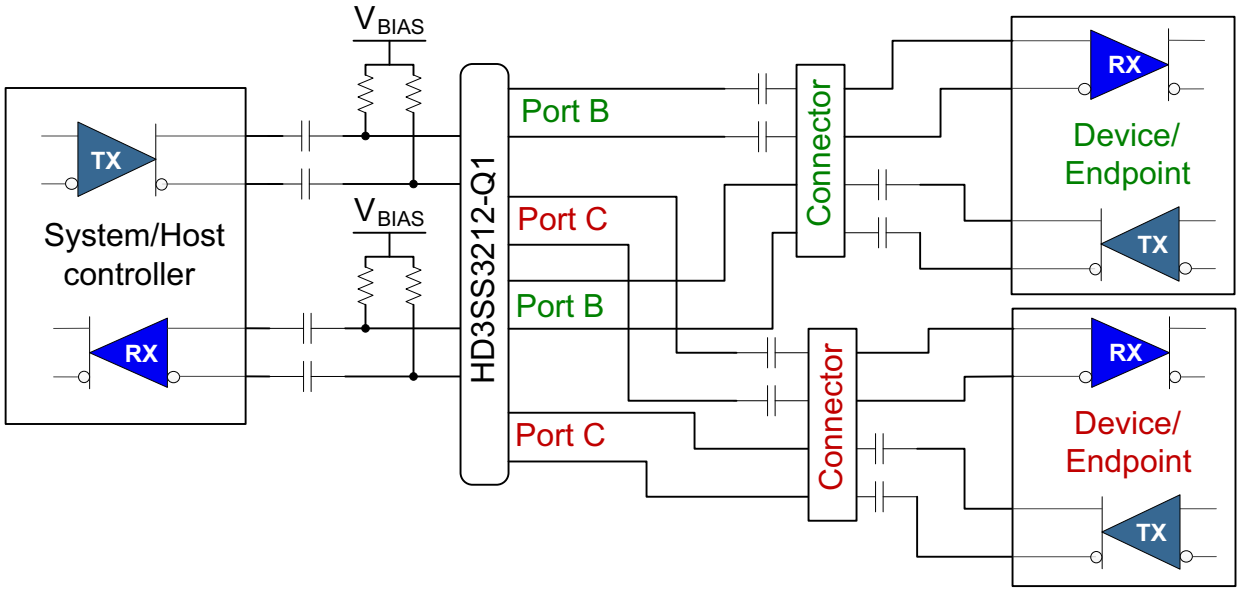


图 5. AC Coupling Capacitors on Host TX and Endpoint TX

If the common mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in 图 6). A biasing voltage of <2 V is required.



V_{BIAS} can be GND

Capacitor and resistor values depend upon application

图 6. AC Coupling Capacitors on Both Sides of Switch

Application Information (接下页)

The HD3SS3212-Q1 can be used with the USB Type C connector to support the connector's flip ability. 图 7 provides the generic location for the AC coupling capacitors for this application.

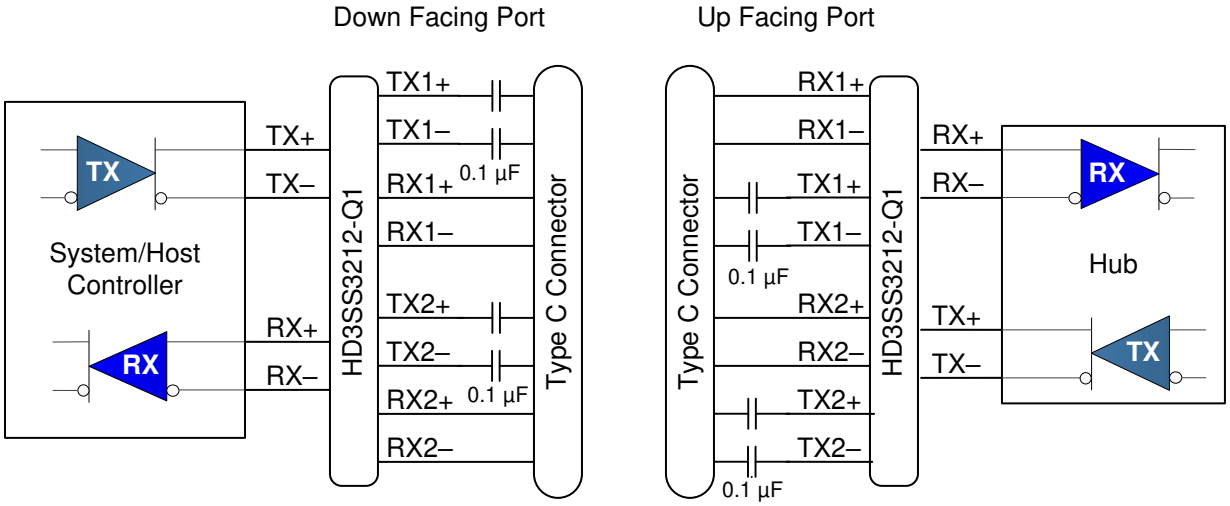


图 7. AC Coupling Capacitors for USB Type C

9.2 Typical Applications

9.2.1 Down Facing Port for USB3.1 Type C

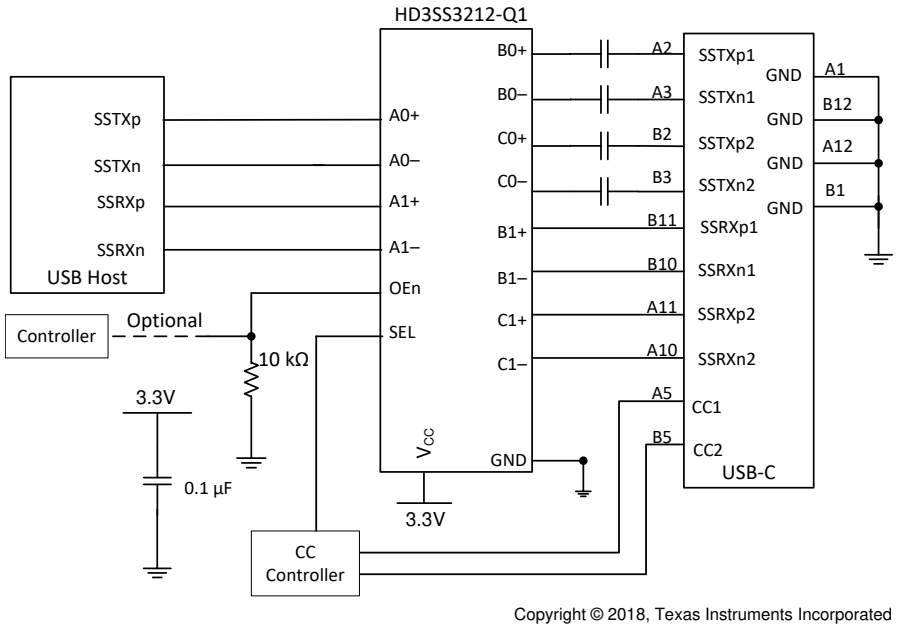


图 8. Down Facing Port for USB3.1 Type C Connector

9.2.1.1 Design Requirements

The HD3SS3212-Q1 can be designed into many different applications. All the applications have certain requirements for the system to work properly. The HD3SS3212-Q1 requires 3.3-V ±10% V_{CC} rail. The OEn pin must be low for device to work otherwise it disables the outputs. This pin can be driven by a processor. The expectation is that one side of the device has AC coupling capacitors. 表 2 provides information on expected values to perform properly.

表 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
AXp/n, BXp/n, CXp/n CM input voltage	0 V to 2 V
Control/OEn pin max voltage for low	0.8 V
Control/OEn pin min voltage for high	2.0 V
AC coupling capacitor	75 to 265 nF
R_{BIAS} (图 8) when needed	100 kΩ

9.2.1.2 Detailed Design Procedure

The HD3SS3212-Q1 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. The device can support 2 to 3 inches of board trace and a connector on either end.

To design in the HD3SS3212-Q1, the designer needs to understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Depending upon the application, determine the best place to put the AC coupling capacitor.
- Provide a control signal for the SEL and OEn pins.
- The thermal pad must be connected to ground.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground

9.2.1.3 Application Curves

图 9 and 图 11 shows the eye at the input of the HD3SS3212-Q1. 图 10 and 图 12 shows the eye at the output of the HD3SS3212-Q1.

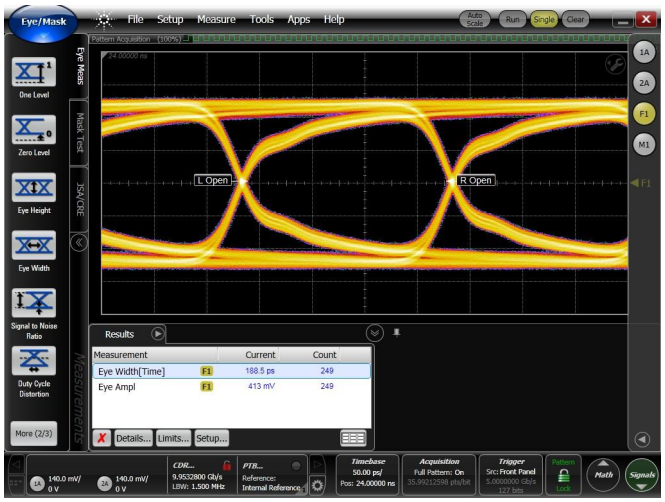


图 9. 5 Gbps Source Eye Diagram

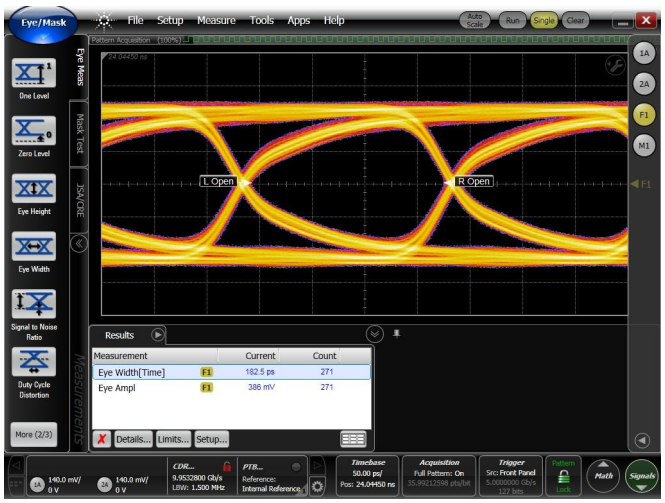


图 10. 5 Gbps Output Eye Diagram

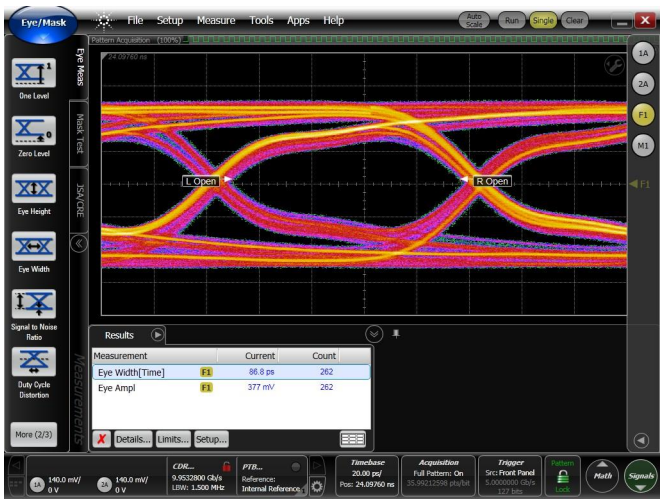


图 11. 10 Gbps Source Eye Diagram

图 12. 10 Gbps Output Eye Diagram

9.3 Systems Examples

9.3.1 Up Facing Port for USB 3.2 Type C

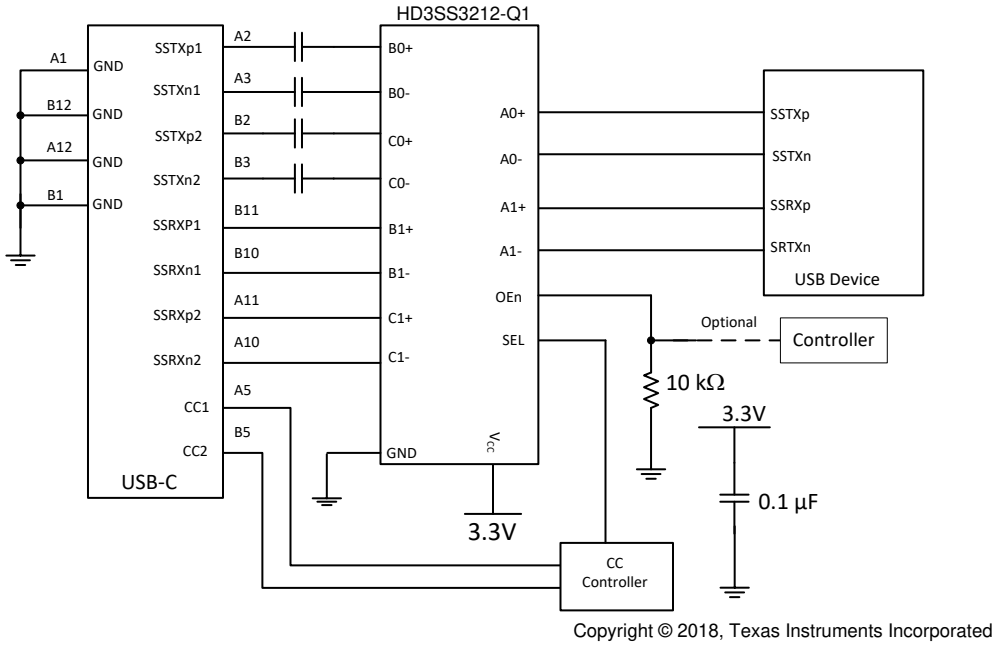


图 13. Up Facing Port for USB 3.2 USB Type-C Connector

9.3.2 PCIe/SATA/USB

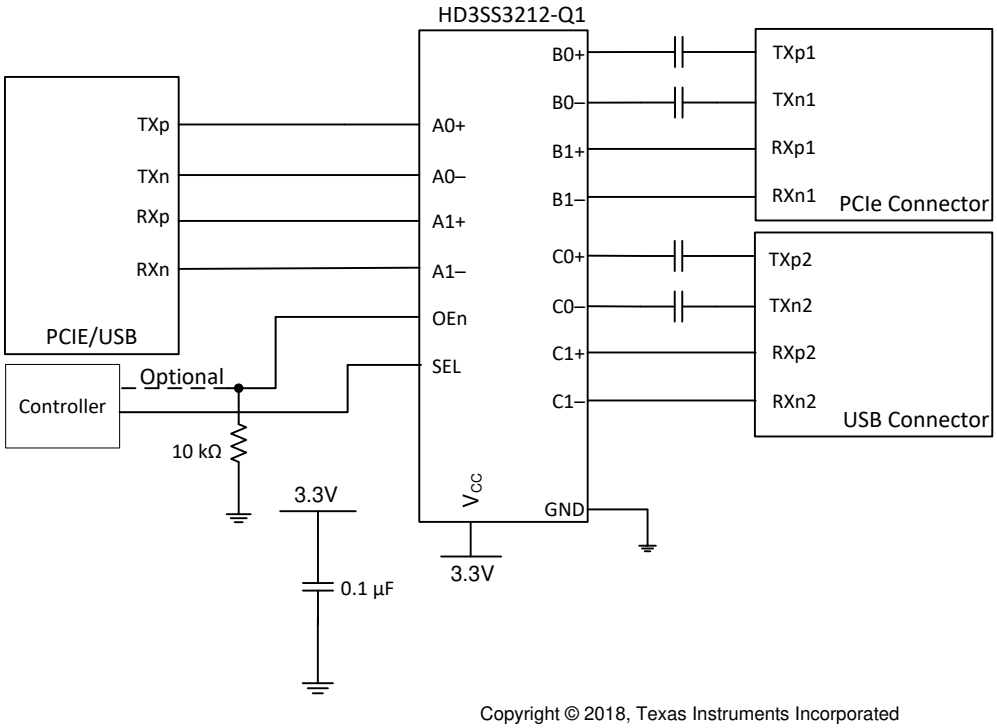


图 14. PCIE Motherboard

Systems Examples (接下页)

9.3.3 PCIE/eSATA

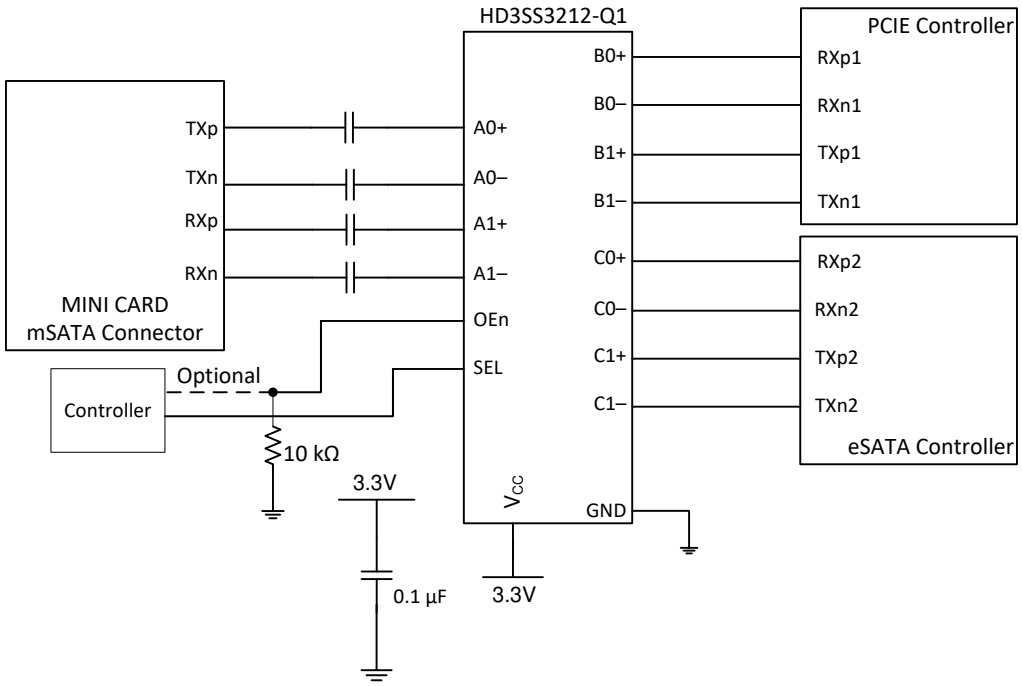


图 15. PCIe and eSATA Combo

9.3.4 USB/eSATA

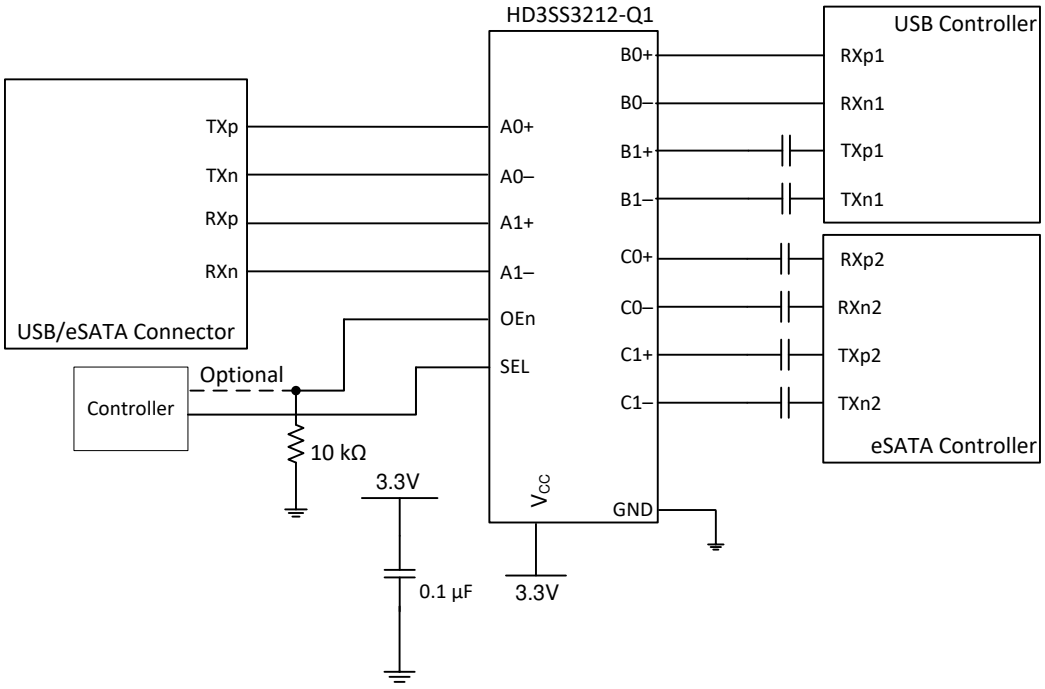


图 16. eSATA and USB 3.2 Combo Connector

10 Power Supply Recommendations

The HD3SS3212-Q1 does not require a power supply sequence. TI also recommends to place ample decoupling capacitors at the device V_{CC} near the pin.

11 Layout

11.1 Layout Guidelines

On a high-K board, TI always recommends to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the HD3SS3212-Q1 can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

On a low-K board, for the device to operate across the temperature range, the designer must use a 1-oz Cu trace connecting the GND pins to the thermal land. A general PCB design guide for PowerPAD packages is provided in *PowerPAD Thermally-Enhanced Package*, SLMA002.

11.2 Layout Example

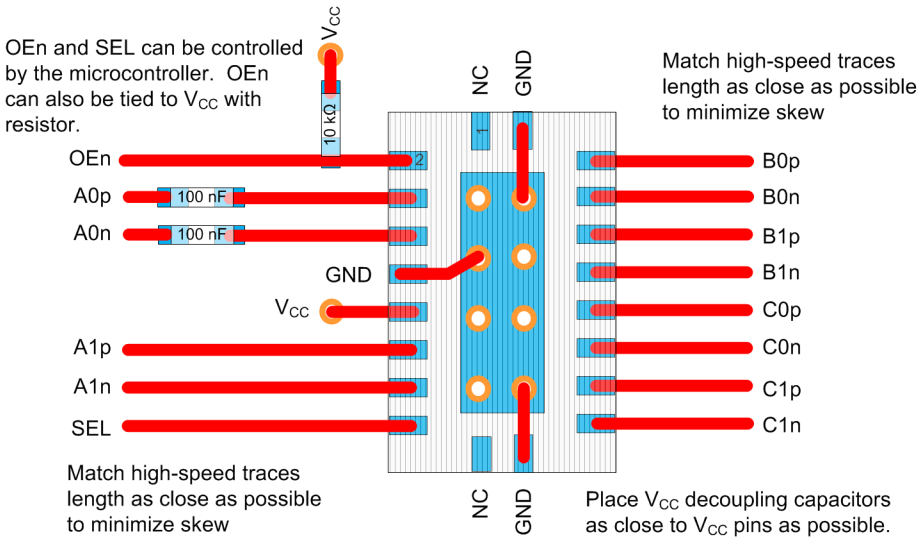


图 17. HD3SS3212-Q1 Basic Layout Example for Application Shown in *Down Facing Port for USB3.1 Type C*

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请转至 TI.com.cn 上您的器件的产品文件夹。请在右上角单击*通知我* 按钮进行注册，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

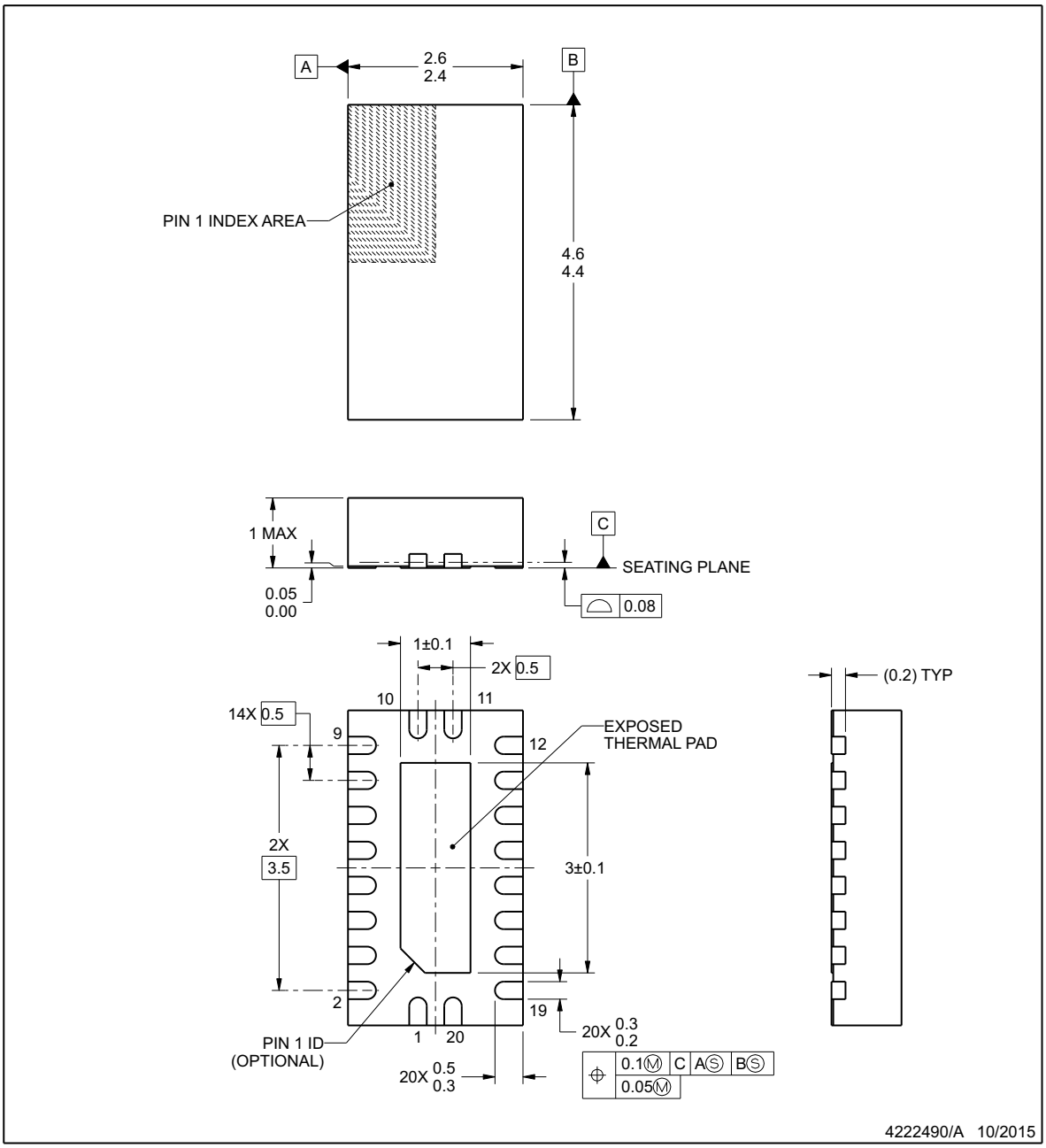
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

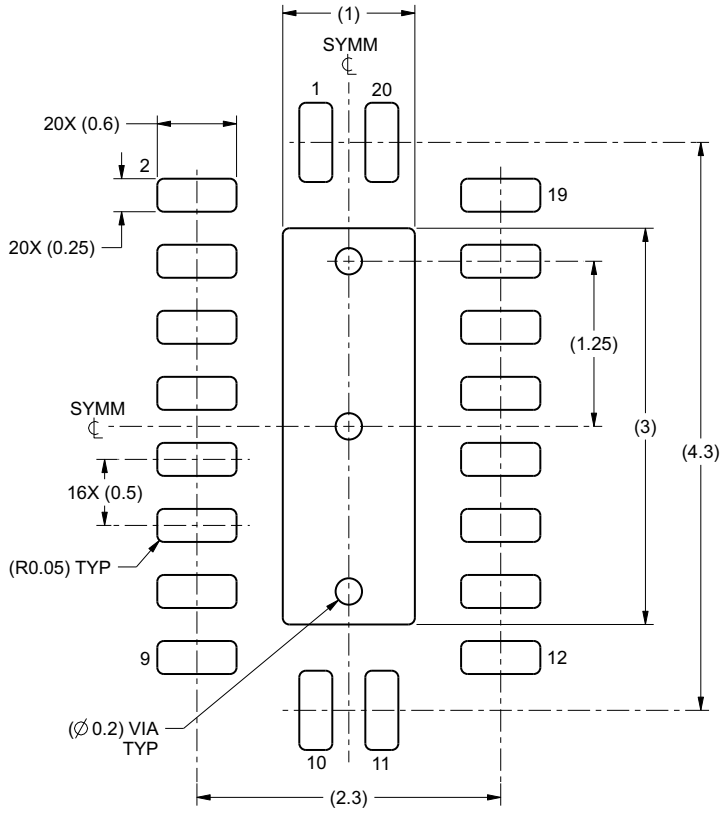
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

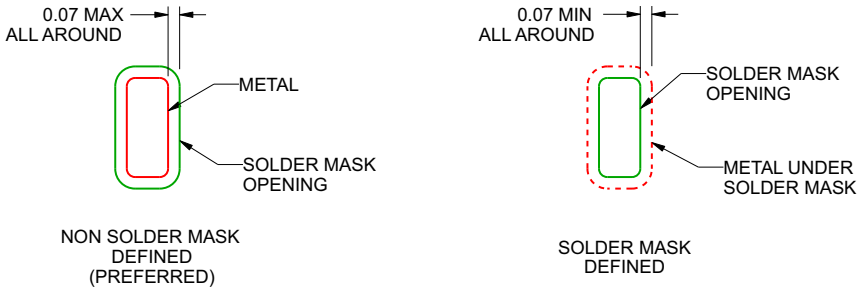
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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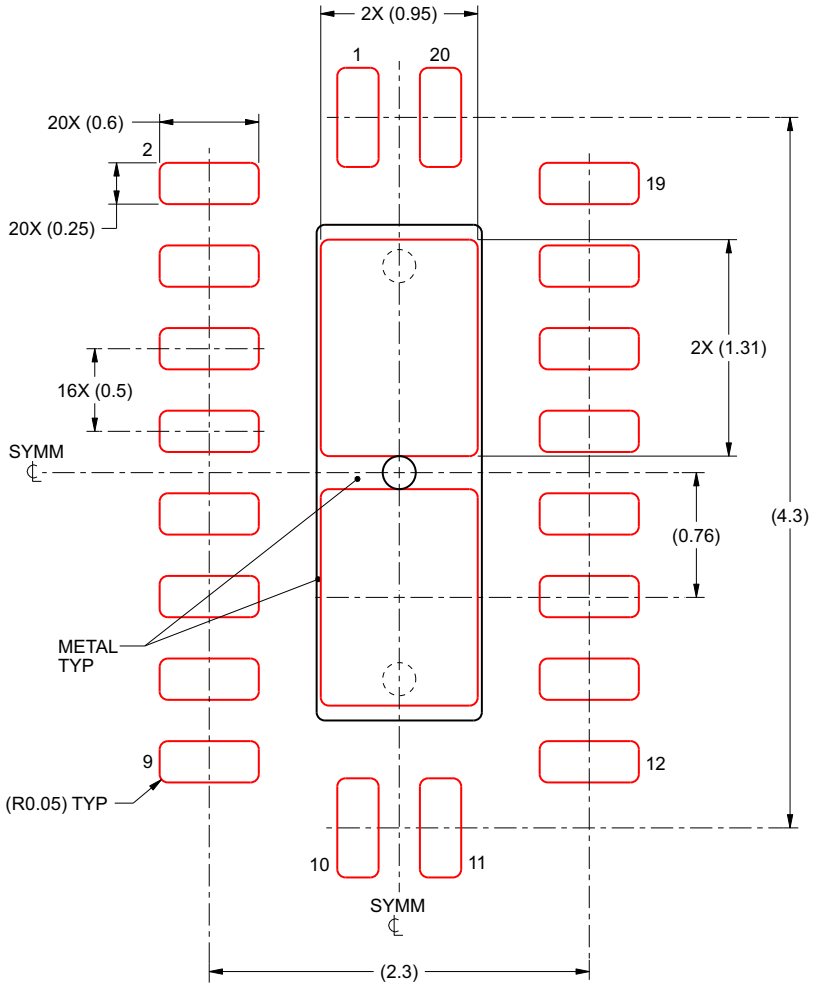
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS3212RKSRQ1	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HD3212Q	Samples
HD3SS3212RKSTQ1	ACTIVE	VQFN	RKS	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HD3212Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

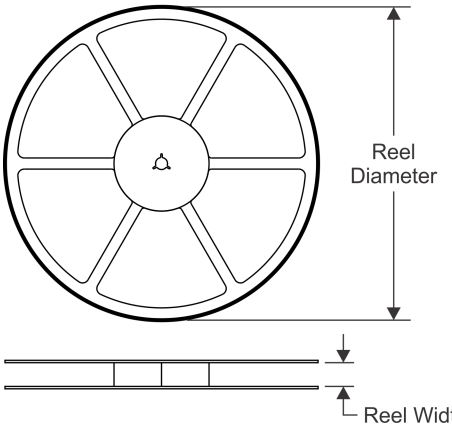
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

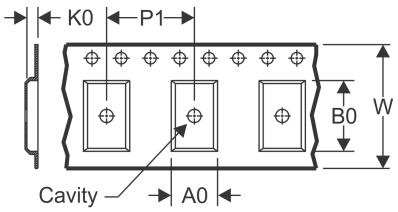
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

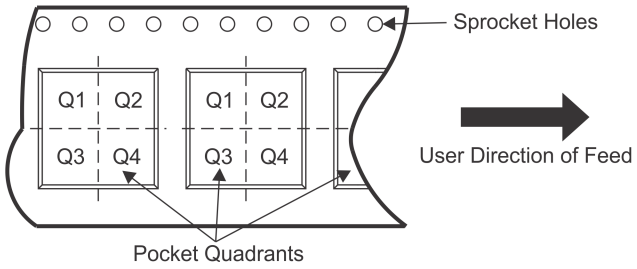


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

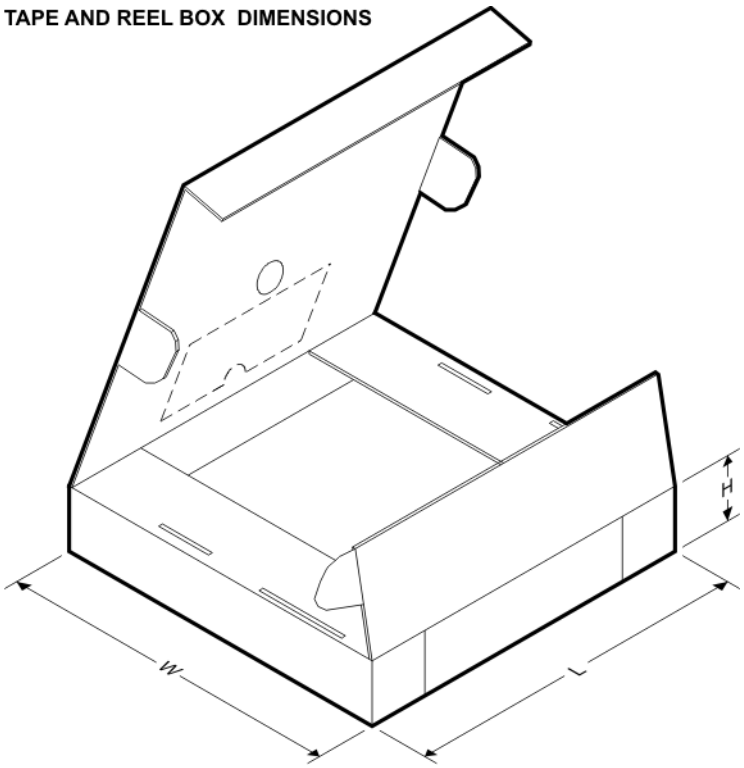
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3212RKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
HD3SS3212RKSTQ1	VQFN	RKS	20	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3212RKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0
HD3SS3212RKSTQ1	VQFN	RKS	20	250	210.0	185.0	35.0

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