

采用小型封装、具有 $\pm 15\text{kV}$ IEC ESD 保护的 TRS3221E 3V 至 5.5V 单通道 RS-232 线路驱动器/接收器

1 特性

- 为 RS-232 引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模型 (HBM)
 - $\pm 8\text{kV}$ (IEC 61000-4-2, 接触放电)
 - $\pm 15\text{kV}$ (IEC 61000-4-2, 空气间隙放电)
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 250kbit/s
- 一个驱动器和一个接收器
- 近似于芯片级封装, 16 引脚 VQFN (RGT, 比 TSSOP 封装小 82%)
- 低待机电流: $1\mu\text{A}$ (典型值)
- 外部电容器: $4 \times 0.1\mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 备选高速引脚兼容器件 (1Mbit/s)
 - TRSF3221E
- 自动断电功能可自动禁用驱动器以节省能耗

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

TRS3221E 是一个单驱动器、单接收器 RS-232 解决方案, 通过单个 V_{CC} 电源供电。RS-232 引脚提供 IEC G1000-4-2 ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。这些器件以高达 250kbit/s 的数据信号传输速率和最高为 $30\text{V}/\mu\text{s}$ 的驱动器输出压摆率运行。

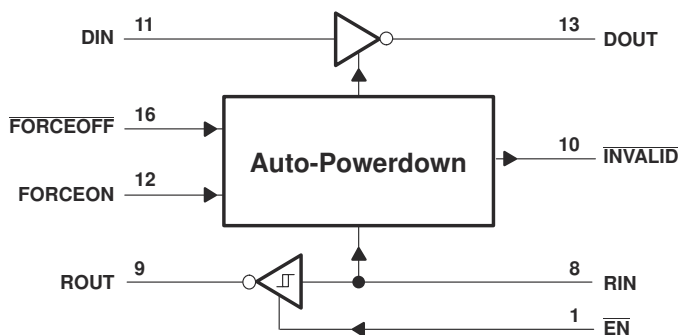
串行端口处于非活动状态时, 可提供灵活的电源管理控制选项。当 FORCEON 为低电平且 FORCEOFF 为高电平时, 自动断电功能启用。在这种运行模式下, 如果器件在接收器输入中未感应到有效的 RS-232 信号, 则禁用驱动器输出。如果 FORCEOFF 设定为低电平且 EN 为高电平, 则驱动器和接收器均关闭, 且电源电流降低至 $1\mu\text{A}$ 。断开串行端口的连接或关闭外围驱动器会导致发生自动断电情况。当 FORCEON 和 FORCEOFF 均为高电平时可禁用自动断电。

启用自动断电的情况下, 向接收器输入施加有效信号时, 器件会自动激活。 INVALID 输出会通知用户接收器输入中是否存在 RS-232 信号。如果接收器输入电压大于 2.7V 或小于 -2.7V, 或者介于 -0.3V 至 0.3V 之间的时间少于 $30\mu\text{s}$, 则 INVALID 为高电平 (有效数据)。如果接收器输入电压在 -0.3V 至 0.3V 之间的时间超过 $30\mu\text{s}$, 则 INVALID 为低电平 (无效数据)。有关接收器输入电平的信息, 请参阅图 7-5。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TRS3221E	SSOP (DB) (16)	6.20mm x 5.30mm
	TSSOP (PW) (16)	5.00mm x 4.40mm
	VQFN (RGT) (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2020) to Revision B (July 2021)	Page
• 更改了应用列表.....	1
• Changed the table note for the <i>ESD Ratings, IEC Specifications</i> to make it applicable to all packages.....	4
• Changed the thermal information for PW and DB packages.....	5

Changes from Revision * (June 2007) to Revision A (December 2020)	Page
• 添加了 <i>ESD 等级、IEC 规格表、热性能信息表、典型特性部分、详细描述部分、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分</i>	1
• 删除了 <i>订购信息表</i>	1
• Added the RGT (VQFN-16) package pinout	3
• Added data rate and $t_{sk(p)}$ rows for the RGT package in <i>Driver Section Switching Characteristics</i> table	6
• Added t_{pLH} , t_{pHL} , $t_{sk(p)}$ rows for the RGT package in <i>Receiver Section Switching Characteristics</i> table	7

5 Pin Configuration and Functions

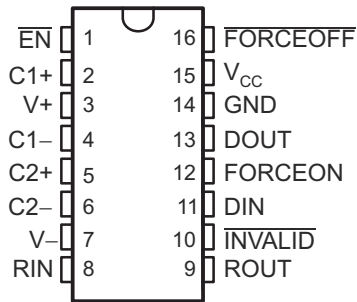


图 5-1. 16-Pin SSOP (DB) or TSSOP (PW) Packages, Top View

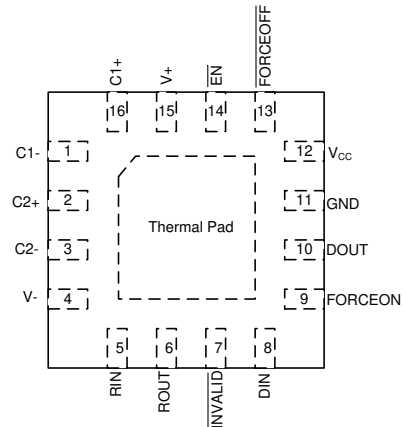


图 5-2. 16-pin VQFN (RGT) Package, Top View

表 5-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	DB or PW	RGT		
C1+	2	16	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5	2	—	
C1-	4	1	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2-	6	3	—	
DIN	11	8	I	Driver input
DOUT	13	10	O	RS-232 driver output
EN	1	14	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
FORCEOFF	16	13	I	Automatic power-down control input
FORCEON	12	9	I	Automatic power-down control input
GND	14	11	GND	Ground
INVALID	10	7	O	Invalid output pin. Output is low when all RIN inputs are unpowered.
RIN	8	5	I	RS-232 receiver input
ROUT	9	6	O	Receiver output
V _{CC}	15	12	—	3-V to 5.5-V supply voltage
V+	3	15	O	5.5-V supply generated by the charge pump
V-	7	4	O	- 5.5-V supply generated by the charge pump
Thermal Pad	None	Thermal Pad	-	Exposed thermal pad. Can be connected to GND or left floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	- 0.3	6	V	
V+	Positive output supply voltage range ⁽²⁾	- 0.3	7	V	
V-	Negative output supply voltage range ⁽²⁾	0.3	- 7	V	
V+ - V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage range	DIN, FORCEOFF, FORCEON, EN	- 0.3	6	V
		RIN	- 25	25	
V _O	Output voltage range	DOUT	- 13.2	13.2	V
		ROUT, INVALID	- 0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature range	- 65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except RIN and DOUT	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	RIN and DOUT pins (RS232 ports)	±15000	
			All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings, IEC Specifications

NAME	TEST CONDITIONS	TYP	UNIT
R _{IN} , D _{OUT}	IEC 61000-4-2 Contact Discharge ⁽¹⁾	±8000	V
	IEC 61000-4-2 Air-Gap Discharge ⁽¹⁾	±15000	

- (1) A minimum of 1-μF capacitor is required between VCC and GND to meet the specified IEC ESD level

6.4 Recommended Operating Conditions

See [图 9-1](#), and note ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, \overline{EN}	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, \overline{EN}			0.8	V
V_I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0	5.5		V
V_I	Receiver input voltage		-25	25		V
T_A	Operating free-air temperature	TRS3221EC	0	70		°C
		TRS3221EI	-40	85		

(1) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2 - C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TRS3221E			UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	52.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	41.7	60.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	57.2	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	56.6	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON, \overline{EN}			±0.01	±1	μA
I_{CC}	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V_{CC}		0.3	1	mA
		Powered off	$V_{CC} = 3.3\text{ V}$ or 5 V , $T_A = 25^\circ\text{C}$ No load, FORCEOFF at GND		1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are C1 - C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2 - C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.7 Driver Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 9-1](#))

PARAMETER	TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = GND		5	5.4		V
V _{OL} Low-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = V _{CC}		- 5	- 5.4		V
I _{IH} High-level input current	V _I = V _{CC}			±0.01	±1	μ A
I _{IL} Low-level input current	V _I = GND			±0.01	±1	μ A
I _{OS} Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V,	V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V,	V _O = 0 V		±35	±60	
r _o Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ±2 V		300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μ A
		V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1 - C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

6.8 Driver Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 9-1](#))

PARAMETER	TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ, See 图 7-1	RGT package	250	500		kbit/s
		DB or PW package	150	250		
t _{sk(p)} Pulse skew ⁽²⁾	C _L = 1000 pF, R _L = 3 kΩ 图 7-2	RGT package		50		ns
		DB or PW package		100		
SR(tr) Slew rate, transition region (see 图 7-1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 pF to 1000 pF	6		30	V/ μ s
		C _L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C1 - C4 = 0.1 μ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at V_{CC} = 5 V ± 0.5 V.

6.9 Receiver Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current	EN = V _{CC}		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Receiver Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER		TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT	
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 7-3	RGT package	100	ns
			DB or PW package	150	
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 7-3	RGT package	125	ns
			DB or PW package	150	
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 7-4	200	ns	
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 7-4	200	ns	
t _{sk(p)}	Pulse skew ⁽²⁾	See Figure 7-3	RGT package	25	ns
			DB or PW package	50	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.11 Auto-Powerdown Section Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = - 1 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

6.12 Auto-Powerdown Section Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

6.13 Typical Characteristics

$V_{CC} = 3.3\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$ unless specified otherwise.

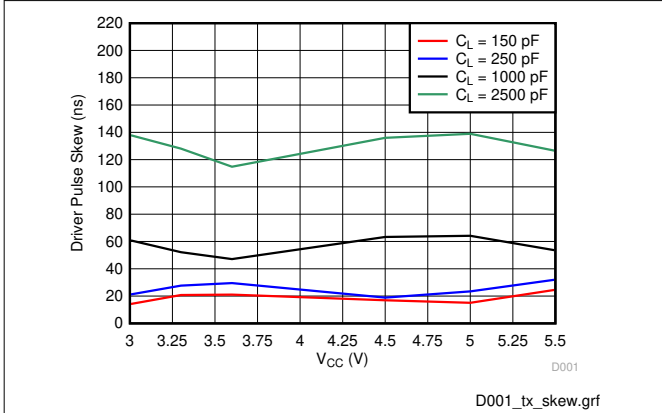


图 6-1. Driver Pulse Skew vs Load Capacitance and Supply Voltage at $T_A = 25\text{ }^\circ\text{C}$ (RGT Package)

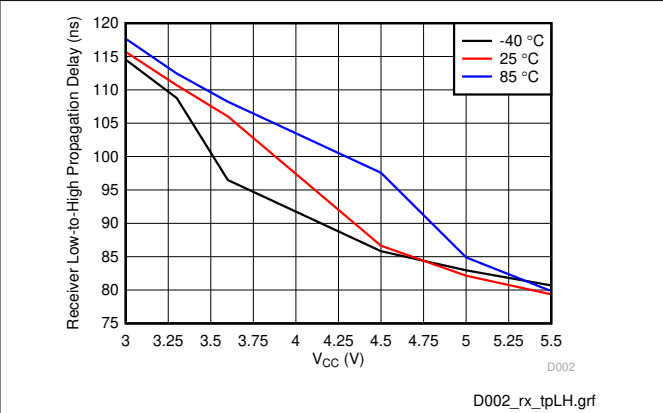


图 6-2. Receiver Path Low-to-High Propagation Delay vs T_A and Supply Voltage (RGT Package)

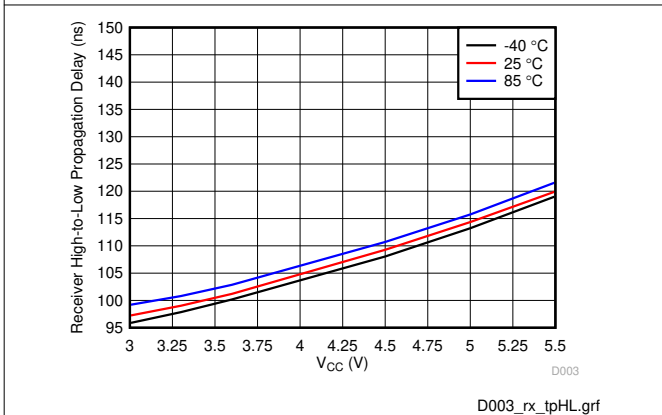


图 6-3. Receiver Path High-to-Low Propagation Delay vs T_A and Supply Voltage (RGT Package)

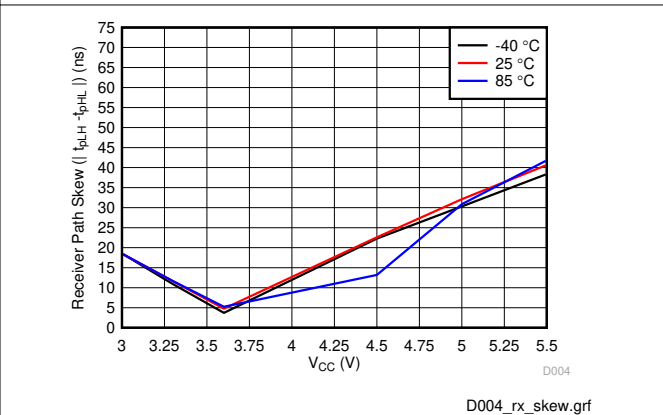
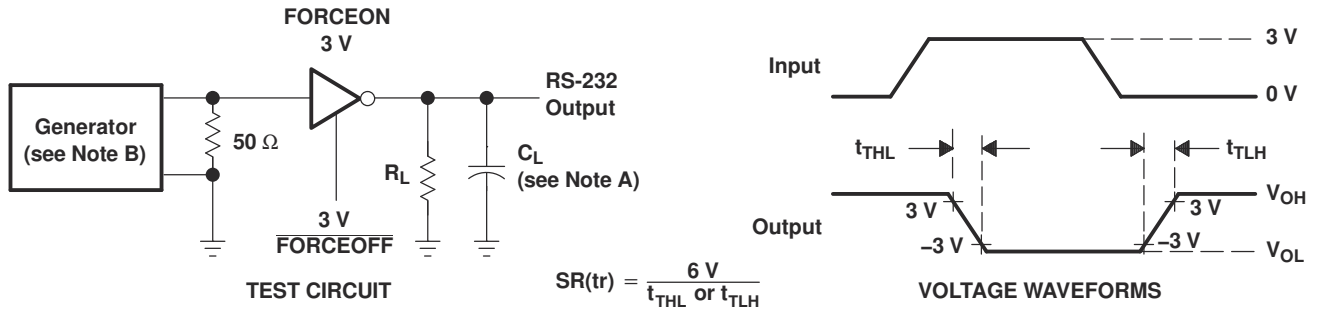


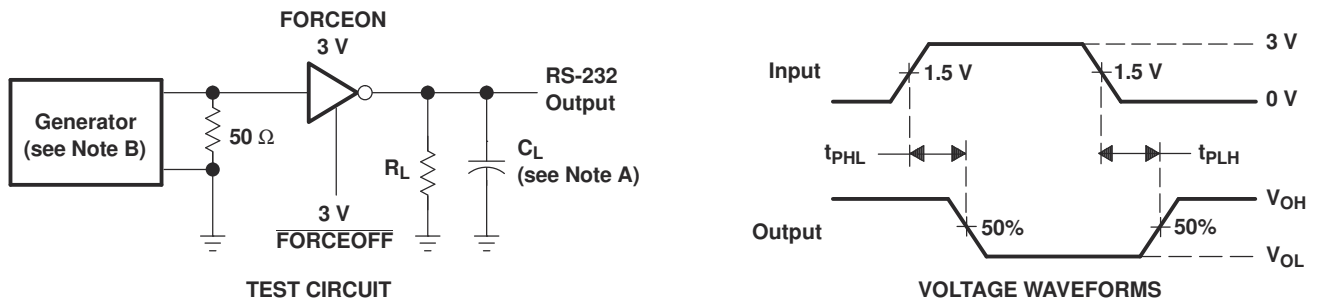
图 6-4. Receiver Pulse Skew ($|t_{pLH} - t_{pHL}|$) vs T_A and Supply Voltage (RGT Package)

7 Parameter Measurement Information



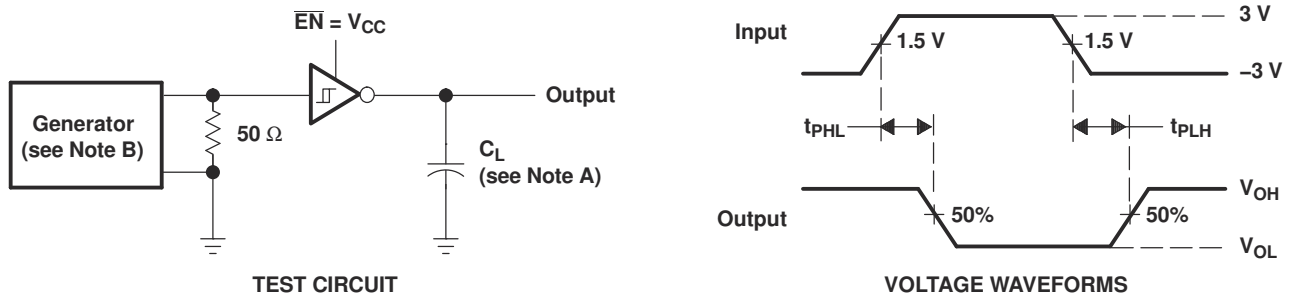
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-1. Driver Slew Rate



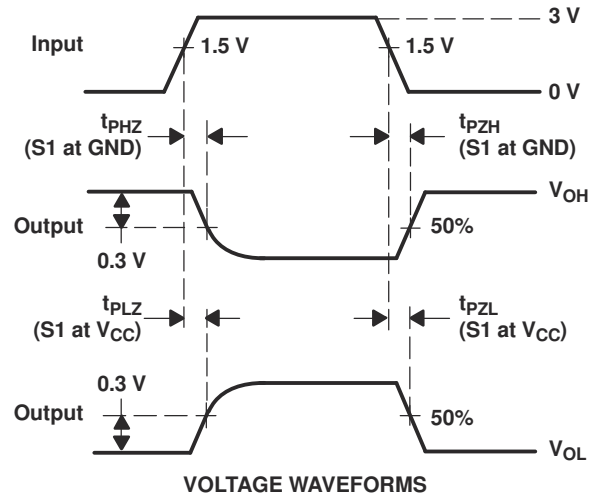
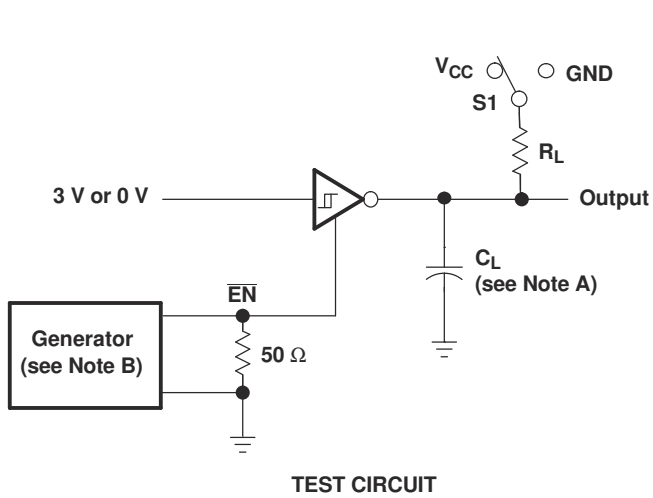
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-2. Driver Pulse Skew



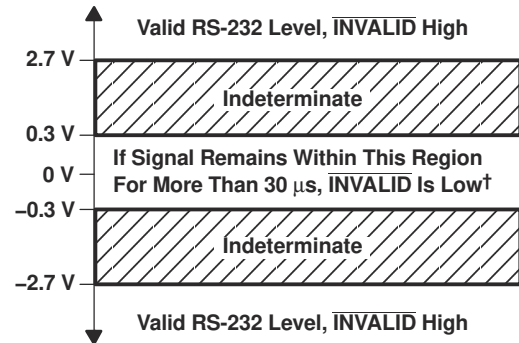
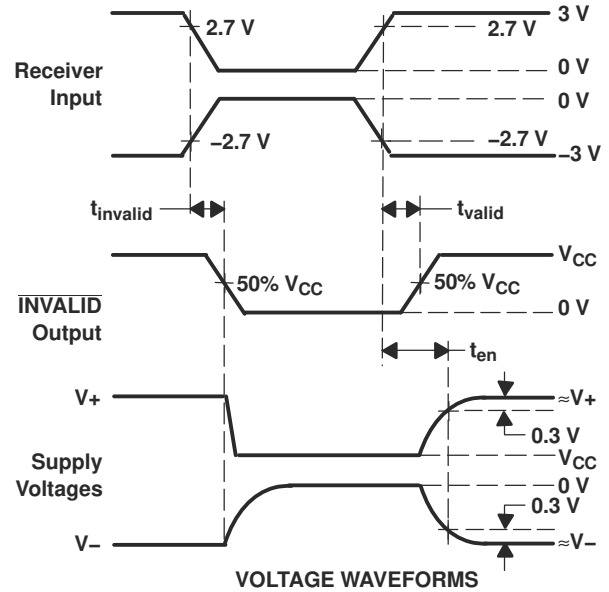
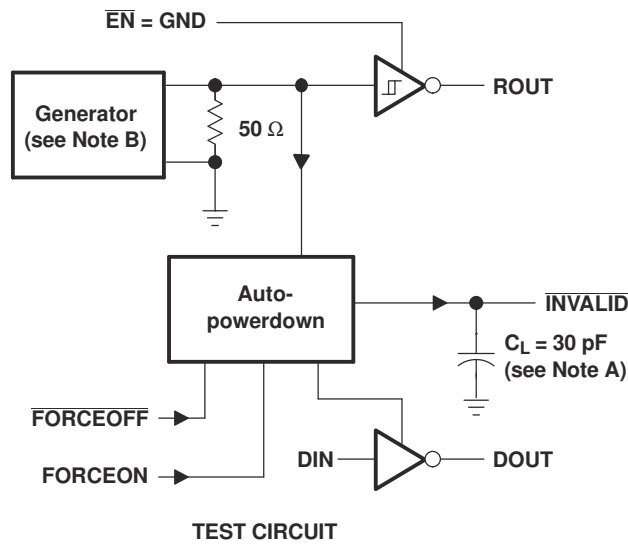
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-3. Receiver Propagation Delay Times



- NOTES:
- C_L includes probe and jig capacitance.
 - The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .

图 7-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

图 7-5. INVALID Propagation Delay Times and Driver Enabling Time

8 Detailed Description

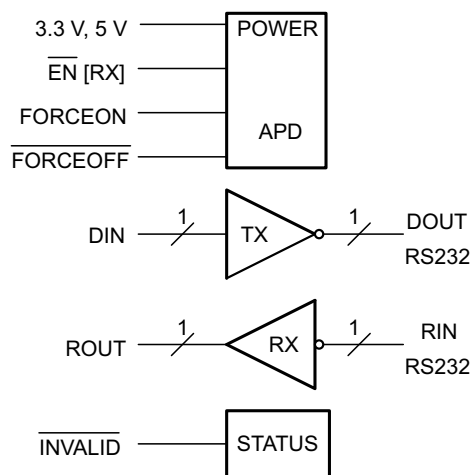
8.1 Overview

The TRS3221E device is a one-driver and one-receiver RS-232 interface device. The RS-232 input and output are protected up to ± 15 kV using the Human-Body Model. The charge pump requires only four small 0.1- μ F capacitors for operation from a 3.3-V supply. The TRS3221E device is capable of running at data rates up to 250 kbps while maintaining RS-232-compliant output levels.

Automatic power down can be disabled when $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ are high. With automatic power down plus enabled, the device activates automatically when a valid signal is applied to any receiver input. The device can automatically power down the driver to save power when the RIN input is unpowered.

$\overline{\text{INVALID}}$ is high (valid data) if receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. $\overline{\text{INVALID}}$ is low (invalid data) if receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to [Figure 7-5](#) for receiver input levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at $V+$ and $V-$ pins using a charge pump that requires four external capacitors. The automatic power-down feature for the driver is controlled by $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs. The receiver is controlled by the $\overline{\text{EN}}$ input (see [Table 8-1](#) and [Table 8-2](#)).

When the device is unpowered, it can be safely connected to an active remote RS232 device.

8.3.2 RS232 Driver

One driver interfaces standard logic level to RS232 levels. DIN input must be valid high or low.

8.3.3 RS232 Receiver

One receiver interfaces RS232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

8.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 μ s. The $\overline{\text{INVALID}}$ output goes high when the receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{CC} is powered regardless of $\overline{\text{FORCEON}}$ and $\overline{\text{FORCEOFF}}$ inputs (see [Table 8-3](#)).

8.4 Device Functional Modes

表 8-1. Driver

INPUTS ⁽¹⁾				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by automatic power-down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = |RIN| > 2.7 V, No = |RIN| < 0.3 V

表 8-2. Receiver

INPUTS ⁽¹⁾			OUTPUT	RECEIVER STATUS
RIN	EN	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 8-3. INVALID

INPUTS ⁽¹⁾				OUTPUT
RIN	FORCEON	FORCEOFF	EN	INVALID
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

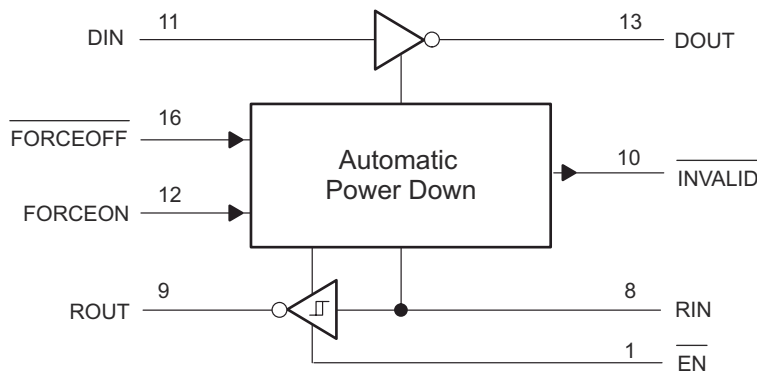


图 8-1. Logic Diagram

9 Application Information Disclaimer

Note

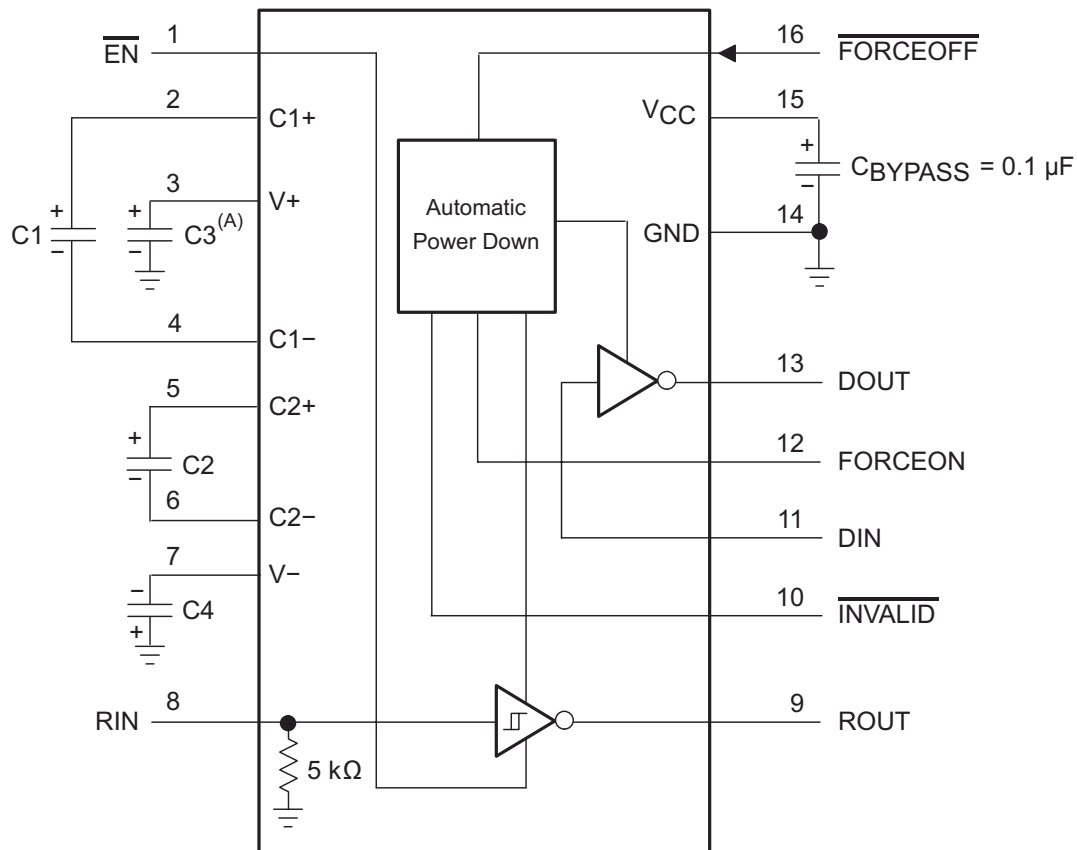
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9.1 Application Information

The TRS3221E device is designed to convert single-ended signals into RS232-compatible signals, and RS232-compatible signals into single-ended signals.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector

9.2 Typical Application



- A. C3 can be connected to V_{CC} or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.
- D. See [表 9-1](#) for capacitor values.

图 9-1. Typical Operating Circuit and Capacitor Values

9.3 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
 - 3 V to 5.5 V is also possible
 - Maximum recommended bit rate is 250 kbps
 - Use capacitors as shown in 图 9-1 and 表 9-1

表 9-1. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

9.4 Detailed Design Procedure

For proper operation, add capacitors as shown in 图 9-1 and 表 9-1.

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on V_{CC} level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC} . INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

9.5 Application Curve

V_{CC} of 3.3 V and 250 kbps alternative bit data stream

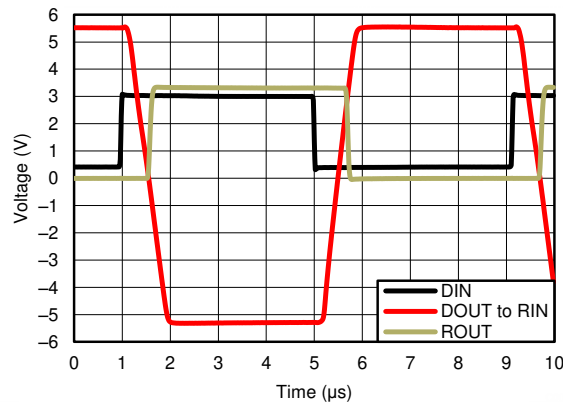


图 9-2. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC} = 3.3 V

Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using 表 9-1.

10 Layout

10.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

10.2 Layout Example

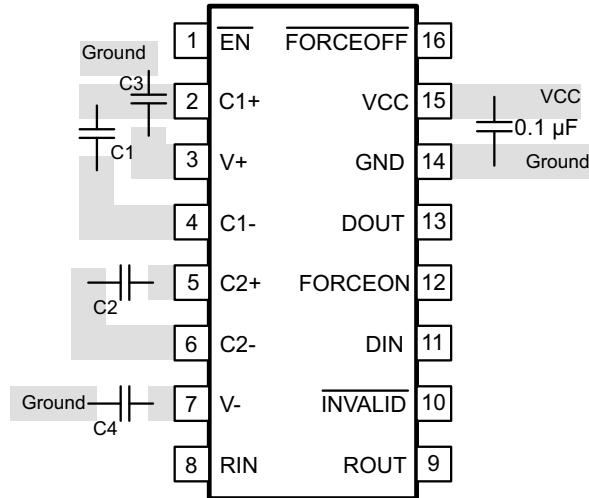


图 10-1. Layout Diagram

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 接收文档更新通知

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS21EC	Samples
TRS3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS21EC	Samples
TRS3221EIDB	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85	RS21EI	
TRS3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI	Samples
TRS3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS21EI	Samples
TRS3221EIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3221	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRS3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRS3221ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRS3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRS3221EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS3221EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

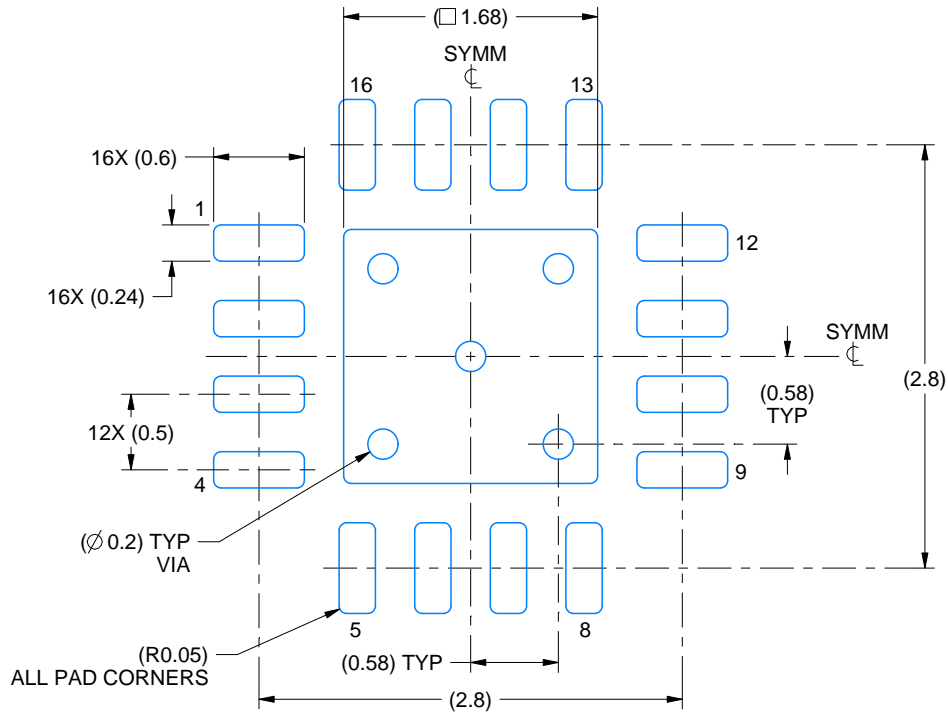
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

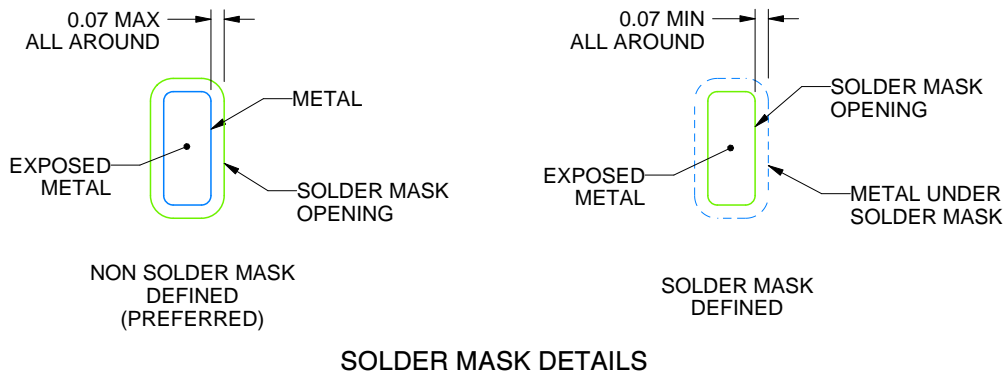
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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