设计指南：*TIDA-01013*

适用于 *DAQ* 和无线传感器物联网系统的低功耗、低噪声 *24* 位模拟前端参考设计

TEXAS INSTRUMENTS

说明

本模拟前端参考设计 具有 一个完整的低功耗和低噪声模拟前端 (AFE) 解决方案，适用于无线传感器物联网应用。通过将 TI 的单端 OPA191 缓冲器与 THS4451 (THS4561) 全差动运算放大器配合使用，此低功耗、低噪声解决方案能以极低功耗 (VLP) 模式驱动高精度 24 位 ADS127L01 ADC。TIDA-01013 AFE 和 ADC 系统具备 104dB 的信噪比 (SNR)，并且功耗仅为 40mW。

资源

TIDA-01013	设计文件夹
ADS127L01	产品文件夹
ADS127L01 EVM	产品文件夹
THS4551	产品文件夹
THS4561	产品文件夹
OPA191	产品文件夹
REF6030	产品文件夹
TPS560200	产品文件夹
LMR23610、LMK00804	产品文件夹
TPS79101、TPS79133	产品文件夹
TPS73118、TPS7A3001	产品文件夹

TI E2E™ Community 咨询我们的 E2E 专家

特性

- 适用于 24 位 Δ-Σ ADC DAQ 系统的低功耗、低噪声 AFE 设计
- 输入信号高达 ±10V
- SNR：104dB
- ENOB：19.1 位
- 功耗：41mW
- AFE 输出参考集成噪声：2.6μV$_{RMS}$

应用

- 数据采集 (DAQ)
- 仪表
- 半导体测试
- 物联网 (IoT)
- 传感器
- 智能工厂
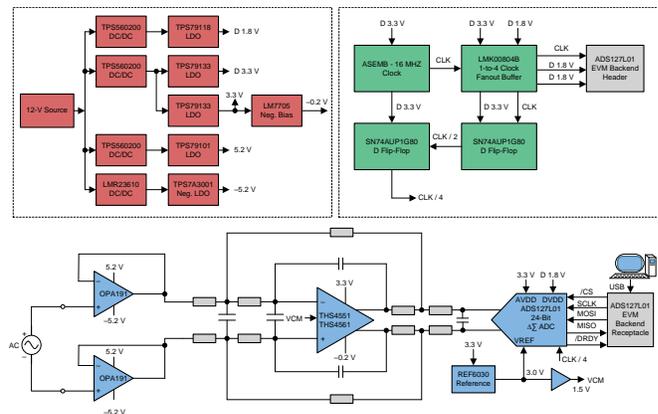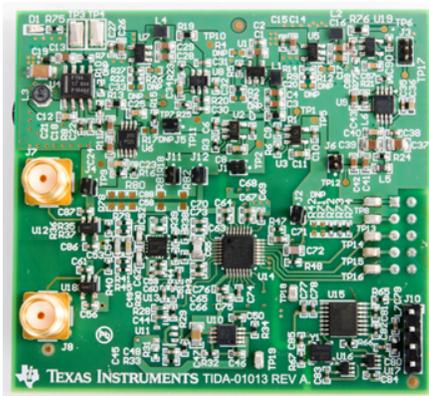
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1 System Description

The need for lower power, lower noise analog front ends (AFE) is becoming increasingly important in many applications today, such as data acquisition systems (DAQs), field instrumentation, Internet of Things (IoT), and automatic test equipment. In many cases, this need is highlighted by the advent of very high-resolution, low-noise, and low-power analog-to-digital converters (ADCs) like TI's 24-bit ADS127L01 Delta-Sigma ADC. These ADCs also need complimentary low-power, low-noise AFEs to support them. These new system solutions allow system designers to integrate a higher number of channels in data acquisition, wireless metering, and field instrumentation systems. The improved ADC and AFE design solutions also better support and improve numerous power sensitive IoT applications. This reference design demonstrates a complete low-power, low-noise AFE and ADC solution designed to support the power sensitive applications.

1.1 Key System Level Specifications

表 1. Key System Level Specifications

| PARAMETER	CONDITIONS	TARGET SPECIFICATION
Input range	—	±10 V fully-differential
Resolution	—	24 bits
ENOB	—	> 19 bits
System SNR	R_I = 3.4 kΩ	104 dB
System THD	R_I = 3.4 kΩ	80 dB
System power	AFE, ADC, voltage reference	40 mW
OPA191 buffer power	±10-V, 30-kHz input signal	< 13 mW
THS4551 FDA power	±10-V, 30-kHz input signal	< 10 mW
THS4561 FDA power	±10-V, 30-kHz input signal	< 9 mW
ADS127L01 power	125-kHz sampling frequency, VLP mode	< 16 mW

2 System Overview

2.1 Block Diagram
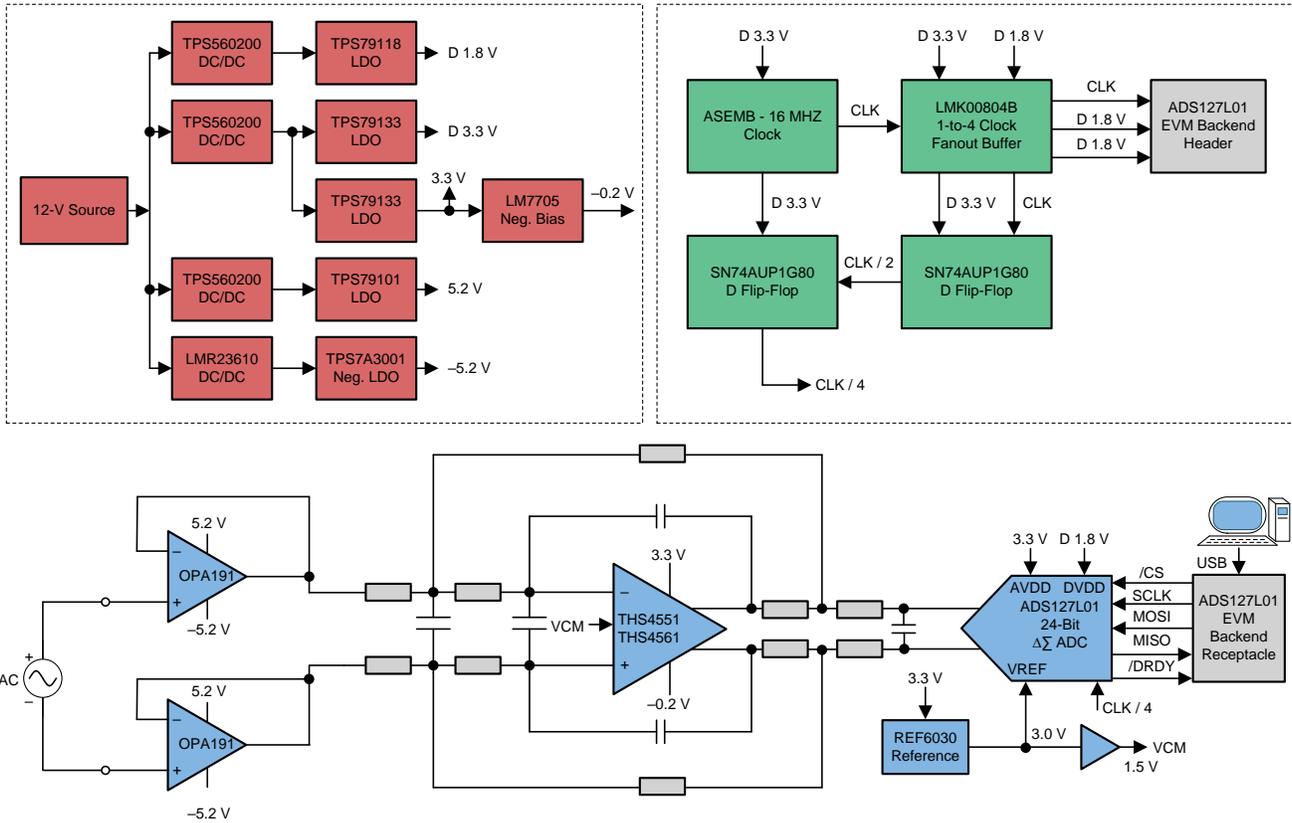
图 1. TIDA-01013 Block Diagram

2.2 *Highlighted Products*

This section covers the devices used in the TIDA-01013 reference design. For more information on each of these devices, see their respective product folders at TI.com.

2.2.1 OPA191

The OPA191 series of CMOS op-amps is a new generation of 36-V, e-trim™ op amps. These devices offer outstanding DC precision and AC performance, including rail-to-rail input/output, low-offset voltage (±5 μV, typical), low-offset drift (±0.2 μV/°C, typical), and 2-MHz bandwidth. The OPA191 also has a low broadband noise of 15 nV/√Hz at 1 kHz. Unique features such as differential input-voltage range to the supply rail, high-output current (±65 mA), high-capacitive load drive of up to 1 nF, and high slew rate (5 V/μs) make the OPA191 a robust, high-performance op-amp for high-voltage industrial applications.

Find the full device features and specifications at the OPA191 product folder.

2.2.2 THS4551

The THS4551 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well-suited for DAQs where high precision is required along with the best SNR and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging precision 16- to 24-bit delta-sigma ADC input requirements. A wide-range output common-mode control supports the ADC running from 1.8- to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

Find the full device features and specifications at the THS4551 product folder.

2.2.3 THS4561

The THS4561 fully differential amplifier (FDA) offers a simple interface from single-ended sources to the differential output required by high-precision analog-to-digital converters (ADCs). Designed for exceptional dc accuracy, low noise, and ultra-low harmonic distortion, the device is well suited for data acquisition systems where high precision is required with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4561 features the required negative rail input when interfacing a dc-coupled, ground-centered, source signal to a single-supply, differential-input ADC. Very low dc error and drift terms support the emerging 16-bit to 20-bit successive approximation register (SAR) input requirements. A 2.85-V to 12.6-V supply range with a flexible output common-mode setting with low headroom to the supplies supports a wide range of ADC input and digital-to-analog converter (DAC) output requirements.

Find the full device features and specifications at the THS4561 product folder.
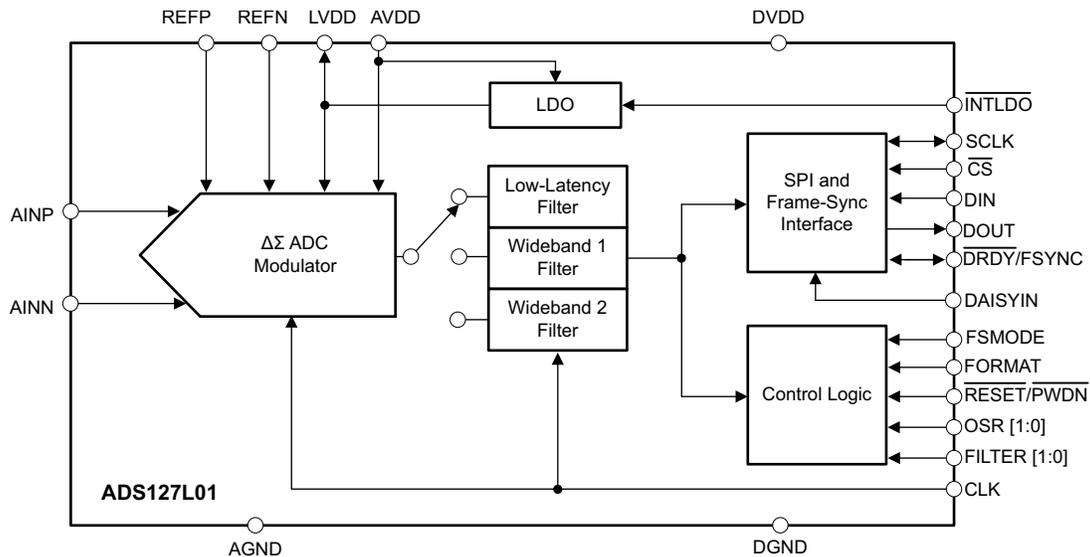
2.2.4   ADS127L01

图 **2. ADS127L01 Block Diagram**

The ADS127L01 is a 24-bit, delta-sigma ($\Delta\Sigma$), ADC with data rates up to 512 kSPS. This device offers a unique combination of excellent DC accuracy and outstanding AC performance. The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The integrated decimation filter suppresses modulator out-of-band noise. In addition to a low-latency filter, the ADS127L01 provides multiple wideband filters with less than ±0.00004 dB of ripple and an option for –116-dB stop-band attenuation at the Nyquist rate.

A variety of operating modes allow for optimization of speed, resolution, and power. A programmable serial interface with one of three options (SPI, frame-sync slave, or frame-sync master) provides convenient interfacing across isolation barriers to microcontrollers or digital signal processors (DSPs).

Find the full device features and specifications at the ADS127L01 product folder.

2.2.5   REF6030

The REF6030 voltage reference has an integrated low-output impedance buffer that enables the user to directly drive the REF pin of precision data converters while preserving linearity, distortion, and noise performance. Both precision SAR and delta-sigma ADCs switch sampling capacitors onto the reference input pin during the conversion process. To support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance, high-bandwidth buffer. The REF6030 device is well-suited, but not limited, to drive the reference input pin of the ADS88xx family of SAR ADCs, ADS127xx family of delta-sigma ADCs, as well as digital-to-analog converters (DACs).

The REF6030 voltage reference is able to maintain an output voltage within 1 LSB for an 18-bit converter with minimal voltage droop. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate DAQ systems. The REF60xx variants of the REF6000 family specify a maximum temperature drift of just 5 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low-output impedance buffer combined.

Find the full device features and specifications at the REF6030 product folder.

2.2.6   LMR23610

The LMR23610 SIMPLE SWITCHER® is an easy-to-use, 36-V, 1-A synchronous step-down regulator. With a wide input range from 4.5 to 36 V, it is suitable for various applications from industrial to automotive for power conditioning from unregulated sources. Peak current mode control is employed to achieve simple control loop compensation and cycle-by-cycle current limiting. A quiescent current of 75 μA makes it suitable for battery powered systems. An ultra-low 2-μA shutdown current can further prolong battery life. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This compensation also minimizes the external components. An extended family is available in 2.5-A (LMR23625) and 3-A (LMR23630) load current options in pin-to-pin compatible packages. A precision enable input simplifies regulator control and system power sequencing. Protection features include cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown due to excessive power dissipation.

Find the full device features and specifications at the LMR23610 product folder.

2.2.7   TPS7A3001

The TPS7A3001 is a negative, high-voltage (–36 V), ultra-low-noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A3001 of linear regulators is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

Find the full device features and specifications at the TPS7A3001 product folder.
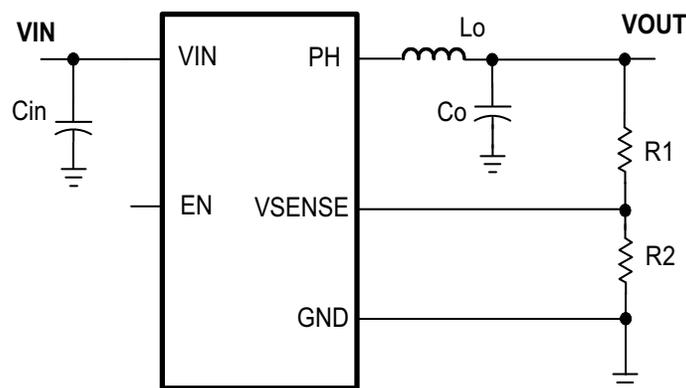
2.2.8   TPS560200

图 3. **TPS560200 Simplified Schematic**

The TPS560200 is an 17-V, 500-mA, low-I_Q, adaptive on-time, D-CAP2™ mode, synchronous monolithic buck converter with integrated MOSFETs in easy-to-use 5-pin SOT-23 package.

The TPS560200 lets system designers complete the suite of various end-equipment power bus regulators with a cost-effective, low-component count, and low-standby current solution. The main control loop for the device uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-Mode operation at light loads.

The TPS560200 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from a 4.5- to 17-V input (V_{IN}). The output voltage can be programmed between 0.8 V and 6.5 V. The device also features a fixed 2-ms soft-start time. The device is available in the 5-pin SOT-23 package.

Find the full device features and specifications at the TPS560200 product folder.

2.2.9   TPS79133

The TPS79133 is a low-dropout (LDO), low-power, linear voltage regulator that features high power supply rejection ratio (PSRR), ultra-low-noise, fast start-up, and excellent line and load transient responses in a small outline, SOT-23 package. This device is stable, with a small 1-mF ceramic capacitor on the output. The TPS79133 uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages. This device has a fast start-up time (approximately 63 ms with a 0.001-mF bypass capacitor) while consuming very low quiescent current (170 mA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 mA. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features as well as the fast response time.

Find the full device features and specifications at the TPS791 product folder.
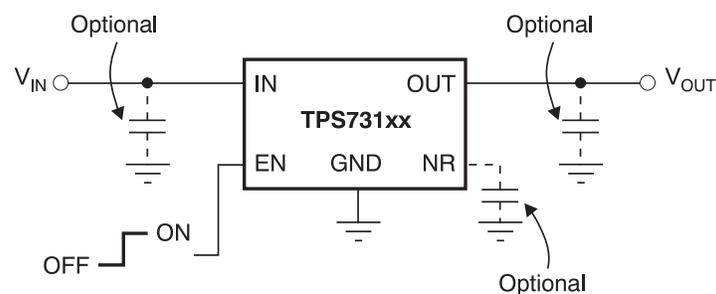
2.2.10   TPS73118

图 **4. TPS73118 Typical Application Circuit**

The TPS73118 LDO linear voltage regulator uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS73118 uses an advanced BiCMOS process to yield high precision while delivering very LDO voltages and low ground pin current. When not enabled, current consumption is less than 1 μA and ideal for portable applications. The extremely low-output noise (30 μV_{RMS} with 0.1-μF CNR) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Find the full device features and specifications at the TPS731 product folder.

2.2.11 LMK00804B
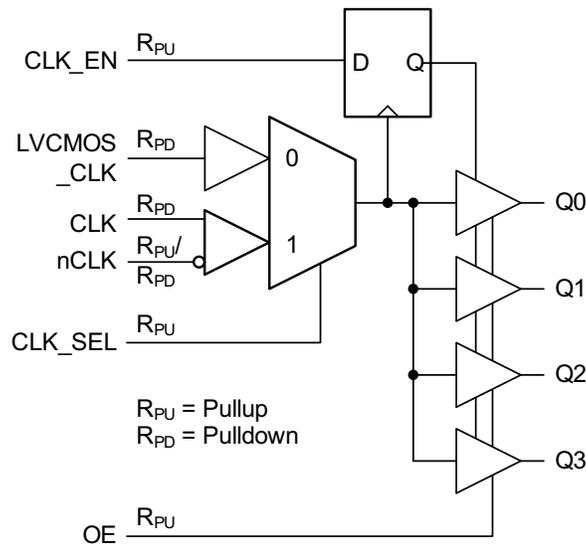
图 **5. LMK00804 Simplified Schematic**

The LMK00804B is a low-skew, high-performance clock fanout buffer that can distribute up to four LVCMOS or LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs, which can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or de-asserted. The outputs are held in logic low state when the clock is disabled. A separate output enable terminal controls whether the outputs are active state or high-impedance state. The low-additive jitter and phase noise floor, and guaranteed output and part-to-part skew characteristics make the LMK00804B ideal for applications demanding high performance and repeatability.

Find the full device features and specifications at the LMK00804B product folder.

2.3   System Design Theory

The primary goal of the TIDA-01013 reference design is to develop an AFE system for ±10-V, 30-kHz input signals. The system must feature a noise level that has insignificant impact to the ADS127L01 noise performance and overall power consumption.

An AFE design requires several components to operate effectively. They are the high-impedance input buffers, the fully-differential amplifier (FDA), the ADC, and the reference voltage (V_{REF}). The following sections detail the design considerations and challenges presented by this system design, including theory, calculations, component selection, simulations, and measurement results. TINA-TI™ and Cadence® Virtuoso® tools were used to aid in development.

2.3.1   High-Input Impedance Buffers

The first stage of the input chain is a buffer stage consisting of two OPA191s. The configuration for the OPA191 can be seen in 图 6 with the operational amplifiers (op amps) in a simple, non-inverting buffer configuration.
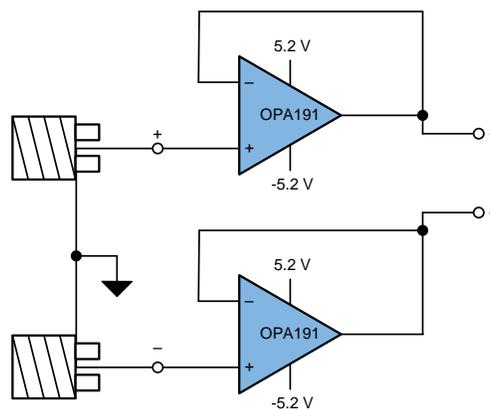

图 6. OPA191 Input Buffers

The purpose of this stage is to present a high input impedance to weak sensor outputs and drive them into the next signal conditioning stage. The OPA191 JFET input stage provides a high common-mode input impedance (Z_{IC}) of 10^{13} Ω and a differential input impedance (Z_{ID}) of 100 MΩ. In addition, this device also offers excellent low quiescent current of 140 µA per amplifier, broadband noise levels of 15 nV/√Hz, and suitable THD performance of 0.0012% (f = 1 kHz, G = 1 and Vo = 3.5 V_{RMS}). The maximum power rails are ±18 V, well beyond the signal of interest of ±10 V. Because the OPA191 is a rail-to-rail input/output amplifier, the power rails can be closer to the input signal without adding significant distortion in the buffered signal, thus reducing the overall power consumption. Power rails of ±5.2 V are selected because they offer improved THD performance. The gain-bandwidth product is 2.5 MHz, which is more than enough headroom for the 30-kHz signal of interest.

The slew rate (SR) of the OPA191 is 5 V/µs, which is used to calculate the maximum input signal frequency without experiencing slew-induced distortion. Slew rate limitation is dependent on the peak signal voltage (V_P) as well as the op-amp's SR figure of merit. The equation can be seen in 公式 1, where the maximum frequency is 112.5 kHz without SR limitations.

$$\frac{V_P}{\sqrt{2}} = \frac{SR}{(2 \times \pi \times f)} \tag{1}$$

Therefore:

$$f_{MAX} = \frac{SR \times \sqrt{2}}{(2 \times \pi \times V_P)}$$

$$f_{MAX} = \frac{5\ V/µs \times \sqrt{2}}{(2 \times \pi \times 10)} = 112.5\ kHz$$

图 7 highlights the schematic used to test the stability of the OPA191 buffer stage in TINA-TI. When measuring the stability of an amplifier, look at the closed-loop noise gain, loaded open-loop gain (Aol), and noise gain (1/β). The phase margin of the circuit needs to be sufficient at unity gain for circuit stability and required settling.
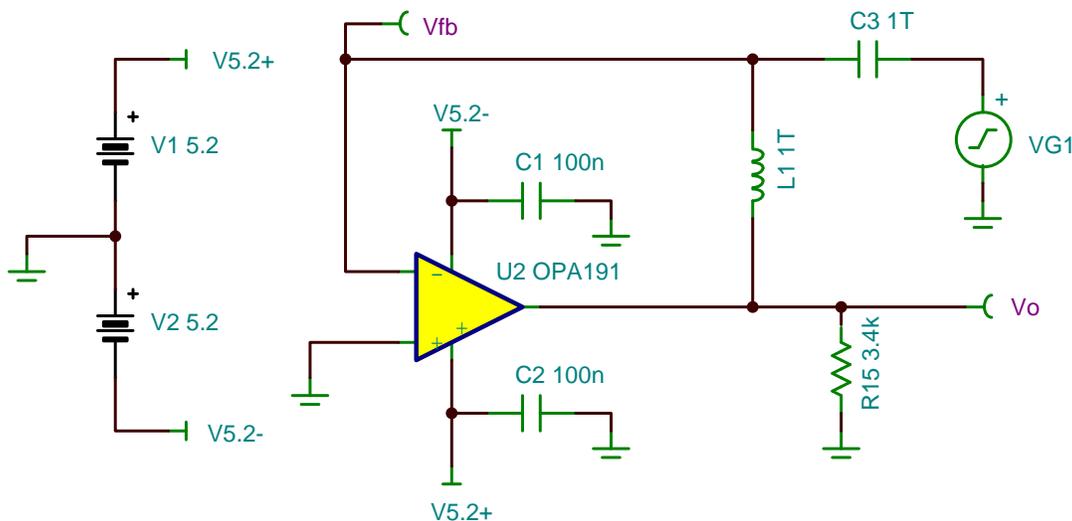

图 **7. OPA191 TINA-TI Stability Schematic**

The TINA-TI schematic in 图 7 includes a 1-TF capacitor and 1-TH inductor for simulation purposes. As the input frequency increases, the impedance of the inductor will increase and break the feedback loop of the amplifier. The capacitor is used to block the dc component of the input signal while providing a low-impedance path to the inverting amplifier input for ac signals. The approximate load the OPA191 will see from the next stage of the system is also added (R15). This load allows for the proper simulation of the circuit stability.

图 8 highlights the results from the OPA191 stability simulation resulting in a phase margin of ≈ 63º, implying the circuit is stable. For more information about amplifier stability, see TI's Precision Labs.
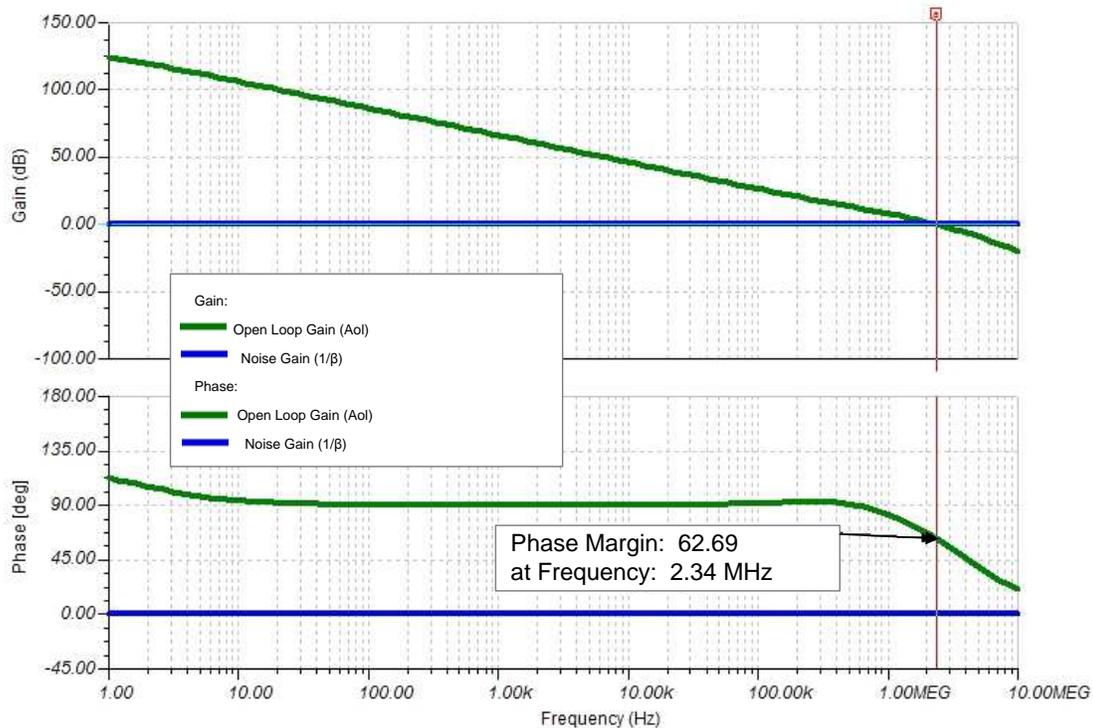

图 **8. OPA191 TINA-TI Stability Simulation Results**

2.3.2   Fully-Differential ADC Driver

The TIDA-01013 input driver circuit for the ADS127L01 high-precision ADC consists of two parts: the THS4551 (THS4561) fully-differential amplifier configured in a second-order multiple-feedback (MFB) filter configuration, and a first-order low-pass RC filter. The THS4551 (THS4561) is used for signal conditioning of the input signal, and its low output impedance provides a buffer between the signal source and the switched-capacitor inputs of the ADC. The low-pass RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage, which draws current during each sample. A careful front-end circuit design is required to meet the resolution, linearity, and noise performance capabilities of the ADS127L01.

2.3.2.1   THS4551

The THS4551 is chosen as the FDA due to its low power consumption combined with low noise and great THD performance. The quiescent current is 1.37 mA at 5 V V_{S+}. Because the input range of the system is ±10 V and the ADC reference voltage is 3 V (V_{REFP} = 3 V and V_{REFN} = GND), an attenuation of 1/3.4 is required to use the full-scale (FS) range of the ADC without saturation. The feedback and gain-setting resistors, R_F and R_I, are set to 1 kΩ and 3.4 kΩ, respectively, as shown in 图 9. The MFB filter configuration produces a second-order, low-pass response with a cutoff frequency of ≈ 600 kHz.

The main function of the low-pass RC filter is to provide charge to the internal sampling capacitors in the ADS127L01 modulator. A 1.6-nF filter capacitor is chosen to be 100 times larger than the 16-pF ADC sampling capacitors. This keeps the initial voltage droop at the beginning of the sampling period to < 1% of the final value. The subsequent recovery results in even smaller error at the end of the sampling period (≈ ½ of the modulator period). The 10-Ω resistors outside the THS4551 feedback loop are required to isolate the amplifier outputs from the capacitive load and maintain circuit stability.
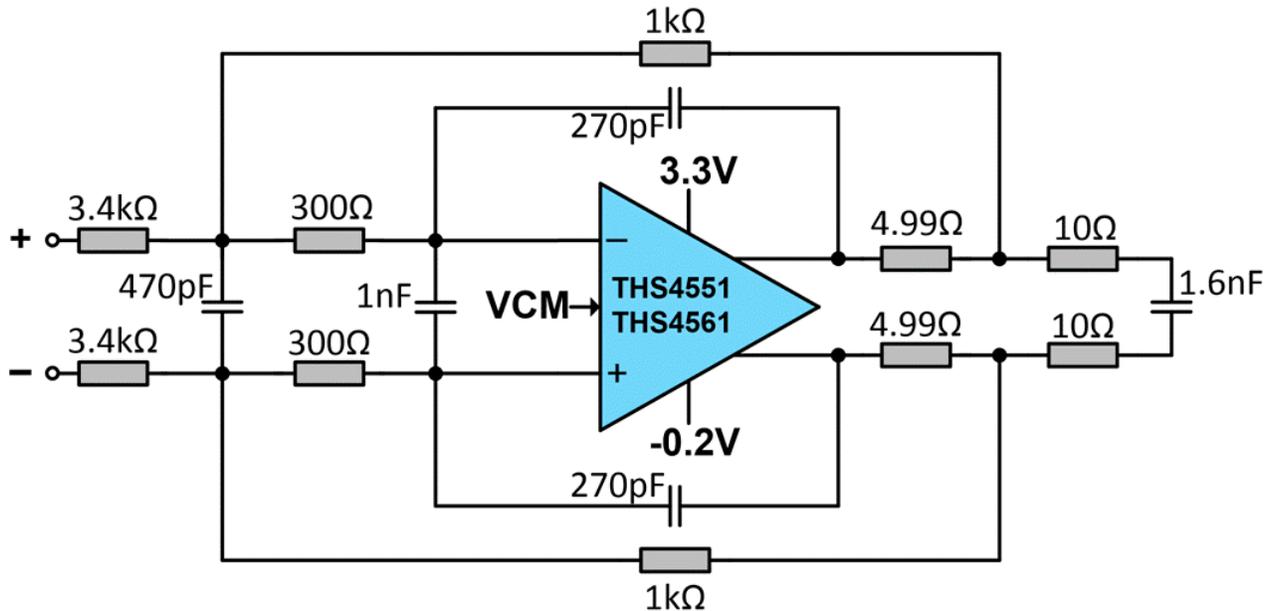
图 **9. THS4551 and THS4561 ADC Driver**

Like the OPA191, the THS4551 has rail-to-rail input and output, so the output signal can reach 0 V and 3.0 V. Because the ADS127L01 has a maximum V_{REF} of 3.0 V, the V_{S+} is chosen to be 3.3 V to allow for improved THD performance, being 300 mV higher than the maximum differential output.

TINA-TI is used to simulate and evaluate the stability of the THS4551 ADC driver subsystem shown in 图 10. Once again, the circuit includes a 1-TF capacitor and 1-TH inductor to break the feedback loop of the amplifier for simulation purposes.
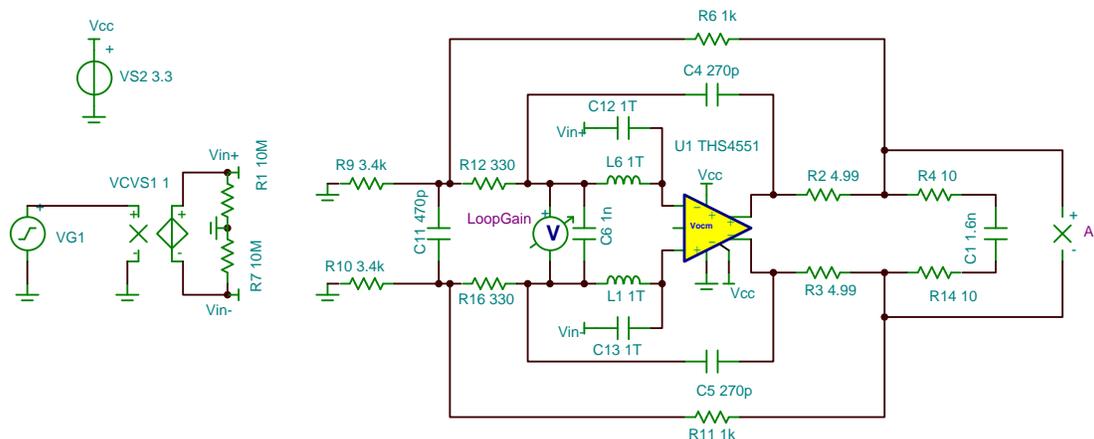

图 **10. THS4551 TINA-TI Stability Schematic**

Simulation results shown in 图 11 include the circuit's loaded open-loop gain (Aol), loop gain (Aol×β), and noise gain (1/β). These results show a phase margin of ≈ 58º, indicating that the circuit is stable. For more information about amplifier stability, see TI's Precision Labs.
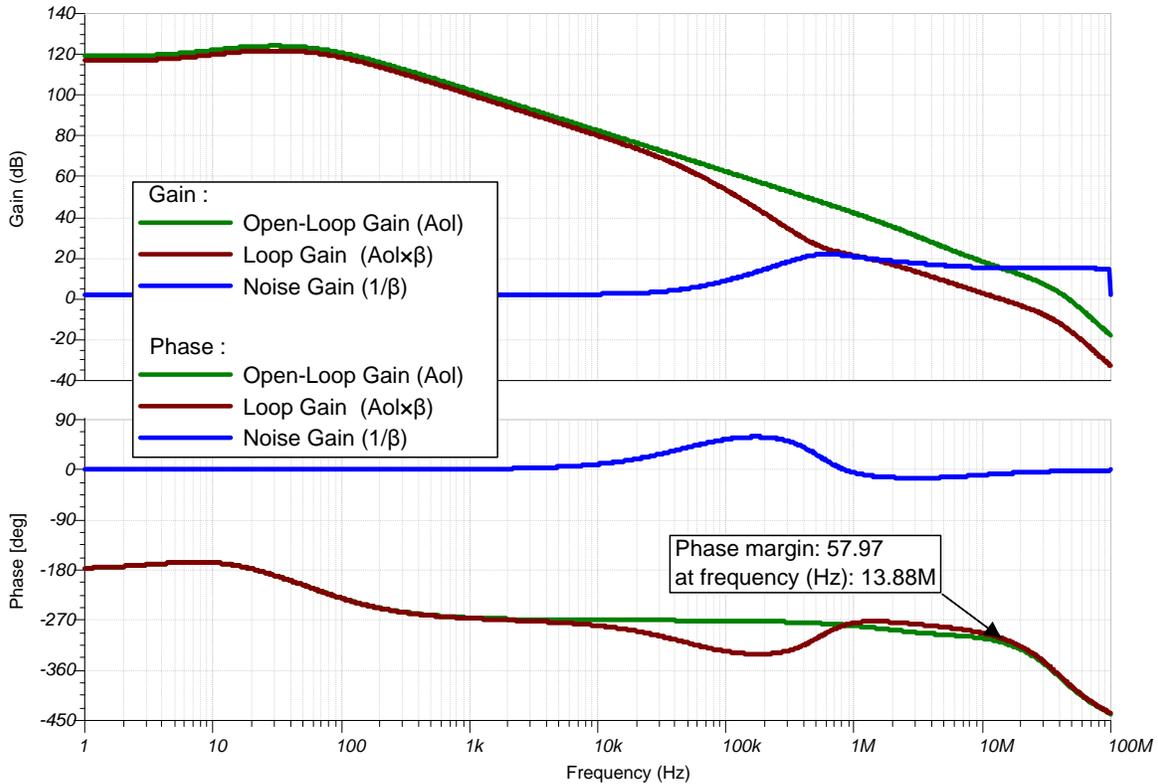

图 **11. THS4551 TINA-TI Stability Plot**

2.3.2.2 THS4561

The THS4561 is chosen as the FDA due to its low power consumption combined with low noise and great THD performance. The quiescent current is 0.85 mA at 5 V V_{S+}. Because the input range of the system is ±10 V and the ADC reference voltage is 3 V (V_{REFP} = 3 V and V_{REFN} = GND), an attenuation of 1/3.4 is required to use the full-scale (FS) range of the ADC without saturation. The feedback and gain-setting resistors, R_F and R_I, are set to 1 kΩ and 3.4 kΩ, respectively, as shown in 图 12. The MFB filter configuration produces a second-order, low-pass response with a cutoff frequency of ≈ 600 kHz.

The main function of the low-pass RC filter is to provide charge to the internal sampling capacitors in the ADS127L01 modulator. A 1.6-nF filter capacitor is chosen to be 100 times larger than the 16-pF ADC sampling capacitors. This keeps the initial voltage droop at the beginning of the sampling period to < 1% of the final value. The subsequent recovery results in even smaller error at the end of the sampling period (≈ ½ of the modulator period). The 10-Ω resistors outside the THS4561 feedback loop are required to isolate the amplifier outputs from the capacitive load and maintain circuit stability.

Like the OPA191, the THS4561 has rail-to-rail input and output, so the output signal can reach 0 V and 3.0 V. Because the ADS127L01 has a maximum V_{REF} of 3.0 V, the V_{S+} is chosen to be 3.3 V to allow for improved THD performance, being 300 mV higher than the maximum differential output.
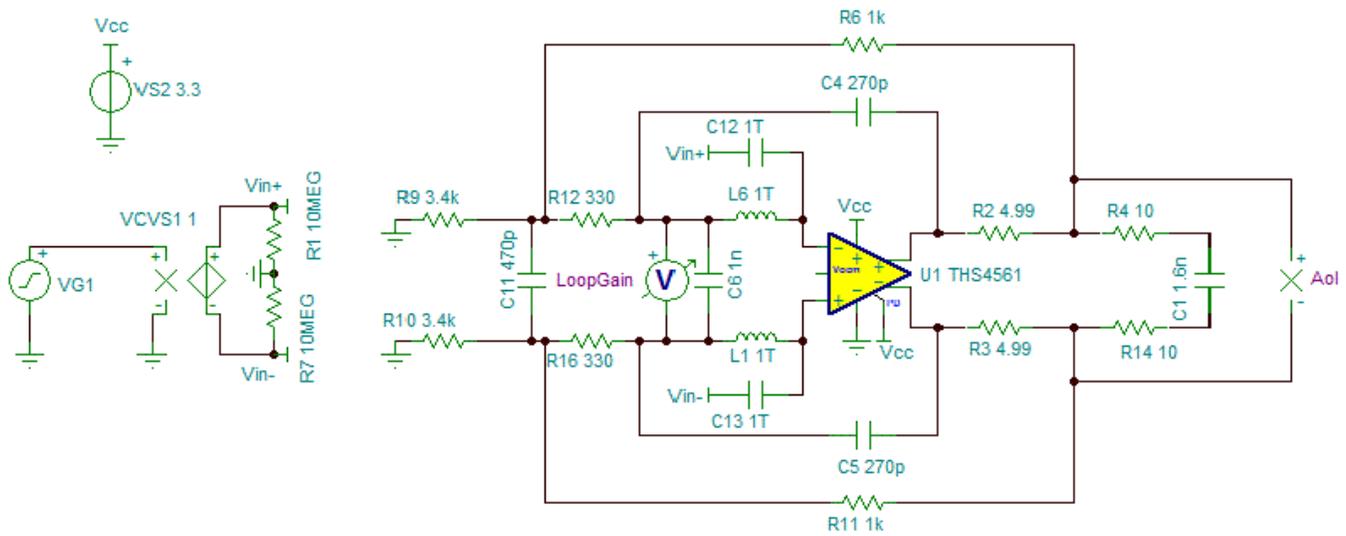
图 **12. THS4561 TINA-TI Stability Schematic**

Simulation results shown in 图 13 include the circuit's loaded open-loop gain (AoI), loop gain (AoI×β), and noise gain (1/β). These results show a phase margin of ≈ 58º, indicating that the circuit is stable. For more information about amplifier stability, see TI's Precision Labs.
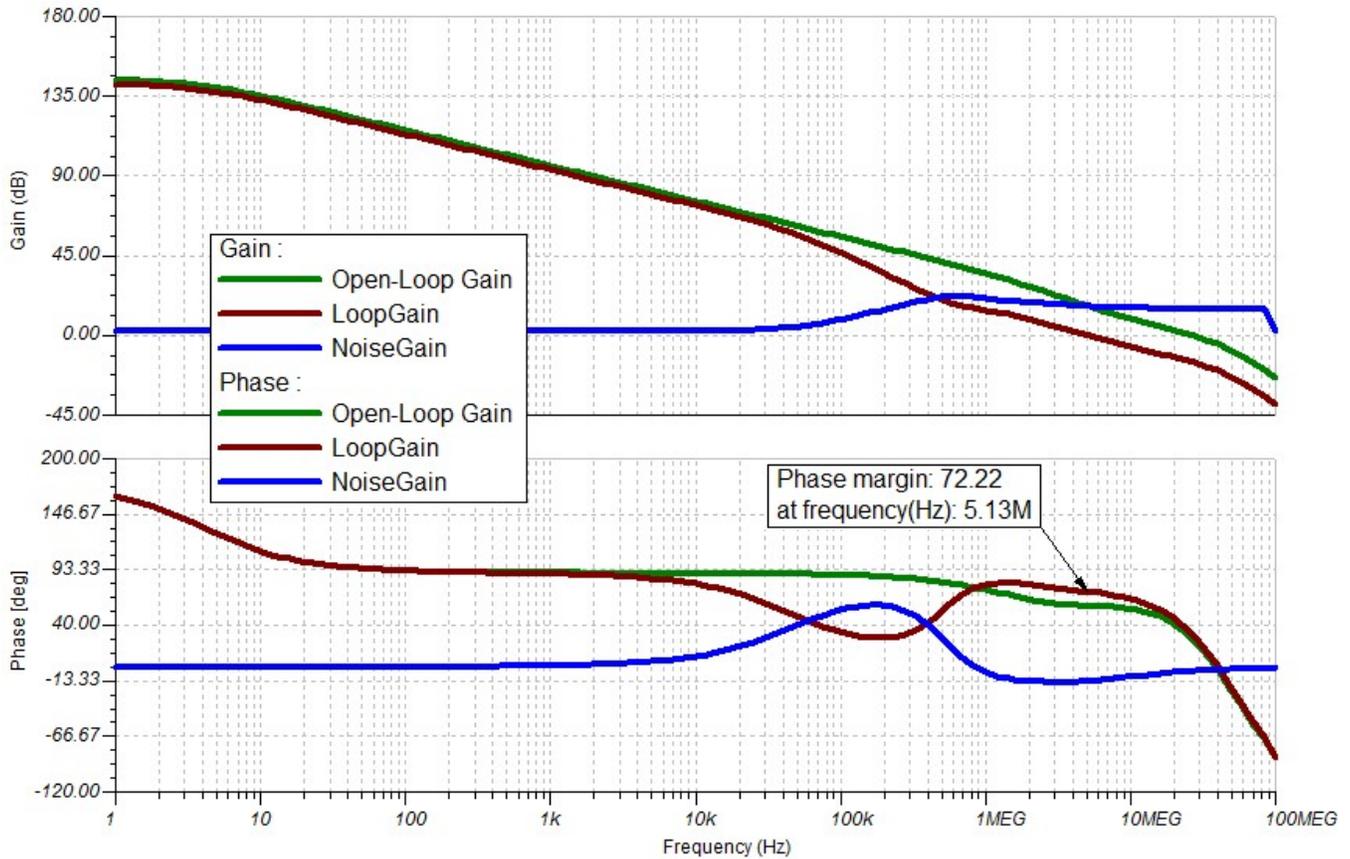

图 **13. THS4561 TINA-TI Stability Plot**

2.3.3 Reference Voltage Design Theory

External voltage reference circuits are used in a DAQ if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits must provide a low-drift, low-noise, and accurate voltage for the ADC reference input. However, the output broadband noise of most references can be a few 100 μV_{RMS}. This noise can degrade the noise and linearity performance of precision ADCs, for which the typical noise is in the order of tens of μV_{RMS}. In addition, voltage reference devices typically have weak drive capability and must only be used to drive high-impedance reference inputs. To optimize the ADC performance, the output of the voltage reference must be appropriately buffered and filtered to drive the switched-capacitor sampling inputs of the ADS127L01.
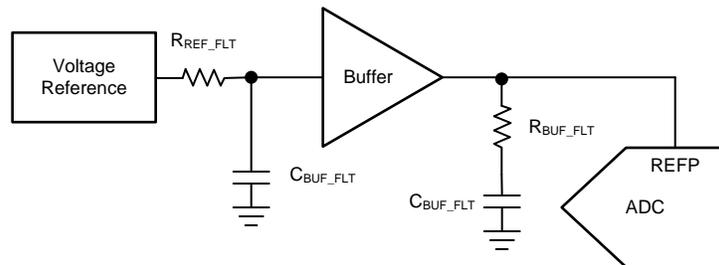

图 **14. Simplified Schematic of Reference Driver**

A simpler approach is to use a low-noise voltage reference device with an integrated buffer, such as the REF6030. Having an integrated buffer is extremely beneficial because it reduces the footprint and complexity of designs. The REF6030 is able to provide a 3.0-V reference with 5 μV_{RMS} while consuming 0.8 mA of quiescent current. This TI Design powers the REF6030 with a 3.3-V source, so the expected power consumption is calculated as 2.64 mW. The REF6030 3.0-V output drives the V_{REFP} pin of the ADS127L01, while the V_{REFN} pin is tied to the analog ground. The schematic can be seen in 图 15.
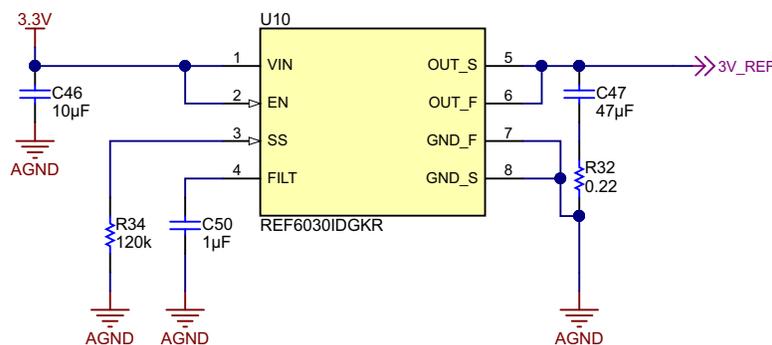

图 **15. Reference Voltage Altium Schematic**

2.3.4   Power Rails

As shown in 图 1, the TIDA-01013 reference design power subsystem requires a wide variety of voltage rails to meet system requirements. All voltage rails are generated from one external 12-V DC power supply. The power tree in 图 16 illustrates the resulting distribution of the required rails, which includes two digital voltage rails (D1.8V and D3.3V) and three analog voltage rails (3.3 V, 5.2 V, and –5.2 V). Each rail is derived by using DC-DC converters to efficiently create intermediate voltages slightly above each output voltage rail, followed by an appropriate LDO to suppress a DC-DC converter switching ripple.
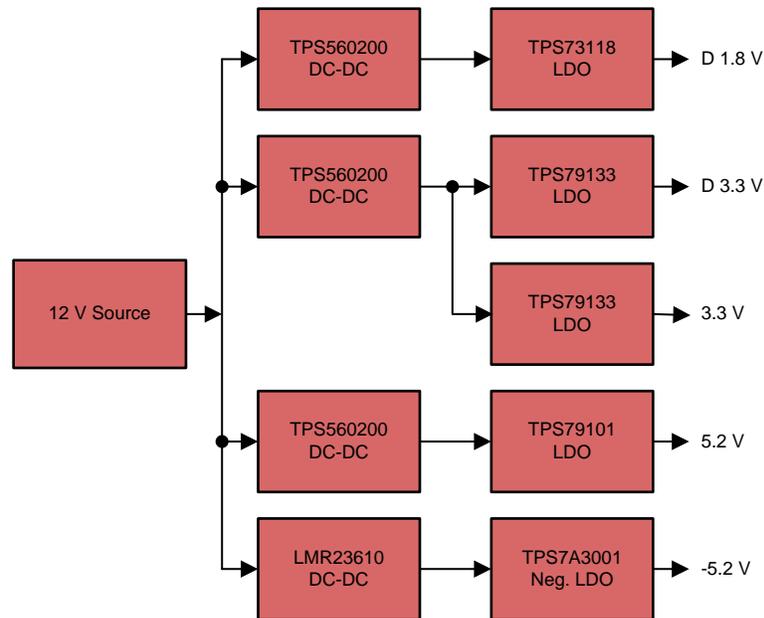

图 16. TIDA-01013 Power Supply Block Diagram

2.3.5 24-Bit Delta-Sigma ADC

Finding the appropriate ADC for a given task can be challenging. There are many parameters to consider, such as the resolution, sampling rate, noise performance, linearity, and input voltage range. In addition, power consumption and footprint size are critical restrictions for mobile applications. The ADS127L01 is selected because it features VLP Mode, which reduces the power consumption to 9.6 mW while maintaining at least 105 dB SNR.

The ADS127L01 also features a built-in digital low-pass filter, which attenuates higher frequency signals and noise and determines the overall frequency response of the ADC. The user has the option to select either a wideband filter with one of two transition bands (Wideband 1 or Wideband 2) or a sinc filter. For this application, the Wideband 2 filter is chosen for its extended flat passband and limited signal aliasing. See the ADS127L01 datasheet for more information on the digital filter response characteristics.

The digital filter is also responsible for decimating the delta-sigma modulator output into a high-resolution data word. The final output data rate (f_{DATA}) is equal to the modulator sampling frequency (f_{MOD}) divided by the oversampling ratio (OSR). The wideband filters in the ADS127L01 offer four OSR options to configure the data rate: 32, 64, 128, and 256. For this application, OSR = 32 is used to set the output data rate to 125 kSPS and the unity-gain bandwidth to 50 kHz. This ensures that the 30-kHz input signal is not attenuated by the digital filter of the ADC.

The expected SNR for a 3-V reference voltage and OSR = 32 is given as a typical specification of 105.8 dB in the ADS127L01 Electrical Characteristics table (see the ADS127L01 datasheet). 公式 2 calculates the expected RMS noise (V_{RMS_Noise}) as 10.88 µV_{RMS}. A more detailed table regarding the operating modes, data rates, and filter bandwidths is found in Table 1 of the ADS127L01 datasheet.

$$V_{RMS\_Noise} = \frac{V_{REF}}{\sqrt{2} \times 10^{\frac{SNR}{20}}}$$

(2)

Therefore:

$$V_{RMS\_Noise} = \frac{3\ V}{\sqrt{2} \times 10^{\frac{105.8\ dB}{20}}}$$

$$V_{RMS\_Noise} = 10.88\ \mu V_{RMS}$$

Using the RMS noise, 公式 3 calculates the effective number of bits (ENOB):

$$ENOB = \log_2\left(\frac{2 \times V_{REF}}{V_{RMS\_Noise}}\right)$$

(3)

Therefore:

$$ENOB_{ADC} = \log_2\left(\frac{2 \times 3\ V}{10.88\ \mu V_{RMS}}\right)$$

$$ENOB_{ADC} = 19.073\ bits$$

2.3.6 TIDA-01013 Analog Front End (AFE)

The block diagram shown in 图 17 illustrates the complete TIDA-01013 AFE subsystem. The following sections describe the critical system parameters of this subsystem including bandwidth, noise, SNR, ENOB, THD, and power. These sections also cover relevant design considerations and trade-offs associated with each parameter.
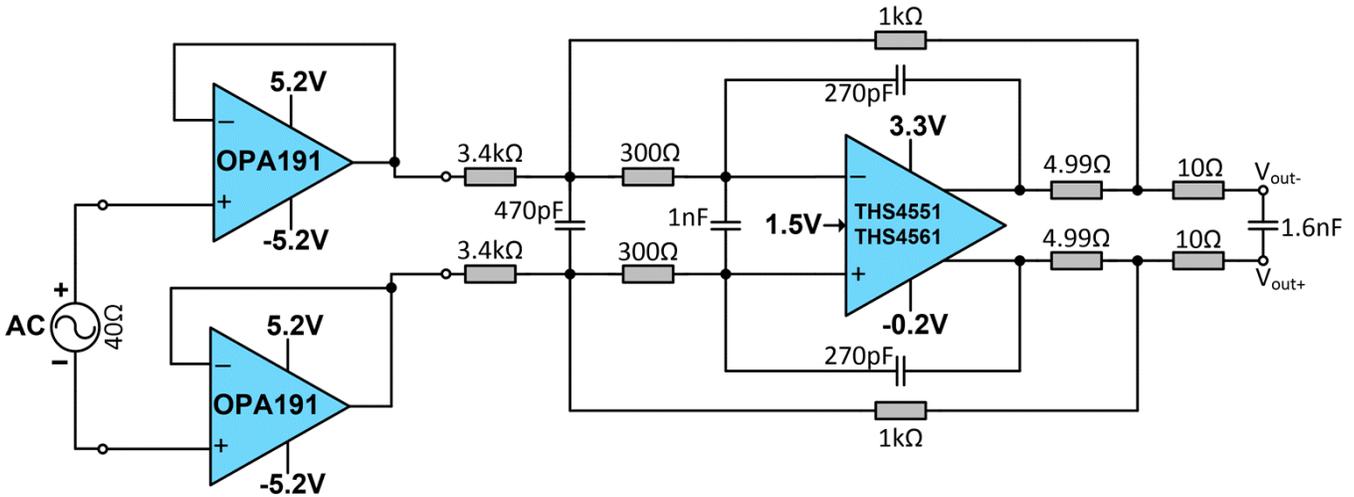

图 **17. TIDA-01013 AFE Subsystem**

图 18 highlights the schematic used to simulate and estimate the bandwidth of the TIDA-01013 AFE stage.
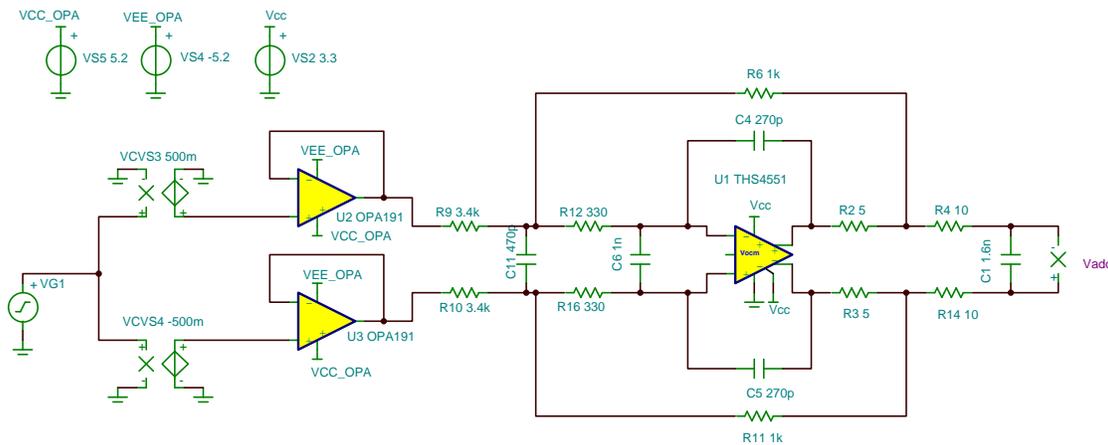

图 **18. TIDA-01013 TINA-TI AFE Schematic**

2.3.6.1 *AFE Bandwidth*

As shown in the simulated bandwidth plot of 图 19, the TIDA-01013 has sufficient bandwidth for the 30-kHz input signal range while significantly filtering higher frequency wideband noise.
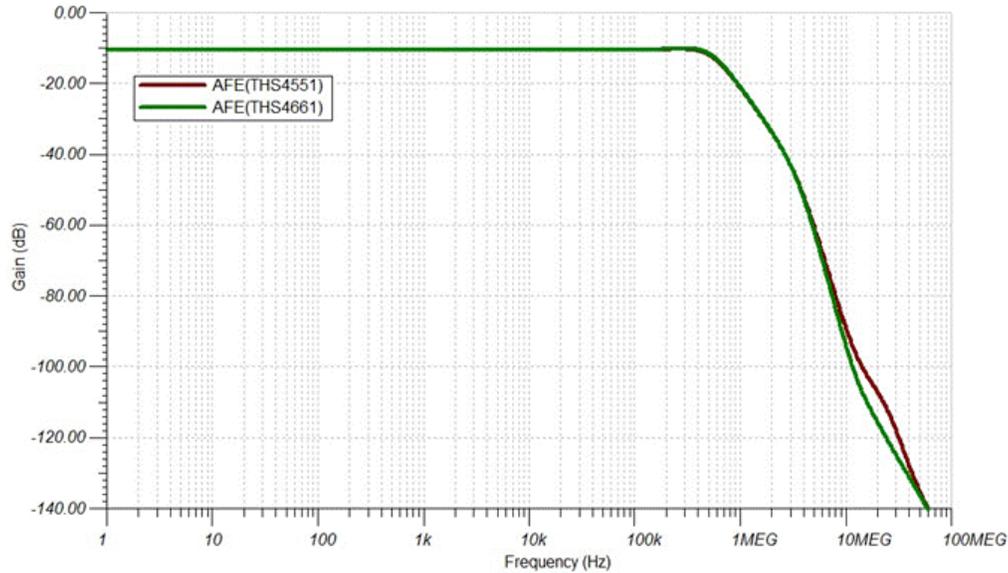

图 **19. TIDA-01013 AFE Bandwidth**

2.3.6.2 *AFE Noise*

The AFE output-referred noise of the TIDA-01013 AFE subsystem in 图 18 is simulated using TINA-TI. The simulation results in 图 20 show an integrated output-referred noise of 2.53 μV_{RMS} (THS4551) / 2.82μV (THS4561) over a

50-kHz bandwidth. As previously mentioned, 50 kHz is the bandwidth of the digital filter configured in 节 2.3.5. Because the bandwidth of the TIDA-01013 AFE is much higher, the ADC digital filter response determines the effective noise bandwidth of the overall system. The response of the digital filter returns to unity gain at multiples of the modulator frequency (that is, 4 MHz, 8 MHz, and so on). For this reason, it is important that AFE stage provides sufficient antialiasing to out-of-band signals at these frequencies. 图 19 illustrates that the AFE response provides approximately 50 dB of attenuation at 4 MHz and continues to roll off at higher frequencies.
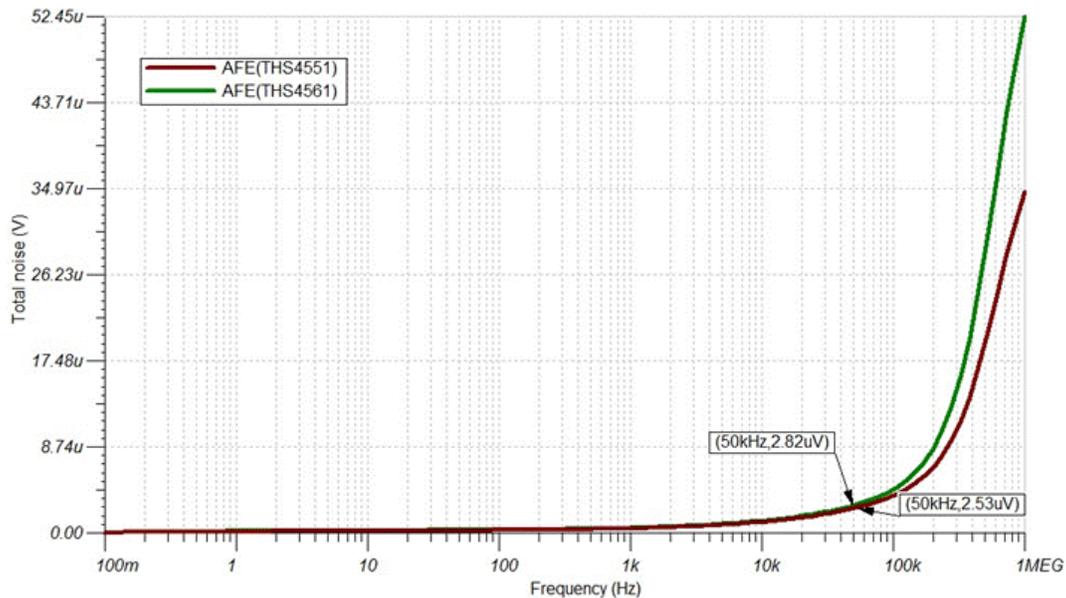
图 **20. TIDA-01013 AFE Output Noise**

2.3.6.3 *AFE SNR*

The maximum input signal to the ADC is limited by the 3-V reference voltage. The best SNR of the TIDA-01013 AFE subsystem can be calculated using a FS input (V_{FS_Signal}) and the simulated RMS noise of the AFE (V_{RMS_Noise}) as 公式 4 shows:

$$SNR_{AFE} = 20 \times \log\left(\frac{V_{FS\_Signal}}{\sqrt{2} \times V_{RMS\_Noise}} \right)$$

$$SNR_{AFE} = 20 \times \log\left(\frac{3\ V}{\sqrt{2} \times 2.53\ \mu V_{RMS}} \right)$$

(4)

The goal of any AFE design must be to meet or exceed the performance of the data converter so as not to limit the overall system performance. The result in 公式 4 illustrates that the AFE is capable of achieving approximately 118.47 dB SNR, which is greater than the expected SNR performance of the ADS127L01 (105.8 dB).

2.3.6.4 *AFE THD*

The expected total harmonic distortion (THD) of the system is approximated by comparing the respective distortion performance of each stage of the design. Figure 25 in the OPA191 datasheet illustrates THD+N (total harmonic distortion plus noise), which is still a close approximation to the THD performance of the amplifier. At 2 kHz, THD+N is approximately –88 dB for a 2-kΩ load. At 20 kHz, this value decreases to about –78 dB. The THD of the THS4551 and the ADS127L01 (in VLP Mode) offer in excess of –129 dB or better THD at these frequencies. This illustrates that the distortion performance of the overall system, though limited by the OPA191 stage, can still meet the performance design goals with minimal added power consumption.

2.3.6.5 *AFE Power Consumption*

The total power consumption of the front end is the sum of the power consumed by each voltage rail. The power consumption at each rail is calculated by multiplying the current draw by the respective voltage potential. The setup for the power consumption can be seen in 图 21. The simulations are done in Cadence Virtuoso with a 0-V dc input source.
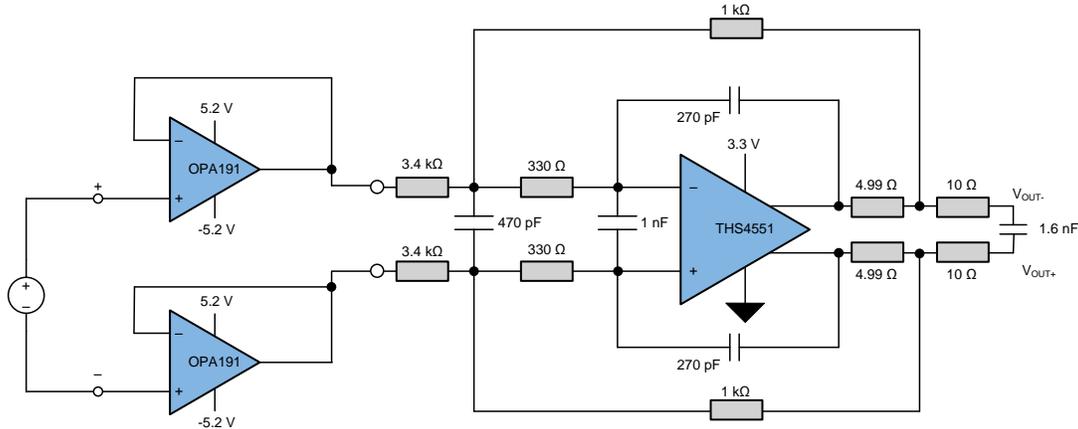

图 **21. TIDA-01013 AFE Power Simulation Schematic**

The current draw from the 5.2-V and –5.2-V sources are 0.28 mA and 0.97 mA, respectively, yielding a total power of 6.5 mW for the OPA191 buffers. The current draw from the 3.3-V source is 1.85 mA, yielding a total power of 6.1 mW for the THS4551. The total power consumption for the AFE sums to 12.6 mW.

2.3.7 TIDA-01013 System SNR and ENOB

Calculate the TIDA-01013 full system (AFE + ADC) SNR by vectorially summing the AFE output-referred noise (see 节 2.3.6.2) to the ADC integrated noise (see 节 2.3.5) as shown in 公式 5, and apply the result to 公式 4.

$$\text{Total Integrated Noise}_{\text{System}} = \sqrt{\text{Noise}_{\text{Front-end}}^2 + \text{Noise}_{\text{ADC}}^2} \tag{5}$$

Therefore:

$$\text{Total Integrated Noise}_{\text{System}} = \sqrt{2.53\,\mu V_{\text{RMS}}^2 + 10.88\,\mu V_{\text{RMS}}^2} = 11.17\,\mu V_{\text{RMS}}$$

$$\text{SNR}_{\text{System}} = 20 \times \log\left(\frac{V_{\text{RMS\_Signal}}}{V_{\text{RMS\_Noise}}}\right)$$

$$\text{SNR}_{\text{System}} = 20 \times \log\left(\frac{10\ V}{3.4 \times \sqrt{2} \times 11.17\ \mu V_{\text{RMS}}}\right)$$

The overall effective number of bits, $\text{ENOB}_{\text{System}}$, includes the noise of the front end as well as the noise from the ADC and is calculated once again using 公式 3.

$$\text{ENOB}_{\text{System}} = \log_2\left(\frac{2 \times 3\ V}{11.18\ \mu V_{\text{RMS}}}\right) = 19.035\ \text{bits}$$

Comparing ENOB$_{System}$ to ENOB$_{ADC}$ of 19.073 (see 节 2.3.5), the AFE noise impact on the system ENOB is less than < 0.1 bits.

Find more information on the noise performance of the ADS127L01 in Section 7.1 of the ADS127L01 datasheet.

2.3.8 AFE Power versus Noise Performance Trade-Offs

The TIDA-01013 design goal of maximizing system SNR performance while minimizing power consumption requires careful design consideration because performance and power are conflicting system parameters. Improving one of these degrades the other. Given the OPA191 buffer, THS4551 ADC driver, and ADS127L01 ADC component selections, as well as the chosen ADS127L01 operating modes described in previous sections, the remaining component values from which to choose that influence performance and power results are the feedback and gain-setting resistors in the THS4551 gain stage, R_F and R_I, respectively. The R_F-to-R_I ratio must be 1/3.4 to achieve the required attenuation factor, but the actual absolute values can be adjusted to alter power and performance results.

One approach to choosing these resistor values is to keep the AFE amplifier total output noise somewhat lower than the total ADC input referred noise over the –3-dB bandwidth of the ADS127L01 digital filter to minimize system SNR degradation. The ADS127L01 digital filter bandwidth is 50 kHz, as described in 节 2.3.2. As a design target, the total output noise must be less than 20% of the ADC input-referred noise, as shown in 公式 6.

$$\text{Integrated Output Noise}_{AFE} \leq 20\% \times \left(\frac{V_{REF}}{\sqrt{2} \times 10^{\frac{ADC\_SNR}{20}}} \right)$$

(6)

where:

- V_{REF} = ADC reference voltage = 3.0 V
- ADC_SNR = ADC signal-to-noise ratio = 105.8 dB as mentioned in 节 2.3.5

Therefore:

$$\text{Integrated Output Noise}_{AFE} \leq 20\% \times \left(\frac{3\,V}{\sqrt{2} \times 10^{\frac{105.8}{20}}} \right)$$

图 22 plots the AFE integrated output noise versus AFE power as simulated in Cadence Virtuoso. R_F values from 1 to 100 kΩ are used while maintaining an R_G value of 3.4 × R_F. As shown in 图 22, the desired AFE integrated output noise approaches, but does not quite meet, the noise target derived in 公式 6. An R_F value of 1 kΩ is selected for the TIDA-01013 to maximize SNR performance according to this design target.
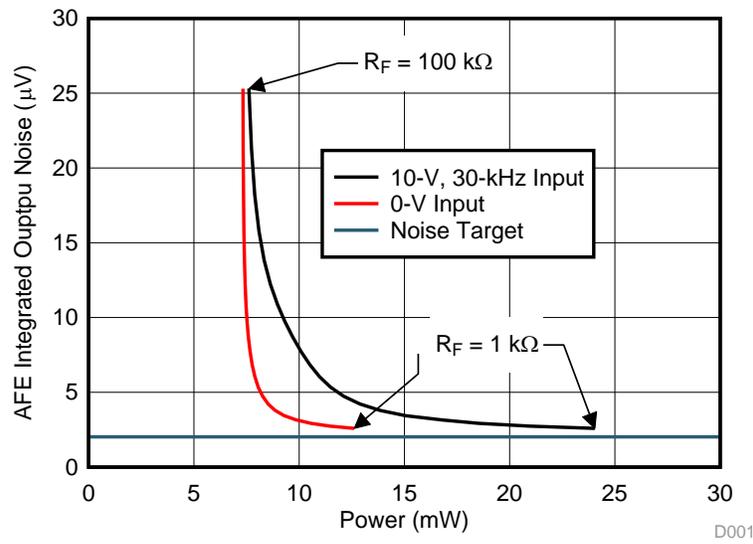
图 **22. TIDA-01013 AFE Integrated Output Noise versus Power Plot**

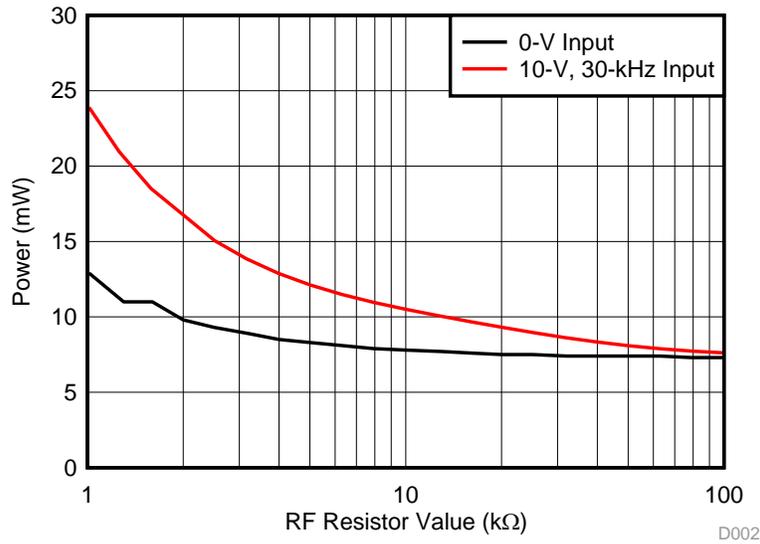图 23 plots the AFE power as a function of R_F resistor values.

图 **23. TIDA-01013 AFE Power versus R_F Resistance**

An alternative approach is to view performance versus power at a system level by plotting system SNR versus system power as shown in 图 24 using the same resistor range as before. With this chart, the optimal operating point for the application can be determined and resistor values selected accordingly.

Note that there is a portion of the curve where power can be reduced with very little impact on SNR. For example, on the 10-V, 30-kHz curve, power can be reduced from 42 mW to 30 mW with only a 1-dB degradation in SNR. Likewise, significant SNR improvement from 98 dB to 105 dB can be achieved by a small increase in power from 26 mW to 30 mW.
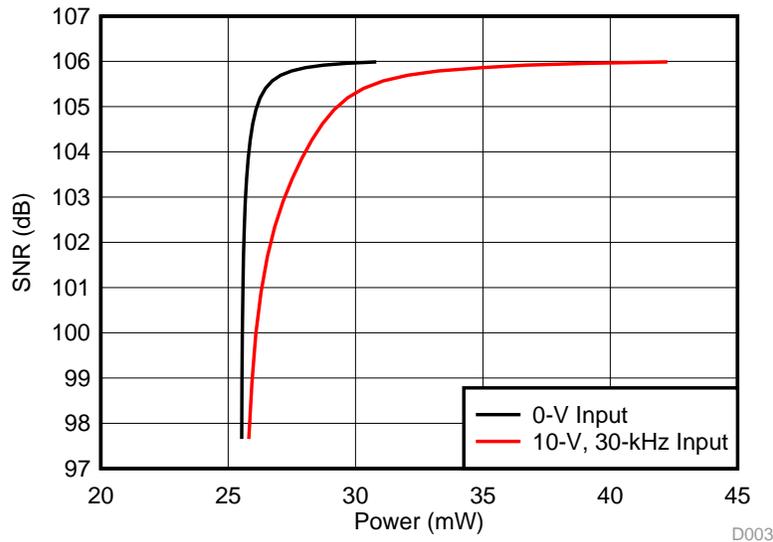

图 **24. TIDA-01013 System SNR versus Power Plot**

3   Hardware, Testing Requirements, and Test Results

3.1   Required Hardware

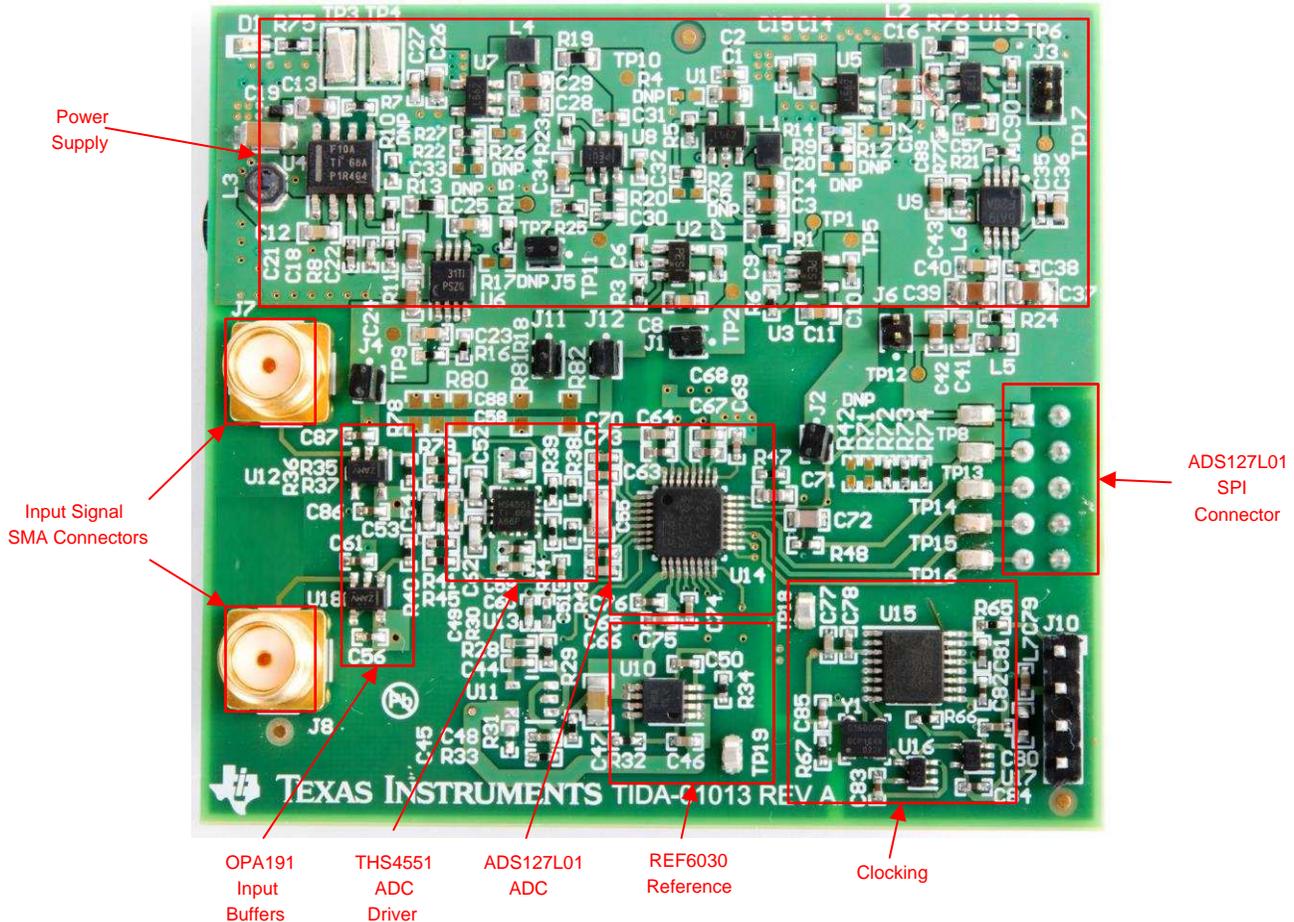图 25 highlights the various subsystems and features of the TIDA-01013 hardware.

图 **25. TIDA-01013 Hardware**

For ease of development, the TIDA-01013 board was designed to be used in conjunction with a slightly modified ADS127L01EVM as a platform for collecting data from the TIDA-01013 system. The resulting solution uses the ADS127L01EVM board's PC Host Interface (PHI) subsystem to communicate with the ADC via SPI and provide communication with a PC over a USB interface. The EVM also includes a software application that runs on a PC to allow for register manipulation and data collection. For this approach, modify the EVM hardware as follows:

1. Use the default jumper settings of the ADS127L01EVM (as described in the ADS127L01 user's guide) with the following exceptions:
    - Uninstall JP11.
    - Uninstall the pin-5 to pin-6 jumper on J3 of the EVM board.
2. Remove the ADS127L01 device on the EVM board (U26). This is required to allow the TIDA-01013 board to use the EVM debug header (J6) and connect the TIDA-01013 ADC SPI signals to the EVM host interface subsystem. Doing so prevents conflict with the ADC included with this EVM. The TIDA-01013 SPI header (J9) can then be mated with the EVM debug header. Alternatively, jumper wires can be used to connect the SPI signals on the TIDA-01013 daughterboard to the right-hand side of J3 with the respective jumpers removed. See the ADS127L01 user's guide for more information on the EVM

SPI signal connections.

3. Connect pin 1 of J10 (TIVA_16MHz) on the TIDA-01013 daughterboard to pin 5 of J3 on the EVM board using an external jumper wire.

4. Connect pin 3 of J10 (D1.8V) on the TIDA-01013 board to TP21 of the EVM board using an external jumper wire.
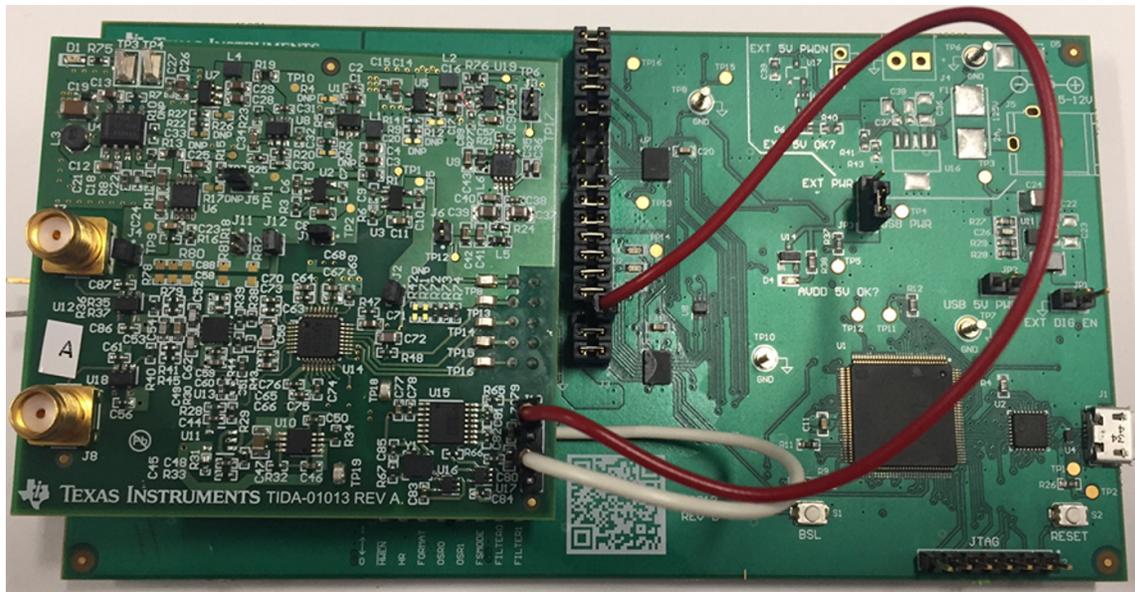

图 26. TIDA-01013 and ADS127L01 System

表 2 highlights the purpose of the various jumpers on the TIDA-01013 board as well as the default configurations.

表 2. TIDA-01013 Board Jumper Settings

JUMPER NAME	DEFAULT POSITION	COMMENT
JP1	Installed	For 3.3-V rail current measurements
JP2	Installed	For D3.3-V rail current measurements
JP3	1-2	D1.8-V power source selection
JP4	Installed	For –5.2-V rail current measurements
JP5	Installed	For 5.2-V rail current measurements
JP11	Installed	For THS_3.3-V rail current measurements
JP12	Installed	For ADC_3.3-V rail current measurements

3.2 Measuring SNR, ENOB, THD, and Power

The design hardware testing requires a high-quality signal generator with a differential output; otherwise, the signal source could limit the measurement results. The Audio Precision AP-2700 series is used to generate the inputs necessary for system characterization and its characteristics are given in 表 3.

表 3. External Source Requirements

SPECIFICATION DESCRIPTION	SPECIFICATION VALUE
External source type	Balanced differential
External source impedance (RS)	10 to 30 Ω
Maximum noise	10 μV_{RMS}
Maximum SNR	110 dB
Maximum THD	−130 dB

Using SMA cables, attach the output of the signal generator to the TIDA-01013 board input signal connectors and then connect the ADS127L01EVM to the PC host using a USB cable. Confirm the signal generator settings and apply power to the TIDA_01013 system before enabling the signal generator output.

Install and run the ADS127L01EVM software provided on the ADS127L01EVM product page. See the ADS127L01 user's guide for installation and start-up instructions. Because the ADS127L01 configuration is set by external pullup and pulldown resistors on the TIDA-01013 daughterboard, the ADS127L01EVM software can only be used to collect data, not to modify the ADC configuration. Data is collected under the Data Analysis window, where it can be viewed in a tabular, time-domain, or histogram format. For additional analysis, the data can be exported to a text file along with the user entries for clock frequency and reference voltage.

3.3 Testing and Results

The following sections describe the test setups, procedures, and performance results for the various tests that were performed on the reference design board.

An Audio Precision 2700 series signal generator is used as the signal source to test the AFE and ADC performance. The AP2700's noise and THD has adequate performance and does not limit measurements. It is crucial to use a quality source as to not limit the system's performance by the signal source. A generic DC power supply is used to generate the 12-V DC input voltages.

The AP2700 is set to output the various input signal frequencies and amplitudes to capture the SNR and THD measurements shown in 表 4 and plotted in 图 27 and 图 28.

表 4. TIDA-01013 SNR and THD Measurements

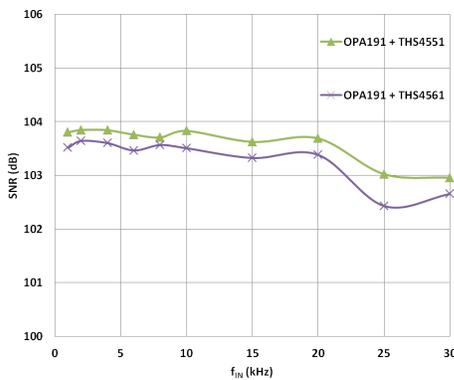| FREQUENCY (kHz)	SNR (dB) ±1 Vp_differential (-20 dBFS) (THS4551)	SNR (dB) ±1 Vp_differential (-20 dBFS) (THS4561)	THD (dB) ±10 Vp_differential (–0.02 dBFS) (THS4551)	THD (dB) ±10 Vp_differential (–0.02 dBFS) (THS4561)
1	103.62	103.51	–90.97	-81.38
2	103.78	103.64	–88.79	-81.28
4	103.78	103.60	–84.78	-80.24
6	103.74	103.46	–83.12	-78.61
8	103.60	103.56	–80.70	-77.86
10	103.76	103.50	–77.59	-76.00
15	103.75	103.32	–72.10	-71.25
20	103.68	103.38	–85.11	-88.63
25	103.65	102.43	–77.77	-80.78
30	103.69	102.65	–114.47	-114.99

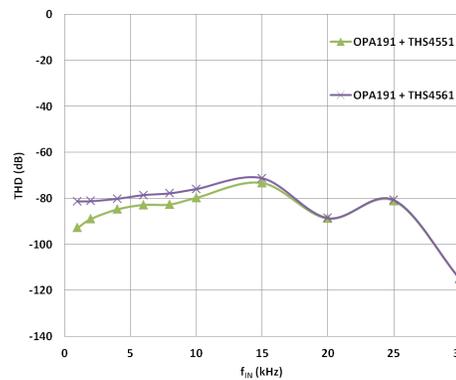**图 27. TIDA-01013 SNR Versus Input Signal Frequency**

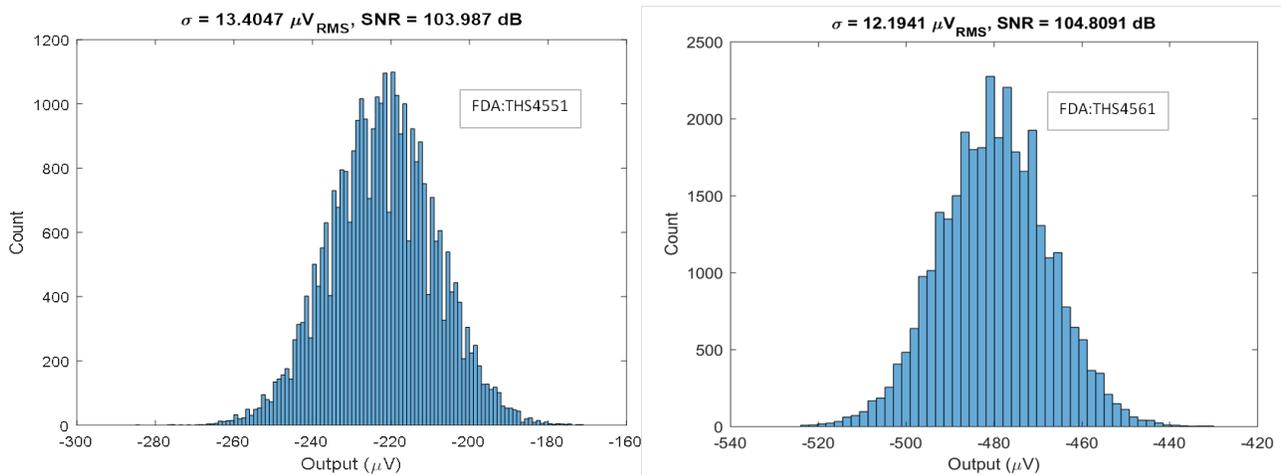**图 28. TIDA-01013 THD Versus Input Signal Frequency**

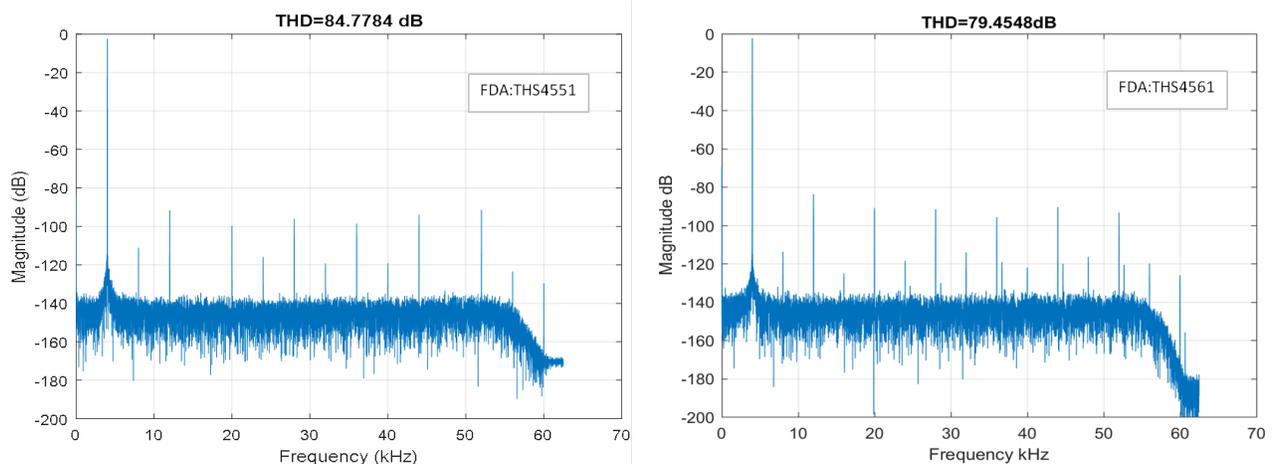图 **29. TIDA-01013 Noise Histogram for 0-V DC Input**

图 **30. TIDA-01013 Fast-Fourier Transform for 10-V$_P$, 4-kHz Sine Wave Input**

The standard deviation of the histogram in 图 29 is 13.4047 μV$_{RMS}$ (FDA:THS4551) or 12.1941 μV$_{RMS}$(FDA:THS4561), which yields an SNR of 103.99 dB (THS4551) or 104.81dB (THS4561). This falls in line with the SNR results over frequency illustrated in 图 27. Overall, the SNR results are similar to the expected results listed in 节 2.3.7, which meet the performance goals of the design.

The THD results are close to the expected performance of the OPA191, which dominated the overall distortion performance as described in 节 2.3.6.4. Up to 15 harmonics were included in the calculation; however, as the input frequency was increased, fewer harmonics remained within the digital filter passband and contributed to the THD results.

The various power rail jumpers listed in 表 2 are used to measure the power consumption of the system by uninstalling each jumper and inserting a digital multimeter to measure the current through each power rail. The measurement results are shown in 图 31 and 图 32. Note that these measurements include only those components associated with the signal chain and, therefore, do not include power supply efficiency losses or clocking circuitry.
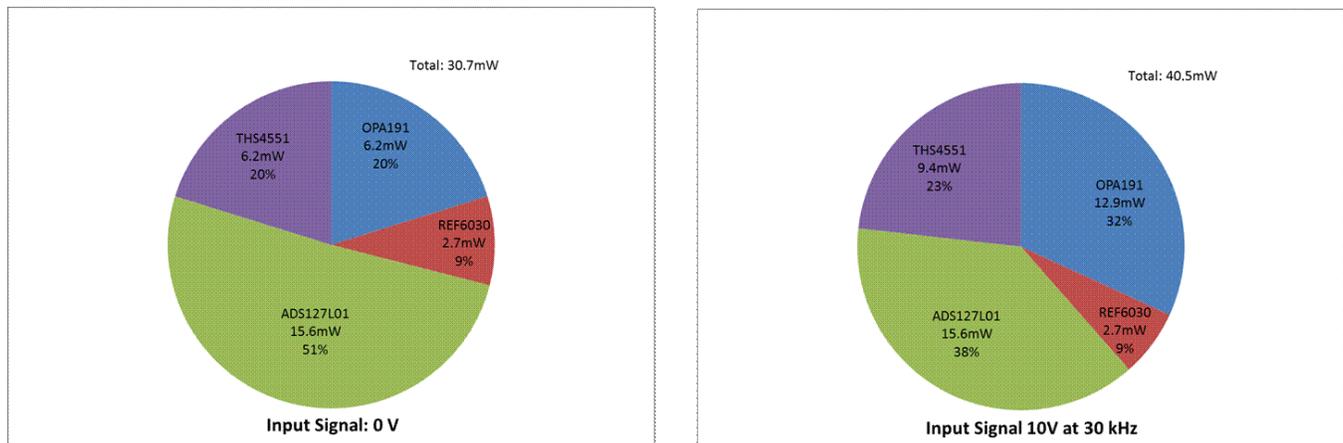
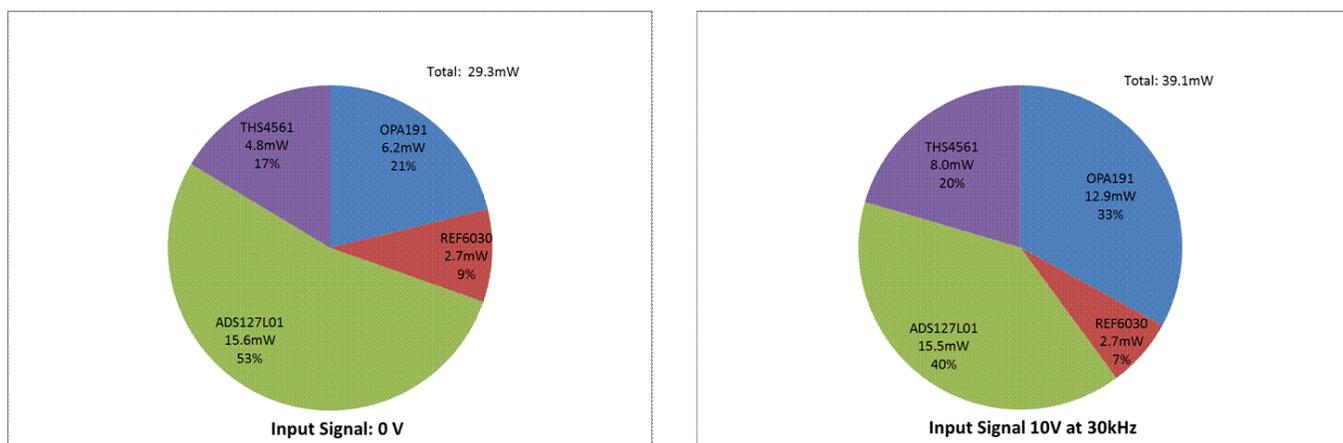**图 31. TIDA-01013 AFE (THS4551) and ADC Power Consumption**

图 32. TIDA-01013 AFE (THS4561) and ADC Power Consumption

These results are consistent with the power estimates simulated in Cadence Virtuoso as described in 节 2.3.6.5 and confirm the very low power performance of this reference design.

These measurements and test results confirm the power and performance simulation results described in 2.3 节 and meet the specification targets defined in 表 1. The THS4551 has better THD performance compared to the THS4561, but the THS4561 has lower power consumption.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01013.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01013.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01013.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01013.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01013.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01013.

5 Software Files

To download the software files, see the design files at TIDA-01013.

6 Related Documentation and Acknowledgments

6.1 Related Documentation

1. Texas Instruments, *Op-Amp Noise Theory and Applications*, Application Report (SLOA082)
2. Texas Instruments, *Multi-Input Reference Design Optimizing Channel-to-Channel Variation for Automatic Test Equipment*, TIDA-01050 Design Guide (TIDUCF5)
3. Texas Instruments, *ADC Driver Reference Design Improving Full Scale THD Using Negative Supply*, TIDA-01052 Design Guide (TIDUCK3)

6.1.1 商标

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6.2 Acknowledgments

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7 Terminology

AFE— Analog front end

DAQ— Data acquisition system

ADC— Analog-to-digital converter

SNR— Signal-to-noise ratio

ENOB— Effective number of bits

THD— Total harmonic distortion

IoT— Internet of Things

FS— Full-scale

VLP— Very low power

8 About the Authors

JORDAN RADICE is a systems designer at Texas Instruments, where he is responsible for developing reference design solutions for the Industrial Test and Measurement sector. Jordan earned his bachelor of science in electrical & computer engineering (BSECE) and master of science in electrical engineering (MSEE) from the University at Buffalo in Amherst, NY.

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