TI Designs：*TIDA-01487*
隔离式 CAN FD 中继器参考设计

说明

此隔离式 CAN FD 中继器参考设计在两个 CAN 总线段之间增加了电气隔离。总线段任一侧的 CAN 帧都被中继到另一侧。此参考设计中的 CAN 收发器和仲裁逻辑支持高达 2Mbps 的 CAN FD 速度。该设计由 5V 至 33V 的宽电源电压供电，并由一个平缓钳位浪涌保护器件提供保护，以防止受高功率瞬态或雷击事件的影响。

资源

TIDA-01487	设计文件夹
TCAN1042H	产品文件夹
ISO7721DR	产品文件夹
LM5166	产品文件夹
SN6501	产品文件夹
TVS3300	产品文件夹

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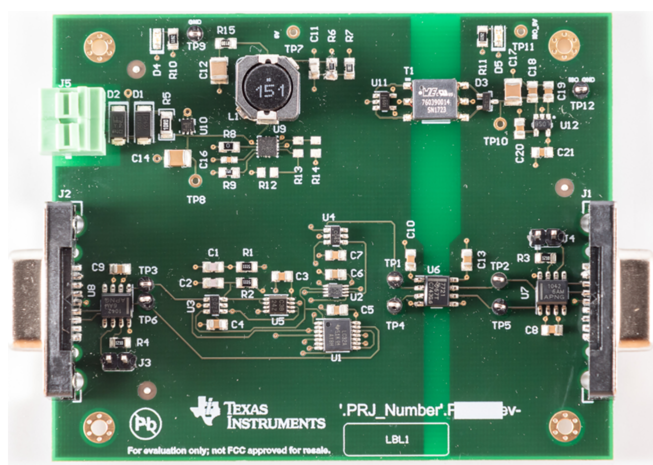
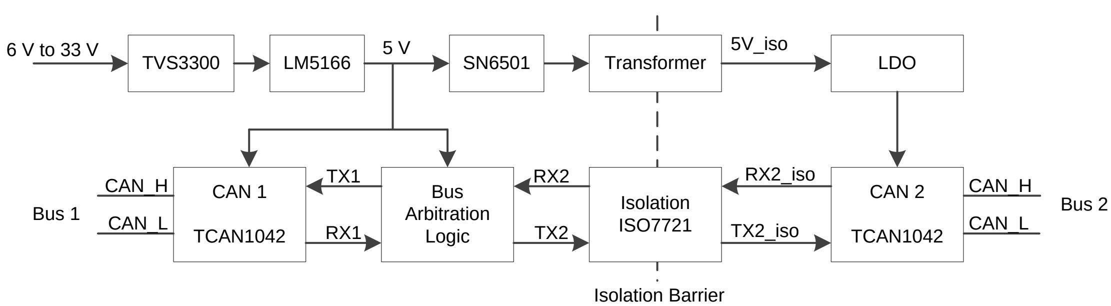
特性

- 隔离式 CAN FD 收发器具有 $3000V_{RMS}$ 隔离等级
- 支持经典 CAN 和 2Mbps CAN FD（灵活数据速率）
- 24V 单工业电源
- 5 至 33V 的宽电源电压范围
- 保护器件免受高功率瞬态或雷击事件的影响
- 板载生成隔离电压

应用

- Fieldbus
- 可编程逻辑控制器 (PLC)
- 工业 I/O 模块
- 通信模块





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TIDUDB5 — http://www-s.ti.com/sc/techlit/TIDUDB5

1 System Description

A Controller Area Network (CAN) bus is an interface for automotive and vehicle applications developed in 1986 by Bosch GmbH. Due to its low cost, the CAN bus is used in factory and process automation to control the production lines. Newly developed products still support the CAN interface to support legacy and factory deployed remote input/output devices, motor drives, sensors, and actuators.

High noise levels on a network bus have the potential to destroy bus transceivers. This noise comes primarily from two sources, ground loops and electrical line surges.

Ground loops occur when bus node circuits at remote locations use their local ground as reference potential. In this case, signal return currents cannot flow back to the ground potential of the sourcing driver on a direct path. Instead they are forced to return through the complex ground network of the electrical installation and, thus, become susceptible to directly coupled, large switching currents of electric machinery. Connecting multiple local grounds directly through a ground wire makes matters worse. Because these grounds often possess significant differences in voltage levels, a low-impedance ground wire causes high, unintended compensation currents to flow, which can damage or destroy components.

Electrical surges are usually the result of inductive-coupled currents into the network cable. In particular, long cable runs are highly susceptible to these surges as the cable might pass electrical equipment switching large currents or might run close to high-current carrying conductors. Other surges include electrostatic discharges (ESD) caused by humans during installation and maintenance work or by direct or indirect lightning strikes. Protecting a network against this destructive energy requires the galvanic isolation of the bus system from the local node circuitry. Modern digital isolators accomplish this goal by incorporating capacitive isolation barriers with up to 5 kV of peak isolation and a transient immunity of up to 50 kV/µs.

Adding bus isolation inside the CAN device protects against dangerous electrical transients and eliminates ground loops. When there is no internal CAN bus isolation, then the device is exposed to the electrical challenges described in this guide. However, isolation still can be added between non-isolated CAN devices by adding an isolated CAN repeater into the CAN bus line.

This TI reference design describes a two-port CAN FD repeater with bus speed up to 2Mbps. This isolated CAN FD repeater reference design adds isolation between the two CAN interfaces and is supplied by a single 24-V industrial voltage supply. The device protects the input power supply from high power transients or lightning strikes with a flat-clamp surge protection device.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	5 to 33 V
CAN bus speed	Up to 2 Mbps
Isolation barrier	3000 V_{RMS} isolation rating

2 System Overview

2.1 Block Diagram

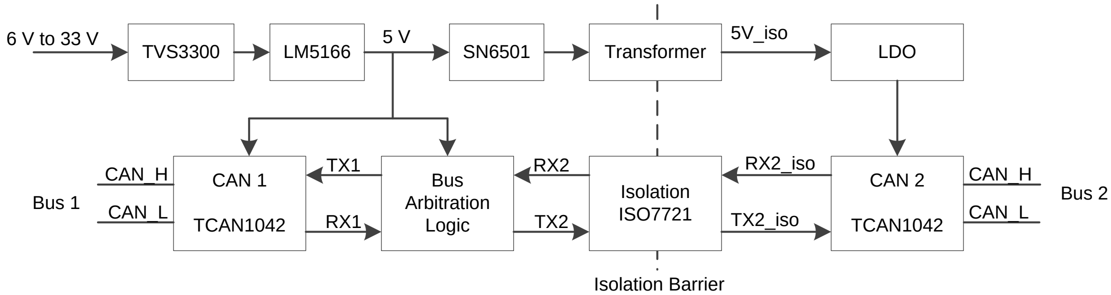

图 1. TIDA-01487 Block Diagram

2.2 Highlighted Products

2.2.1 TCAN1042H

- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- 'Turbo' CAN:
  - All devices support classic CAN and 2Mbps CAN FD (flexible data rate) and "G" options support 5 Mbps
  - Short and symmetrical propagation delay times and fast loop times for enhanced timing margin
  - Higher data rates in loaded CAN networks
- I/O voltage range supports 3.3-V and 5-V MCUs
- Ideal passive behavior when unpowered:
  - Bus and logic terminals are high impedance (no load)
  - Power up or down with glitch free operation on bus and RXD output
- Protection Features:
  - HBM ESD protection: ±16 kV
  - IEC ESD protection: up to ±15 kV
  - Bus fault protection: ±58 V (non-H variants) and ±70 V (H variants)
  - Undervoltage protection on VCC and VIO (V variants only) supply terminals
  - Driver dominant time out (TXD DTO), data rates down to 10 kbps
  - Thermal shutdown protection (TSD)
- Receiver common-mode input voltage: ±30 V
- Typical loop delay: 110 ns
- Junction temperatures from –55°C to 150°C
- Available in SOIC(8) package and leadless VSON(8) package (3.0 mm × 3.0 mm) with improved automated optical inspection (AOI) capability

2.2.2 ISO7721

- Signaling rate: Up to 100 Mbps
- Wide supply range: 2.25 to 5.5 V
- 2.25- to 5.5-V level translation
- Default output high and low options
- Wide temperature range: –55°C to 125°C
- Low power consumption, typical 1.7 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical (5-V supplies)
- High CMTI: ±100 kV/µs typical
- Robust electromagnetic compatibility (EMC):
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Isolation barrier life: > 40 years
- Wide-SOIC (DW-16) and narrow-SOIC (D-8) package options
- Safety-related certifications:
  - VDE reinforced insulation according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5000 V_{RMS} (DW) and 3000 V_{RMS} (D) isolation rating per UL 1577
  - CSA component acceptance notice 5A, IEC 60950-1 and IEC 60601-1 end equipment standards
  - CQC certification per GB4943.1-2011
  - TUV certification according to EN 60950-1 and EN 61010-1
  - VDE, UL, CSA, and TUV certifications for DW package complete; all other certifications planned

2.2.3 LM5166

- Wide input voltage range: 3 to 65 V
- 9.7-µA no-load quiescent current
- Junction temperature range: –40°C to 150°C
- Fixed (3.3-V, 5-V) or adjustable V_{OUT} options
- Meets EN55022 and CISPR 22 EMI standards
- Integrated 1-Ω PFET buck switch:
  - Supports 100% duty cycle for low dropout
- Integrated 0.5-Ω NFET synchronous rectifier:
  - Eliminates external Schottky diode
- Programmable peak current limit supports:
  - 500-mA, 300-mA, or 200-mA loads
- Selectable PFM or constant on-time (COT) mode operation
- 1.223-V ±1.2% internal voltage reference
- Switching frequency up to 600 kHz
- 900-µs internal or externally-adjustable soft start

- Diode emulation and pulse skipping for ultra-high, light-load efficiency
- No loop compensation or bootstrap components
- Precision enable and input UVLO with hysteresis
- Open-drain power good indicator
- Thermal shutdown protection with hysteresis
- Pin-to-pin compatible with the LM5165
- 10-pin, 3-mm×3-mm VSON package

2.2.4 SN6501

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (max)
  - 3.3-V supply: 150 mA (max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

2.2.5 TVS3300

- 33-V, flat-clamp, surge-protection device
- Protects against 1 kV, 42 Ω IEC 61000-4-5 surge test for industrial signal lines
- Max clamping voltage of 40 V at 35 A of 8/20-µs surge current
- Standoff voltage: 33 V
- Survives over 4,000 repetitive strikes of 30-A 8/20-µs surge current at 125°C
- Robust surge protection
  - IEC61000-4-5 (8/20 µs): 35 A
  - IEC61643-321 (10/1000 µs): 4 A
- Small, 1.1-mm^2 WCSP and 4-mm^2 SON footprints

2.3 Design Considerations

The isolated CAN FD repeater design consists of two CAN bus transceivers. Between the two CAN bus transceivers is an isolation barrier and an arbitration logic. The arbitration logic detects which of the two CAN transceivers enter the dominant state first and prevents the loopback of the secondary CAN transceiver side, which would stall the CAN bus into dominant state otherwise.

2.4 System Design Theory

The isolated CAN FD repeater reference design consists of a power supply section, two CAN transceivers devices, CAN bus arbitration logic, and CAN bus isolation device. Each of these subsystems are discussed in the following subsections.

2.4.1 Power Supply

The first stage in the power supply subsystem is the input protection stage.

- Overvoltage protection > 36 V: TVS diode
- Reverse polarity protection: inline diode
- Transient voltage suppression: TVS3300 diode with current limiting resistor

The first stage protects against miss-wiring and high voltage surges of up to 1 kV peak amplitude. High voltage surges can come from source impedance of 42 Ohms to 2 Ohms. Without the high voltage surge protection of the first stage any sensitive electronics can get damaged. A typical protection scheme consists of a bi-directional and miss-wiring safe TVS Diode (D2 in the schematics), which is strong enough to handle the peak current of the voltage surge. With 42 Ohms the peak current is 24 A and with 2 Ohms the peak current is 500 A. Under these circumstances classical TVS diodes still produce a significant overshoot which can reach up to 90 V. After the first TVS diode (D2) there is an in-line diode (D1) for miss-wiring protection and to prevent reverse current during the surge undershoot. A series resistor (R5) limits the peak current and the TVS3300 flat-clamp diode (U10) protects the circuit from the remaining surge overshoot. The filtered voltage at the output of the first stage is guaranteed to never exceed 40V. The LM6166 DC/DC converter (U9) inside the second stage has low current requirements and therefore the series resistor (R5) can have a value of 10 Ohm. If the second stage requires higher current, series resistor (R5) can be reduced to 2 Ohm because high voltage surges can be handled by the limiting resistor inside the TVS3300 flat-clamp diode.

The second stage in the power supply subsystem converts the input voltage of 5 to 33 V to a 5-V supply voltage using the LM5166 DC/DC converter. The circuit is based on the COT reference design of the LM5166. One advantage of the LM5166 is the wide input voltage range from 5 to 33 V for this reference design. The LM5166 also has an ultra-high power conversion efficiency of 93.5% with a 12-V input supply and 250-mA current consumption. The non-isolated voltage supplies one TCAN1042H, the CAN bus arbitration logic, and the primary side of the ISO7721 isolator device.

The isolated voltage supply is generated by the SN6501 transformer driver. An LDO is generating the isolated 5-V supply from the transformer voltage. The isolated 5 V is supplied to the TCAN1042H device and the secondary side of the ISO7721 isolator device on the secondary side.

2.4.2 CAN Transceiver

Two TCAN1042H transceivers are used in this reference design. The TCAN1042H support classic CAN data rates and CAN FD data rates of up to 2Mbps. The RX and TX pins of the two TCAN1042H are going into the arbitration logic.

2.4.3 CAN Bus Arbitration Logic

The CAN bus arbitration logic is needed to prevent both CAN buses to get stuck in dominant state due to the loopback function inside the CAN transceiver devices.

The arbitration logic detects which of the two CAN bus sides is entering the dominant state first. Based on the detection of the first CAN bus side, the arbitration logic blocks the secondary CAN bus side from also asserting dominant state due to the loopback. Once the first CAN bus releases the dominant state the arbitration logic starts a time delay unit. After the time delay unit expires, the block of the secondary side is removed. The arbitration logic works in both CAN bus directions.

The delay line unit has an asymmetric delay of the CAN bus line transition. This unit has only a delay of 210 ns from dominant state to resistive state and no delay from resistive state to dominant state. The asymmetric delay of 210 ns is needed to support higher CAN data rates as 2Mbps.

The CAN bus arbitration logic has been simulated as seen in 图 2. The simulation shows when both sides of the CAN bus interface get into a dominant state. Then the side that stays longer in the dominant state wins the bus arbitration, and the device that enters resistive state goes back to receive mode.

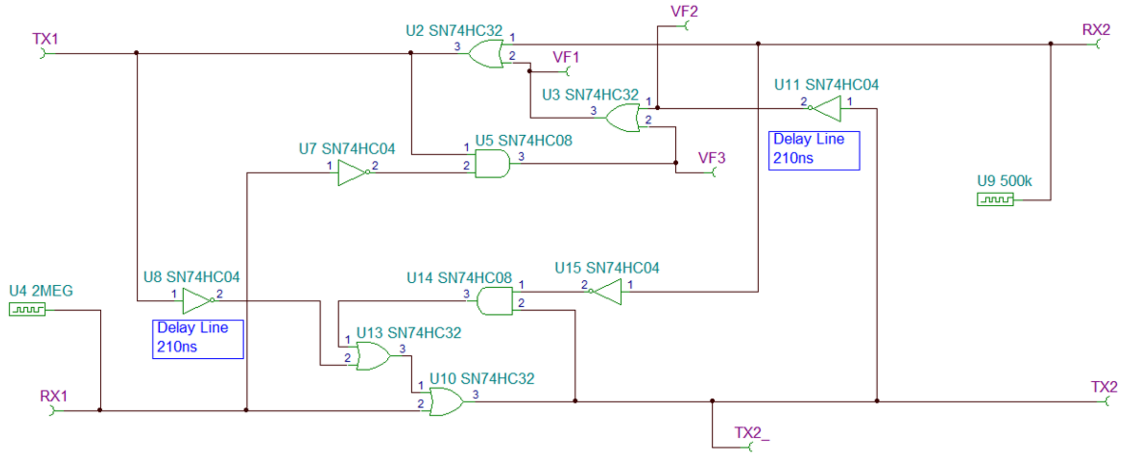

图 2. CAN Bus Arbitration Logic Circuit

The stimulus on the left side is a 2-Mbps square wave signal and on the right side a slower 500-kHz square wave signal. Note that the stimulus are not CAN signals because they do not detect dominant state and switch off driving the bus. The two stimulus are mainly used to test the initial arbitration of the CAN bus arbitration logic.

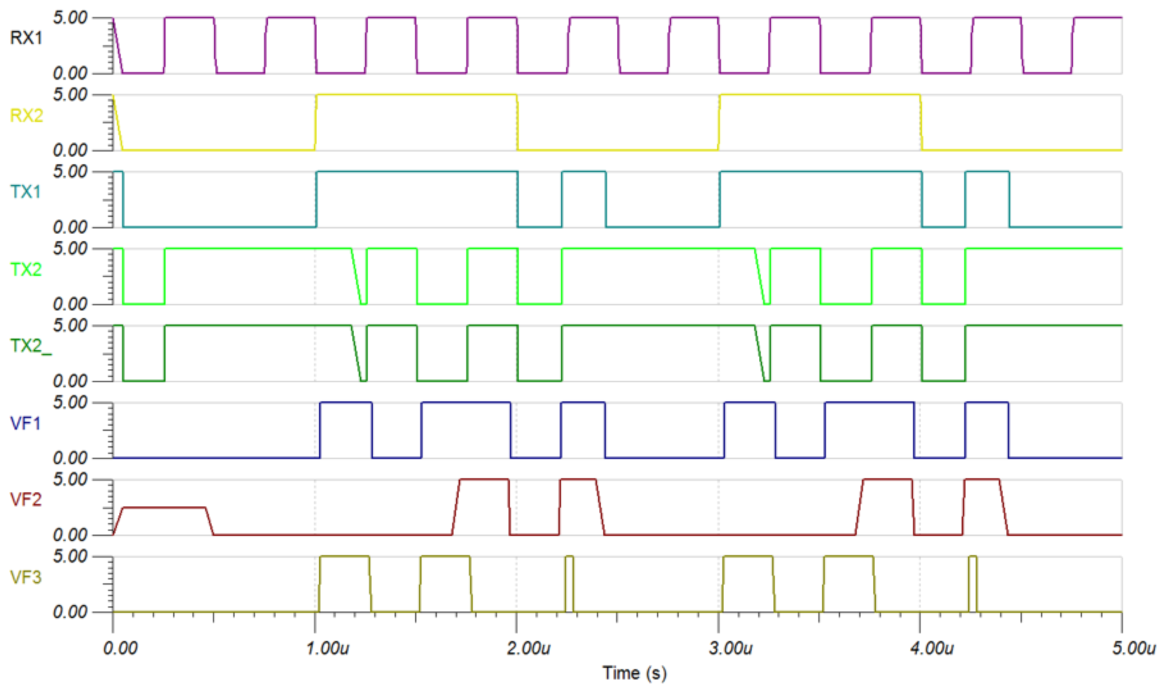

图 3. Arbitration Logic Simulation Results

The secondary side (RX2) stays longer in the dominant state and therefore is in favor of the arbitration detection logic.

图 4 is the simulation of the asymmetric time delay unit.

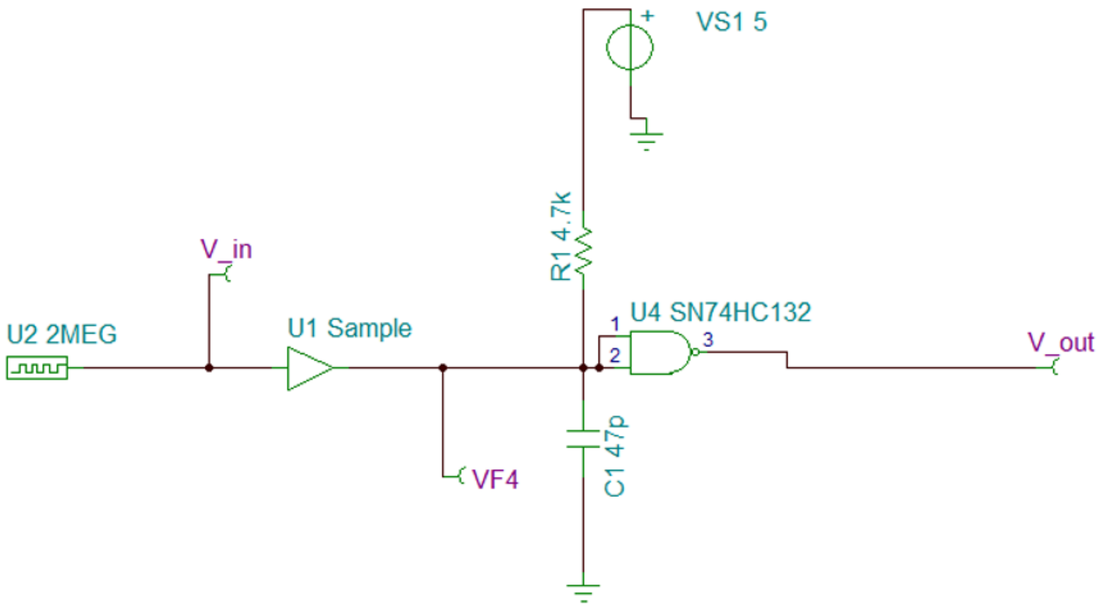

图 4. Delay Logic Circuit

The time delay unit simulation results are shown in 图 5. The capacitor is charged (VF4) when the CAN bus transitions from dominant state to resistive state (V_in). When the voltage VF4 reached the threshold, the time delay unit set V_out to high. As the time delay unit is asymmetric, there is no delay when V_in goes to low and V_out goes immediately low, too.

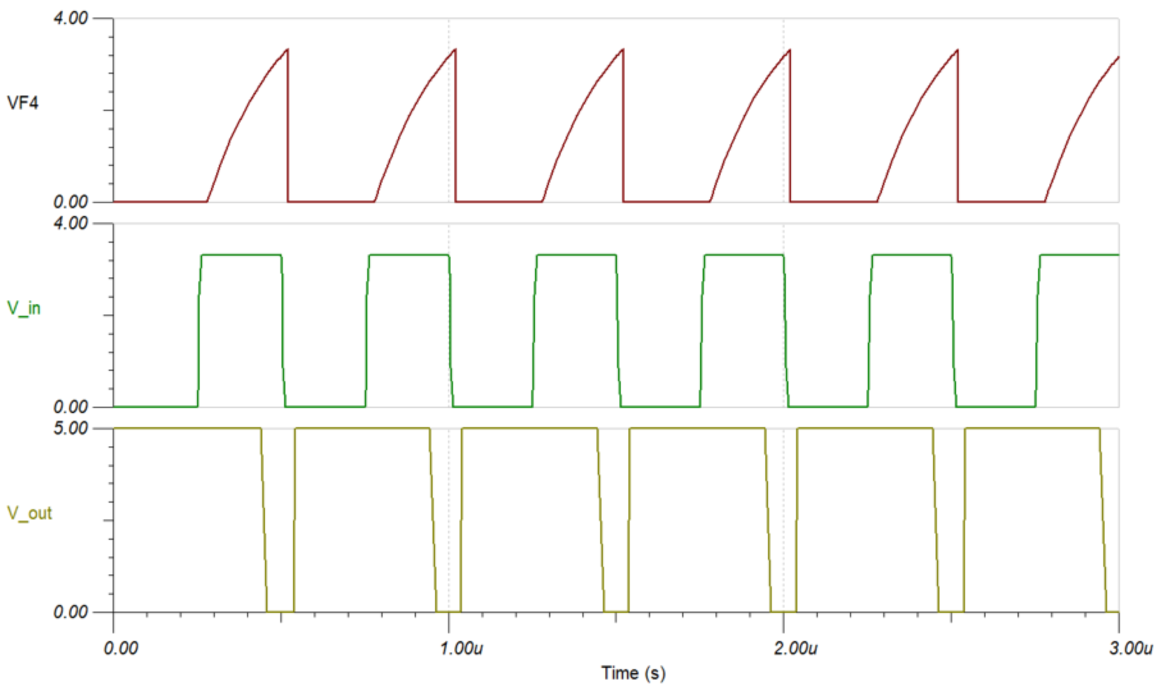

图 5. Delay Logic Simulation Results

2.4.4 CAN Bus Isolation Logic

The ISO7721 device has been chosen for this reference design as it supports two data lines, one in each direction. The ISO7721 device isolates the two CAN transceiver signals RX and TX between the two CAN busses. The ISO7721 device supports 3000 V of isolation with the SOIC (D) package. Note that if a higher isolation voltage is required, then the SOIC (DW) package has to be used.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

Connect a 24-V power supply to J5 of the isolated CAN FD repeater board. Switch the power supply.

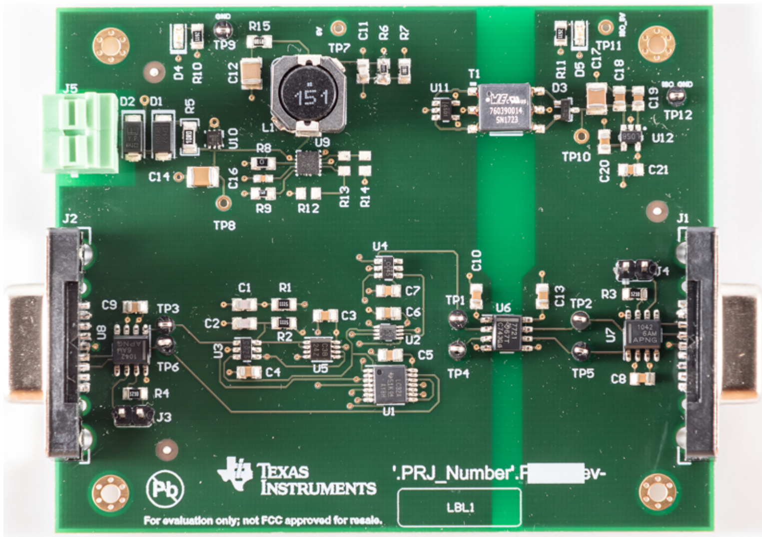

图 **6. TIDA-01487 Board**

Place the isolated CAN FD repeater board in between a CAN bus, which must get isolated. Connect the 9-pin Sub-D connector J1 to the primary side and J2 to the secondary side.

3.2 Testing and Results

The isolated CAN FD repeater has been validated with two TIDA-01406 CAN open reference designs, which operate on BeagleBone Black.

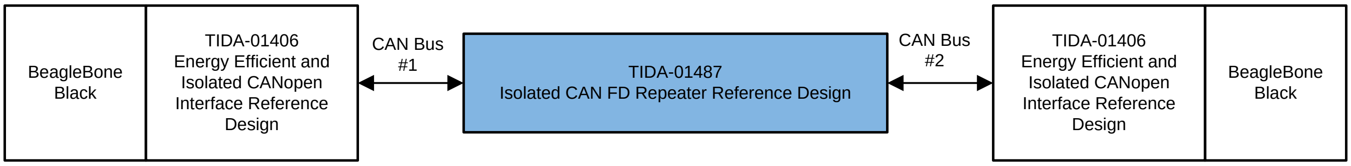

图 7. TIDA-01487 Test Setup

3.2.1 CAN Communication

图 8 shows CAN bus communication between CAN1 to CAN2 at 1 Mbps.

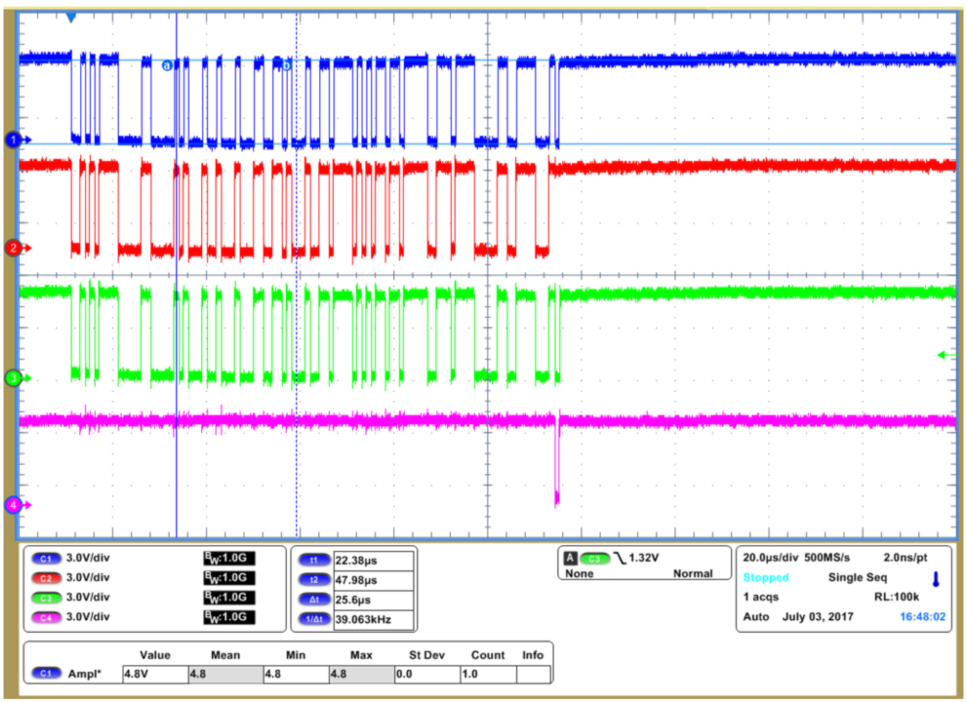

图 8. Communication CAN1 to CAN2 at 1 Mbps

Scope channel legend:

- Channel 1: RX1 at TP6
- Channel 2: TX2_ at TP4
- Channel 3: RX2_ at TP1
- Channel 4: TX1 at TP3

The arbitration logic detects that Channel 1 (RX1) gets into a dominant state first. The CAN frame is routed from CAN bus 1 to CAN bus 2. At the end of the CAN frame, the CAN bus 2 acknowledges the reception by pulling the bus 2 to dominant state—this can be seen on Channel 4. The bus acknowledge pulse can be observed on Channel 1 and Channel 2.

图 9 shows CAN bus communication between CAN bus 2 to CAN bus 1 at 1 Mbps.

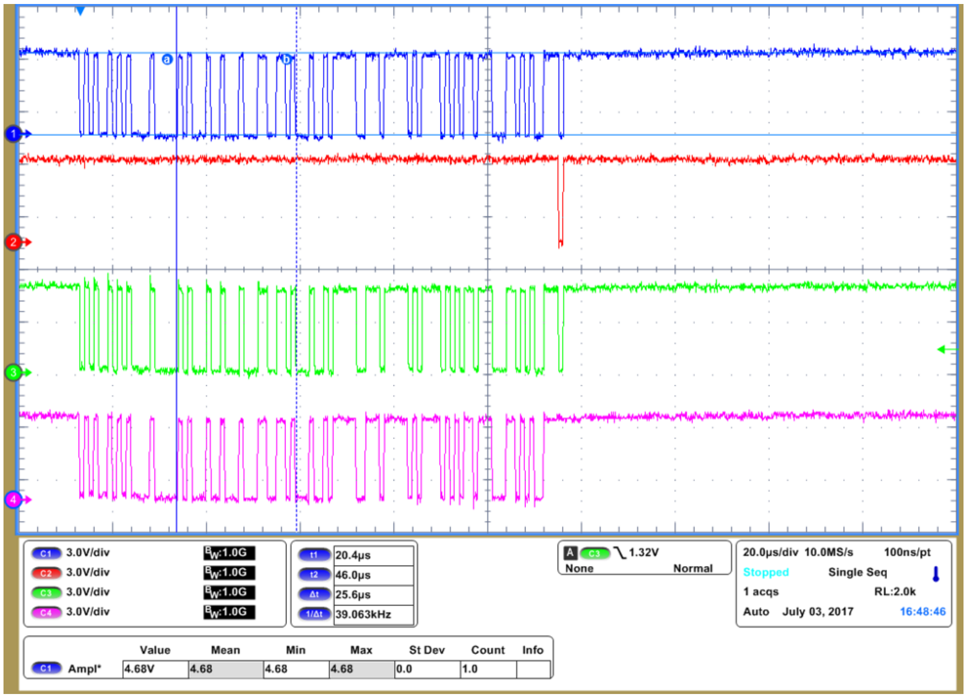

图 **9. Communication CAN Bus 2 to CAN Bus 1 at 1 Mbps**

Scope channel legend:

- Channel 1: RX1 at TP6
- Channel 2: TX2_ at TP4
- Channel 3: RX2_ at TP1
- Channel 4: TX1 at TP3

The arbitration logic detects that Channel 1 (RX1) gets into a dominant state first. The CAN frame is routed from CAN bus 1 to CAN bus 2. At the end of the CAN frame, the CAN bus 2 acknowledges the reception by pulling the bus 2 to a dominant state—this can be seen on Channel 2. The bus acknowledge pulse can be observed on Channel 1 and Channel 3.

3.2.2 Delay Line Logic

图 10 and 图 11 show the signal delay added by the delay line logic. This delay line logic operates asynchronous, meaning it adds a 228-ns delay from the dominant state to resistive state, and a 2.8-ns delay from the resistive state to dominant state.

- Channel 1: TP3
- Channel 2: U7, pin 7

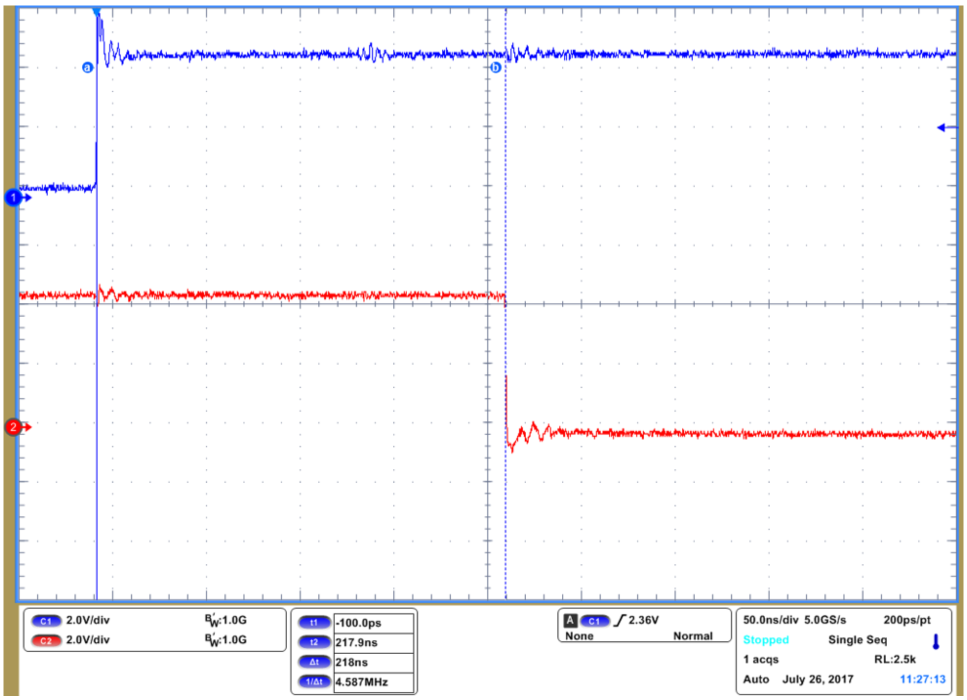

图 10. Delay From Resistive State to Dominant State

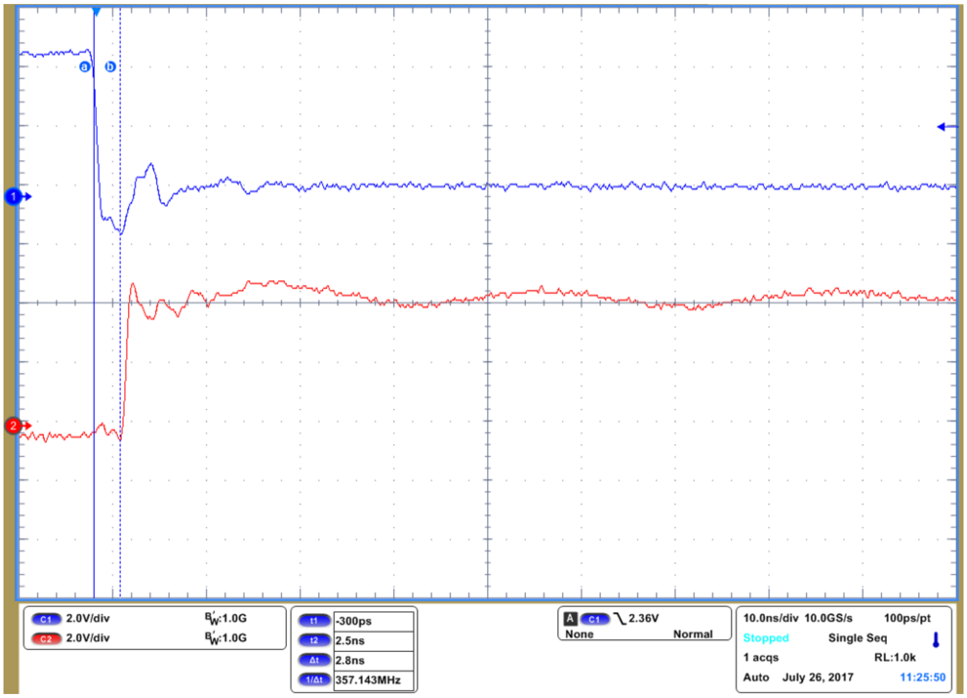

图 **11. Delay From Dominant State to Resistive State**

3.2.3 CAN Transceiver Loopback

图 12 and 图 13 show the TCAN1042H loopback delay. The TX line gets dominant until the CAN transceiver loops back the signal on the RX line. The delay measured is 86.6 ns for CAN 1 (U8) and 88.5 ns for CAN 2 (U7).

- Channel 1: TP3
- Channel 2: TP6

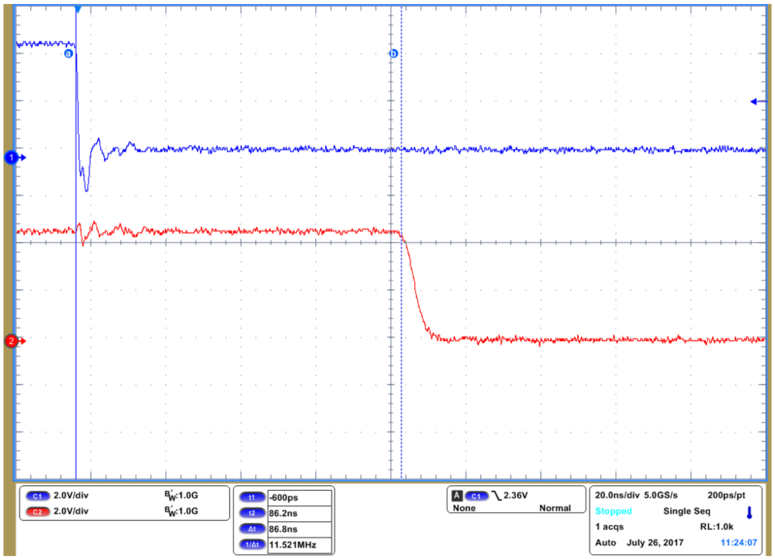

图 12. Loopback Delay CAN 1

- Channel 1: TP5
- Channel 2: TP2

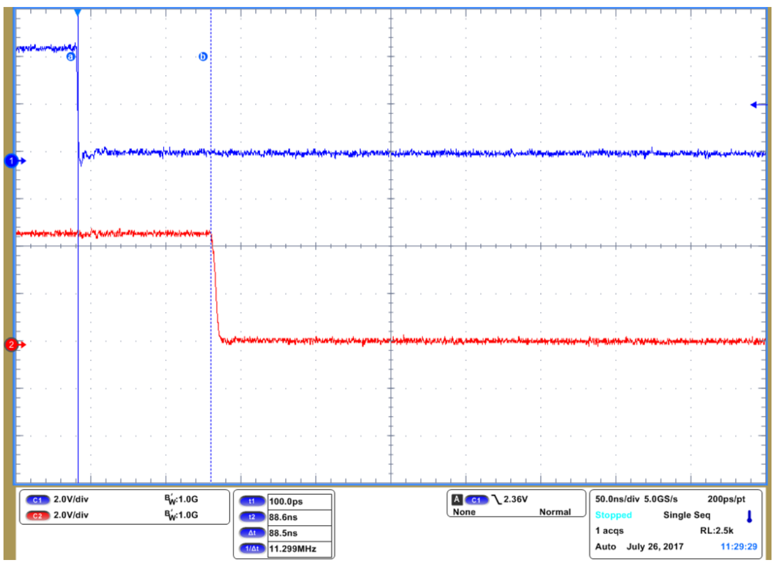

图 13. Loopback Delay CAN 2

3.2.4 CAN Isolation Delay

图 14 shows the ISO7721 and the CAN 2 loopback delay. This is a total of 108.5 ns. By subtracting the CAN 2 loopback delay of 88.5 ns, the ISO7721 has a round-trip delay of 20 ns, or 10 ns for one direction.

- Channel 1: TP4
- Channel 2: TP1

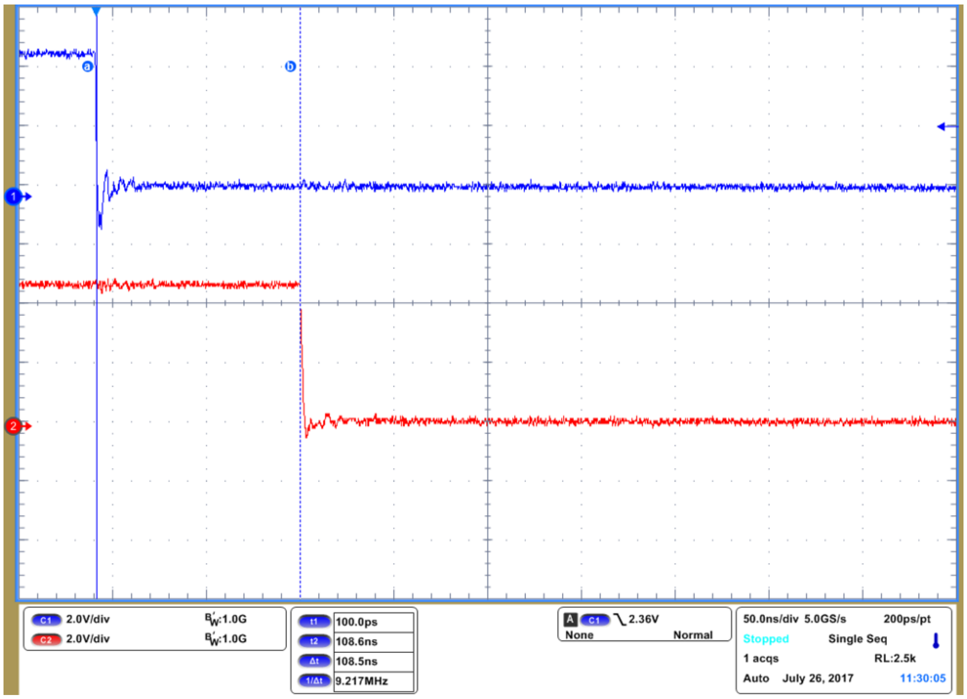

图 14. ISO7721 and CAN 2 Delay

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01487.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01487.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01487.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01487.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01487 .

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01487.

5 Software Files

To download the software files, see the design files at TIDA-01487.

6 Related Documentation

1. Texas Instruments, *Energy Efficient and Isolated CANopen Interface Reference Design for PLC and Communication Modules*, TIDA-01406 design guide
2. Texas Instruments, *LM5166EVM-C50A Evaluation Module*, user's guide
3. Texas Instruments, *TVS0500-3300 Adapter Board*, TVS3300 Evaluation Module (TVS-00EVM)

6.1 商标

7 About the Author

THOMAS MAUER is a system engineer in the Factory Automation and Control Team at Texas Instruments Freising. He is responsible for developing reference design solutions for the industrial segment. Thomas brings his extensive experience in industrial communications like Industrial Ethernet, fieldbuses, and industrial applications to this role. Thomas earned his degree in electrical engineering (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany

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Changes from Original (August 2017) to A Revision **Page**

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122