TI Designs：TIDA-01466
适用于超声波模拟前端的低电压低噪声电源参考设计

说明

该参考设计是一款经过优化的电源，用于为超声波成像系统的八个 16 通道 AFE IC 供电。该电源设计通过使用单芯片直流/直流转换器 + LDO 组合稳压器以及将每个 LDO 输入设置为恰好高于压降来减少部件数，同时最大限度地提高效率。超低噪声 LDO 有助于实现更高的模数转换分辨率，从而实现更高的图像质量。该设计允许频率与系统时钟同步，从而允许设计人员应用滤波技术以消除接地回路上的电源开关噪声或使用扩频时钟以降低 EMI。该设计实现了电子保险丝 IC，从而提供简单灵活的过流保护。

资源

TIDA-01466	设计文件夹
TPS54122-Q1	产品文件夹
TPS54824	产品文件夹
TPS7A84	产品文件夹
TPS7A8300	产品文件夹
LM3881	产品文件夹
CDCLVC1106	产品文件夹
TPS25926	产品文件夹
TLV704	产品文件夹

TI E2E™ Community

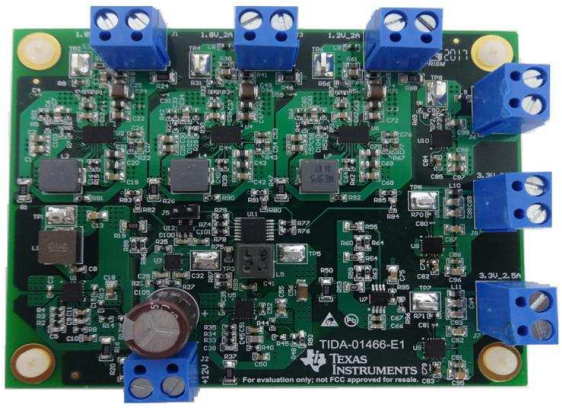
咨询我们的 E2E 专家

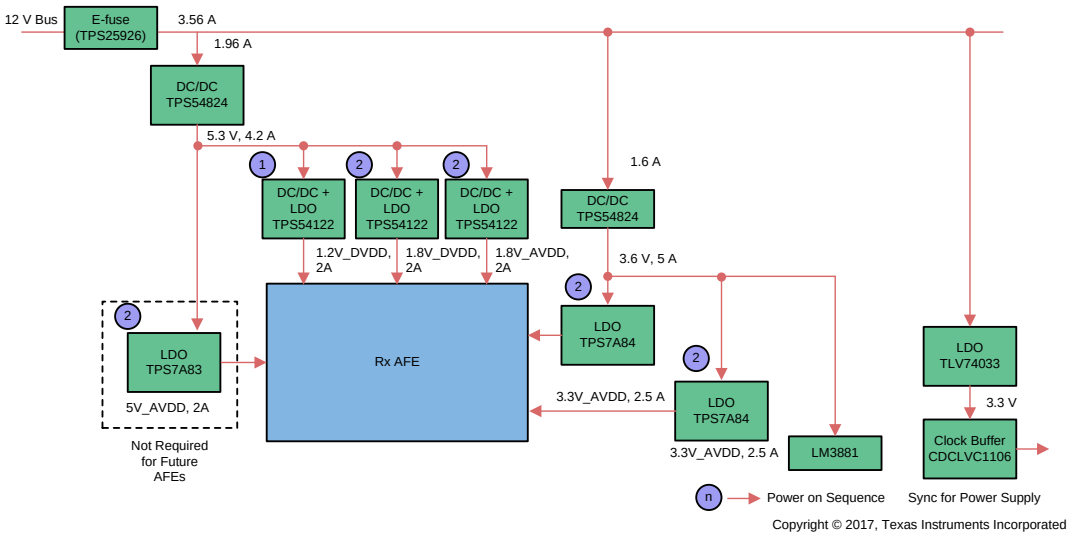
特性

- 适用于 12V 输入超声波系统前端
- 具有输入电流限制为 4.2A 的电子保险丝
- 能够为八个 AFE 供电，通道多达 128 个（可扩展通道数），支持 36W 功率输出
- 组合直流/直流转换器 + LDO IC 可通过将 LDO 输入设置为恰好高于压降电压来最大限度地提高 LDO 效率
- 使用高 PSRR 和超低噪声 (4.4μV_{RMS}) LDO 来实现可能的最高模数转换分辨率
- 在同一块 T/R 板上为所有 AFE 提供共用的同步电源，从而减小布板空间，同时有助于降低噪声和消除 EMI

应用

- 医用超声波扫描仪
- 声纳成像设备
- 无损评价设备





1 System Description

Ultrasound imaging systems use high-frequency sound waves (several MHz or more) to image internal structures by the differing reflection signals produced when a beam of sound waves is projected into the body and bounces back at the interfaces between those structures. Ultrasound diagnosis differs from radiological diagnosis in that there is no ionizing radiation involved. The use of ultrasound to create images is based on the reflection and transmission of a wave at a boundary. When an ultrasound wave travels inside an object that is made up of different materials (such as the human body), each time it encounters a boundary (for example, between bone and muscle, or muscle and fat), part of the wave is reflected and part of it is transmitted. The reflected rays are detected and used to construct an image of the object.

图 1 shows the block diagram of an ultrasound imaging system. An ultrasound imaging system has a transmitter section and a linear or pulse transmitter section, which generates excitation pulses for ultrasound transducers of frequencies typically ranging from 1 to 15 MHz of amplitude ±2.5 to ±100 V. On the transmit (Tx) side, the Tx beamformer determines the delay pattern and pulse train that set the desired transmit focal point. Ultrasound transducers are piezoelectric transducers that undergo mechanical deformation on the application of electrical pulses, which in turn produces an ultrasound waveform. The process is also reversible, and it can convert ultrasound to electrical energy. The reflected signal received transducer is conditioned by the receiver analog front end (AFE). The AFE is usually integrated with a voltage controlled amplifier (VCA), a low-noise amplifier (LNA), PGA, and an analog-to-digital converter (ADC). The AFE produces digitized output that is given to the receive beamformer FPGA and then to the DSP for processing, image forming, and displaying. On the receive (Rx) side, there is a T/R switch, generally a diode bridge, that blocks the high-voltage Tx pulses. This switch is followed by an LNA and one or more variable-gain amplifiers (VGAs), which implement time gain compensation (TGC). Time gain control—which provides increased gain for signals from deeper in the body (and therefore arriving later)—is under operator control and used to maintain image uniformity.

As continuous wave (CW) Doppler has the largest dynamic range of all signals in an ultrasound system—during CW, a sine wave is transmitted continuously with half of the transducer array while the other half is receiving. There is a strong tendency for the Tx signal to leak into the Rx side; there are also strong reflections coming from stationary body parts that are close to the surface. This tends to interfere with examination of, for example, blood flow in a vein deep in the body along with very weak Doppler signals. At its current state, CW Doppler signals cannot be processed through the main imaging (B-mode) and pulsed wave (PW) Doppler (F-mode) path in a digital beamforming system; for this reason, images can be formed as a sequence of analog levels that are delayed with analog delay lines, summed, and converted to digital after summation, indicated as CW Doppler processing. The Rx AFE also integrates CW mixer and a low-noise summer to form a CWD beamformer. LNA output is passed through the CW mixer to demodulate the Doppler frequencies and produce I and Q signals. These I and Q signals from all the channels in the same AFE are summed at a low-noise summer. Sixteen selectable phase delays can be applied to each analog input signal. The most common use of ultrasound, creating images, has industrial and medical applications. Ultrasound systems has different forms or variants available in the market including cart based, portable, or handheld.

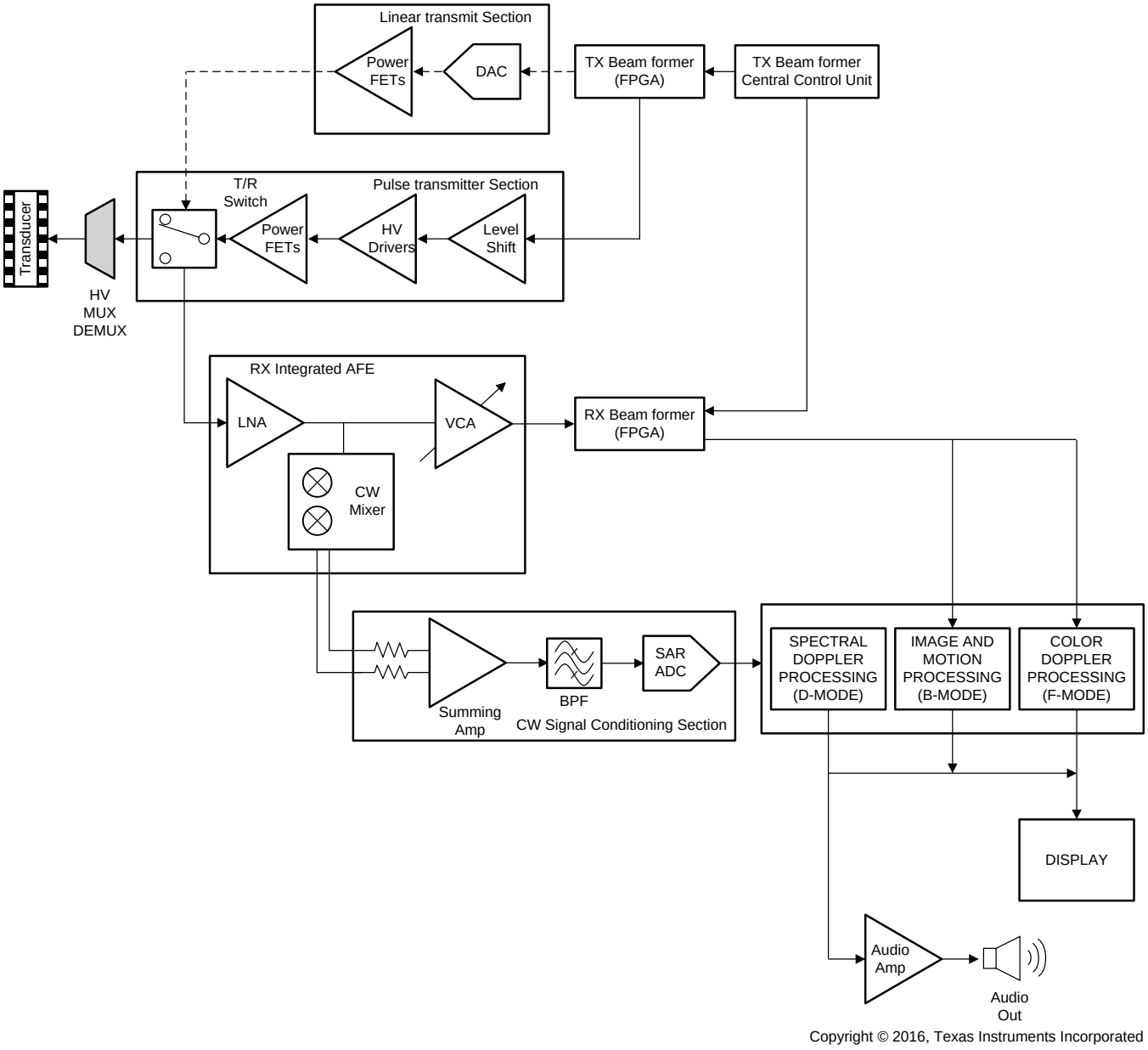


图 1. Ultrasound Imaging System Block Diagram

This reference design is a power supply optimized specifically for providing power to eight 16-channel receive AFE ICs for ultrasound imaging systems. This design uses single-chip DC-DC converter + LDO combo regulators to obtain maximum efficiency by setting the low dropout (LDO) input just above the dropout voltage while taking full advantage of the LDO PSRR and reducing part count. In addition, ultra-low-noise LDOs helps to attain highest resolution possible from A/D conversion, leading to higher image quality. This reference design is capable of switching frequency synchronization with the master and system clock frequency to aid system designers apply simple filtering techniques to remove power supply switching noise on ground loops or use spread-spectrum clocking to reduce EMI. Additionally, the design implements an eFuse IC, providing a simple and flexible means of overcurrent protection.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage (V)	12 V
OUTPUT VOLTAGES (V)	
Vout_1, Iout_1	5 V, 2 A
Vout_2, Iout_2	3.3 V, 2.5 A
Vout_3, Iout_3	3.3 V, 2.5 A
Vout_4, Iout_4	1.8 V, 2 A
Vout_5, Iout_5	1.8 V, 2 A
Vout_6, Iout_6	1.2 V, 2 A
LOAD REGULATION	
Vout_1 (5 V)	0.04%
Vout_2 (3.3V_1)	0.091%
Vout_3 (3.3V_2)	0.06%
Vout_4 (1.8V_1)	0.78%
Vout_5 (1.8V_2)	0.723%
Vout_6 (1.2V)	0.90%
OUTPUT VOLTAGE NOISE (dBm)	
Vout_5V	Max –60.04 dBm at 524 kHz
Vout_3V3	Max –73.23 dBm at 524 kHz
Vout_1V8	Max –50.23 dBm at 480 kHz
Vout_1V2	Max –60.47 dBm at 476.2 kHz
Rated output power (W)	36.1 W
Efficiency	91.20%
Protections	The overall power exceeds 50-W eFuse cuts of, this sets a limit of 4.2 A

2 System Overview

2.1 Block Diagram

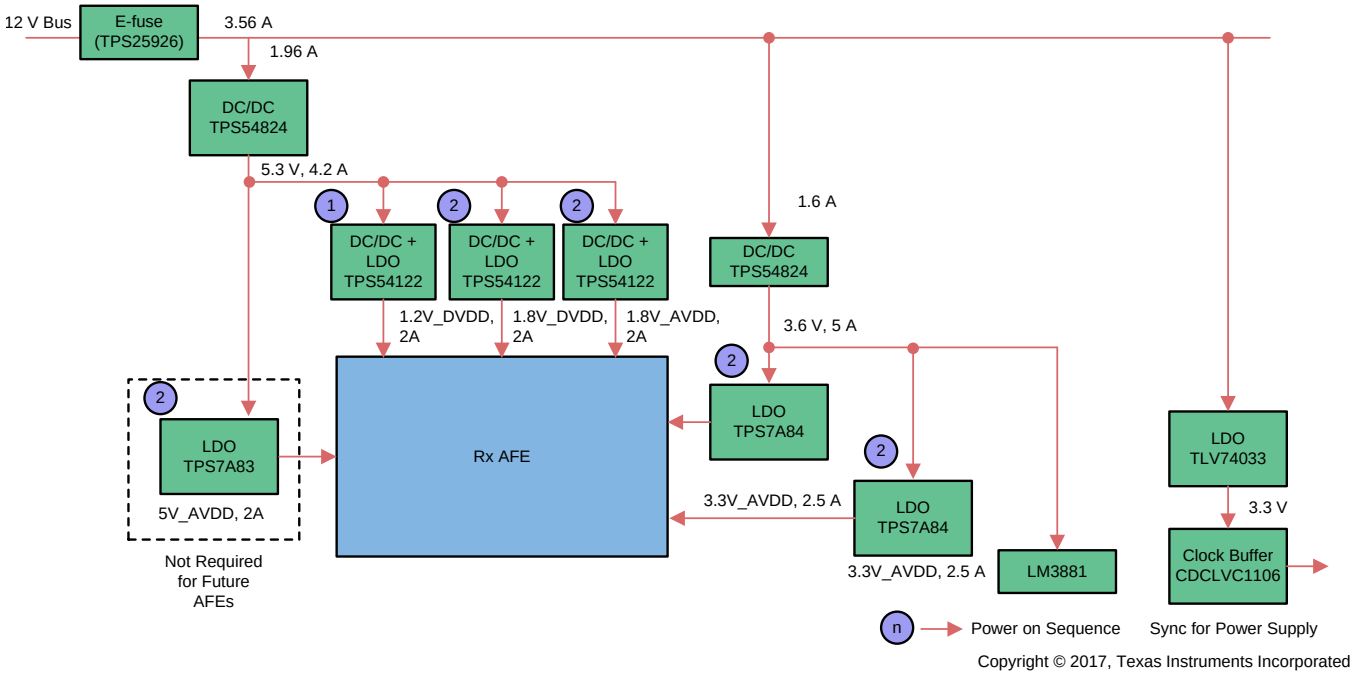


图 2. TIDA-01466 Block Diagram

2.2 Highlighted Products

2.2.1 TPS54122

The TPS54122 device combines the efficiency of a step-down switching (DC-DC) converter with a high power-supply rejection (PSR), low-noise, LDO to provide an ultra-low-noise power supply that delivers QuietSupply™ rails to noise-sensitive applications. The TPS54122 device is ideally suited for systems with 5-V power buses and can support 3-A continuous output current on both the DC-DC or LDO output. The LDO output voltage can be set from 0.8 to 3.6 V and the DC-DC can be adjusted from 0.83 to 5.0 V using external resistors. The TPS54122 device can be used in a wide range of low-noise applications because the DC-DC converter and LDO are completely configurable. In addition, the TPS54122 device includes features such as soft-start, switching frequency synchronization, and a power-good signal. The TPS54122 device can also be configured as a dual-supply rail device, supplying a total of 3 A. The TPS54122 device is available in a space-saving, 3.50-mm×5.50-mm VQFN package, and is specified to operate over a –40°C to 125°C ambient temperature range.

2.2.2 TPS54824

The TPS54824 is a full featured 17-V, 8-A synchronous step-down converter in a 3.5-mm×3.5-mm HotRod™ QFN package. The device is optimized for small solution size through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through peak current mode control, which reduces component count, and by selecting a high switching frequency, which reduces the inductor footprint. The peak current mode control simplifies the loop compensation and provides fast transient response. Cycle-by-cycle peak current limiting on the high-side and low-side sourcing current limit protects the device in overload situations. Hiccup limits MOSFET power dissipation if

a short circuit or overloading fault persists. A power good supervisor circuit monitors the regulator output. The PGOOD pin is an open drain output and goes high impedance when the output voltage is in regulation. An internal deglitch time prevents the PGOOD pin from pulling low unless a fault has occurred. A dedicated EN pin can be used to control the regulator on/off and adjust the input undervoltage lockout. The output voltage startup ramp is controlled by the SS/TRK pin, which allows operation as either a standalone power supply or in tracking situations.

2.2.3 TPS7A84

The TPS7A84 is a low-noise (4.4 μV_{RMS}) LDO capable of sourcing 3 A with only 180 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 to 3.95 V and adjustable from 0.8 to 5.0 V using an external resistor divider. The combination of low noise (4.4 μV_{RMS}), high PSRR, and high-output current capability makes the TPS7A84 ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of the TPS7A84 limits power-supply-generated phase noise and clock jitter, making this device ideal for powering high-performance serializer and deserializer (SerDes), ADCs, digital-to-analog converters (DACs), and RF components. Specifically, RF amplifiers benefit from the high-performance and 5.0-V output capability of the device. For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input, low-output (LILO) voltage operation, the exceptional accuracy (0.75% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A84 ensure optimal system performance. The versatility of the TPS7A84 makes the device a component of choice for many demanding applications.

2.2.4 TPS7A83

The TPS7A83A device is a low-noise (4.4 μV_{RMS}) LDO capable of sourcing 2 A with only 200 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 to 3.95 V and adjustable from 0.8 to 5.2 V using an external resistor divider. The combination of low noise (4.4 μV_{RMS}), high PSRR, and high-output current capability makes the TPS7A83A ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of the TPS7A83A limits power-supply-generated phase noise and clock jitter, making this device ideal for powering high-performance SerDes, ADCs, DACs, and RF components. Specifically, RF amplifiers benefit from the high-performance and 5.2-V output capability of the device. For digital loads (such as ASICs, FPGAs, and DSPs) requiring LILO voltage operation, the exceptional accuracy (0.75% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A83A ensure optimal system performance. The versatility of the TPS7A83A makes the device a component of choice for many demanding applications.

2.2.5 LM3881

The LM3881 Simple Power Sequencer offers the easiest method to control the power-up and power-down of multiple power supplies (switching or linear regulators). By staggering the start-up sequence, it is possible to avoid latch conditions or large inrush currents that can affect the reliability of the system. Available in VSSOP-8 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. When the LM3881 is enabled, the three output flags sequentially release after individual time delays, thus permitting the connected power supplies to start up. The output flags follow a reverse sequence during power down to avoid latch conditions. Time delays are defined using an external capacitor, and the output flag states can be inverted by the user.

2.2.6 TLV70433

The TLV704 series of LDO regulators are ultra-low quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power microcontrollers, such as the MSP430™ MCU. The TLV704 operates over a wide operating input voltage of 2.5 to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients. The TLV704 is available in a 3-mm × 3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.

2.2.7 TPS25926

The TPS25925x/TPS25926x family of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current. Current limit level can be set with a single external resistor and current limit set has a typical accuracy of ±15%. Overvoltage events are limited by internal clamping circuits to a safe fixed maximum with no external components required. TPS25926x devices provide overvoltage protection (OVP) for 12-V systems and TPS25925x devices for 5-V systems. In cases with particular voltage ramp requirements, a dV/dT pin is provided that can be programmed with a single capacitor to ensure proper output ramp rates.

2.2.8 CDCLVC1106

The CDCLVC11xx is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments. The entire family is designed with a modular approach in mind. It is intended to round up TI's series of LVCMOS clock generators. Seven different fan-out variations, 1:2 to 1:12, are available. All of the devices are pin-compatible to each other for easy handling. All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range. The CDCLVC11xx supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low. The CDCLVC11xx family operates in a 2.5-V and 3.3-V environment and are characterized for operation from –40°C to 85°C.

2.3 System Design Theory

This reference design is a power supply designed for providing power to eight 16-channel receive AFEs of 12-V ultrasound Imaging systems. This design is based on the specifications of the TI Ultrasound AFE, AFE5818. 表 2 shows the specification summary of eight AFE5818 devices for a 128-channel ultrasound system.

表 2. Specification Summary of 8 AFE5818 for 128-Channel System

AFE RAIL	V_{IN}	V_{OUT}	CURRENT (SINGLE AFE ONLY)	CURRENT (128 CHANNELS, 8 AFEs)	SOLUTION
AVDD_5V	12 V	5 V	0.14 A	1.12 A	Buck + High PSRR LDO
AVDD_3V3	12 V	3.3 V	0.5 A	4 A	Buck + High PSRR LDO
AVDD_1V8	12 V	1.8 V	0.2 A	1.6 A	Buck + DC-DC and LDO
AVDD_1P2	12 V	1.2 V	0.2 A	1.6 A	Buck + DC-DC and LDO

表 2. Specification Summary of 8 AFE5818 for 128-Channel System (continued)

AFE RAIL	V_{IN}	V_{OUT}	CURRENT (SINGLE AFE ONLY)	CURRENT (128 CHANNELS, 8 AFEs)	SOLUTION
AVDD_1P8	12 V	1.8 V	0.15 A	1.2 A	Buck + DC-DC and LDO

This reference design has three low-noise DC-DC converter + LDO combos (TPS54122) to provide 1.2 DVDD, 1.8 DVDD, and 1.8 AVDD for the AFEs, a low-dropout voltage regulator (TPS7A83) to provide 5 AVDD, a high-current, high-accuracy, low-noise LDO voltage regulator (TPS7A84) to provide 3.3 AVDD, and two 8-A synchronous swift step-down converters (TPS54824) to generate the input voltages (5.6 V and 3.6 V) for TPS54122, TPS7A83, and TPS7A84. This reference design also uses a power sequencer with adjustable timing (LM3881) for the power sequencing of AFE5818. A low-jitter 1:6 LVCMOS fan out clock buffer (CDCLVC1106) acts as a clock signal fan out buffer for external clock in sync mode for all the DC-DC converters used on board. A 12-V, accurate adjustable current limit eFuse (TPS25926) provides multiple protections. A 24-V, 150-mA, ultra-low I_Q LDO regulator (TLV70433) provides power to the clock buffer.

2.3.1 5.6-V Generation Using DC-DC Converter

图 3 shows the switching circuit to generate 5.6 V using the TPS54824 from a 12-V input. This 5.6 V is used as input for the LDO TPS7A83 for 5-V generation and input to the DC-DC + LDO combo TPS54122 for 1.8 DVDD, 1.8 AVDD, and 1.2 DVDD generation. The TPS54824 DC-DC is a synchronous buck converter designed to provide up to 4.2 A.

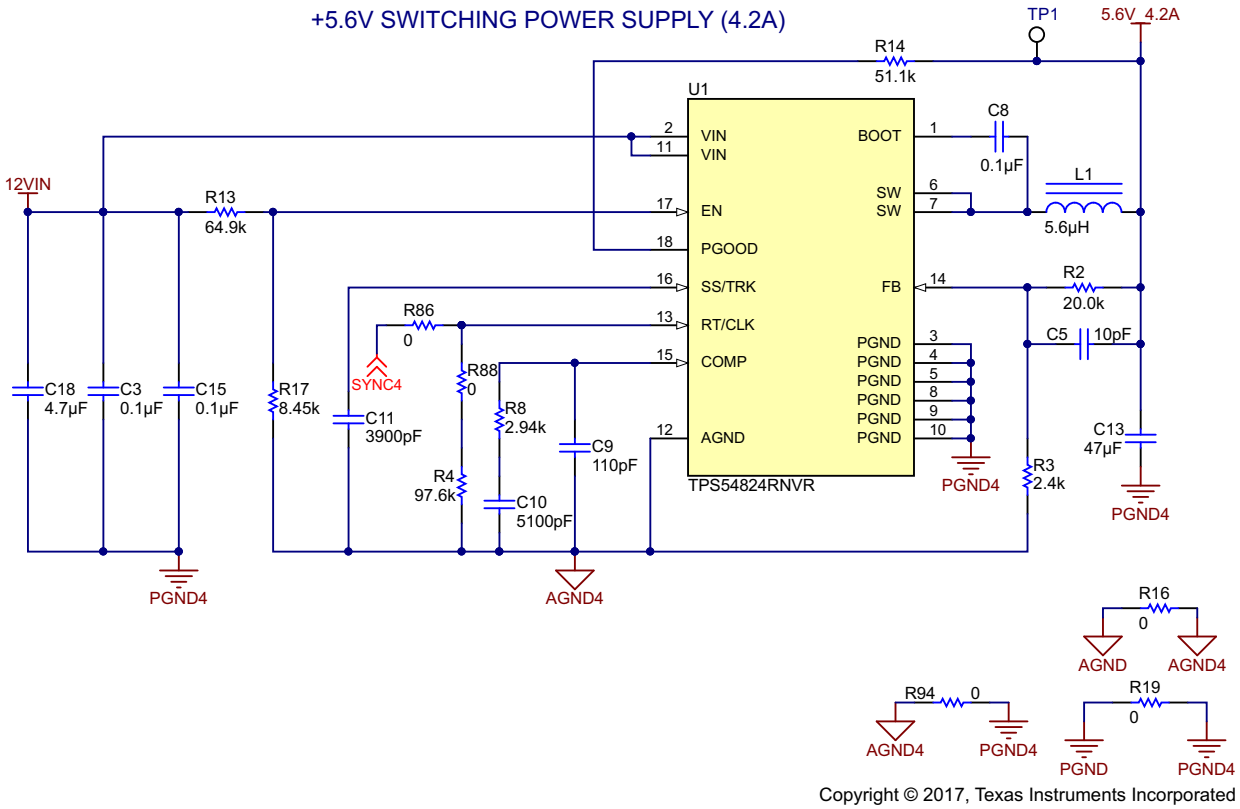


图 3. 5.6-V Generation Using DC-DC Converter

2.3.1.1 Voltage Set Point

The output voltage is set by the resistor divider network of R2 and R3, and the reference voltage V_{REF} is 0.6 V. Output voltage can be calculated using 公式 1.

$$R2 = R3 \times \left(\frac{V_{OUT}}{0.6\ V} - 1 \right) \quad (1)$$

Where:

- R2 = 20 kΩ
- R3 = 2.4 kΩ

Substituting R2 and R3 in 公式 1 gives:

$$V_{OUT} = \left(\frac{20\ k\Omega}{2.4\ \ k\Omega} + 1 \right) \times 0.6\ V = 5.6\ V$$

2.3.1.2 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can set the switching frequency of the device in two modes: RT and CLK.

In RT mode, the R4 (R_T) resistor is connected between the RT/CLK pin and GND. The switching frequency of the device can be adjustable by using a resistor R4 (RT) of value, which ranges from 50 to 150 kΩ based on the inductor rating chosen for the DC-DC converter. To determine the value of the RT resistor for a given switching frequency (F_{SW}), use 公式 2.

$$F_{SW}\ (\text{kHz}) = 43660 \times R_T\ (\text{k}\Omega)^{-0.973} \quad (2)$$

Where:

- R4 = 97.6 kΩ

Substituting R4 in 公式 2 gives:

F_{SW} (kHz) = 43660 × $97.6^{-0.973}$ = 506 kHz

2.3.1.3 CLK Mode

In CLK mode, an external clock is connected through the clock buffer (U11) to the RT/CLK pin. The DC-DC converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The DC-DC converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 200 and 1600 kHz and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 35 ns. The clock signal amplitude must transition from lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of the RT/CLK pin.

In this reference design, 0-Ω resistors R86 and R88 are used on board to select between RT/CLK mode. Placing R86 resistor sets external sync and placing R88 sets CLK mode. See the TPS54824 datasheet (SLVSDC9) for more details.

2.3.1.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R13 and R17. See the TPS54824 datasheet (SLVSDC9) for detailed instructions for setting the external UVLO. Additionally, the TPS54824 provides adjustable soft start and a power good output.

See the TPS54824 datasheet (SLVSDC9) and TPS54824 EVM user's guide (SLVUAX8) for the detailed design instructions and recommendations. See the Texas Instruments WEBENCH® Design Center for generating solutions using this part.

2.3.2 3.6-V Generation Using DC-DC Converter

图 4 shows the switching circuit to generate 3.6 V using TPS54824 from a 12-V input. This 3.6 V is used as input for the two LDOs (TPS7A84) to generate 3.3 V. The TPS54824 DC-DC is a synchronous buck converter designed to provide up to 5 A.

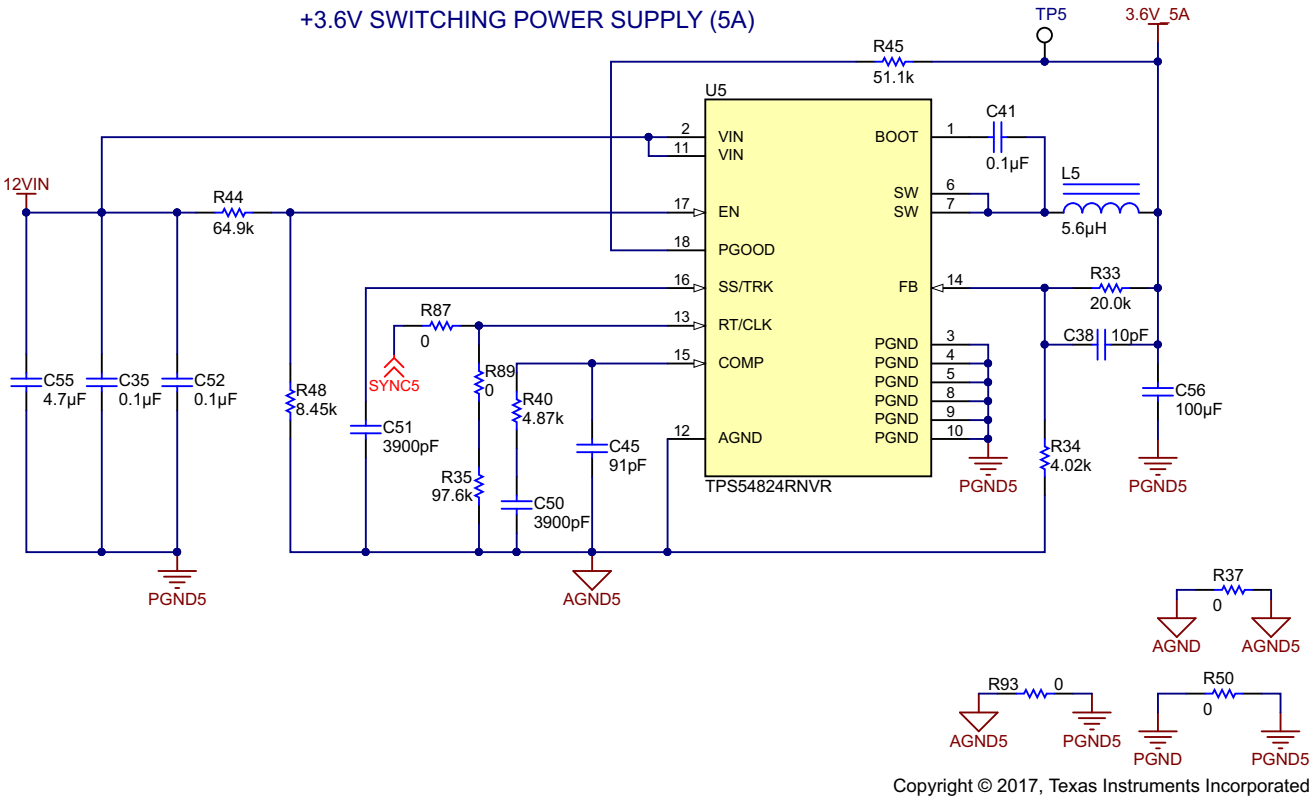


图 4. 3.6-V Generation Using DC-DC Converter

2.3.2.1 *Voltage Set Point*

The output voltage is set by the resistor divider network of R33 and R34 and the reference voltage (V_{REF}) is 0.6 V. Output voltage can be calculated using 公式 3.

$$R33 = R34 \times \left(\frac{V_{OUT}}{0.6\ V} - 1 \right) \quad (3)$$

Where:

- R33 = 20 kΩ
- R34 = 4.02 kΩ

Substituting R33 and R34 in 公式 3 gives:

$$V_{OUT} = \left(\frac{20\ k\Omega}{4.02\ k\Omega} + 1 \right) \times 0.6\ V = 3.6\ V$$

2.3.2.2 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can set the switching frequency of the device in two modes: RT and CLK.

In RT mode, the R35 (RT) resistor is connected between the RT/CLK pin and GND. The switching frequency of the device can be adjustable by using a resistor R35 (RT) of value, which ranges from 50 to 150 kΩ based on the inductor rating chosen for the DC-DC converter. To determine the value of the RT resistor for a given switching frequency (F_{SW}), use 公式 4.

$$F_{SW}\ (kHz) = 43660 \times R_T\ (k\Omega)^{-0.973} \quad (4)$$

Where:

- R35 = 97.6 kΩ

Substituting F_{SW} in 公式 4 gives:

F_{SW} (kHz) = 43660 × $97.6^{-0.973}$ = 506 kHz

2.3.2.3 CLK Mode

See 节 2.3.1 for CLK mode operation using the TPS54824.

In this reference design, 0-Ω resistors R87 and R89 are used on board to select between RT/CLK mode. Placing an R87 resistor sets external sync, and placing R89 sets CLK mode. See the TPS54824 datasheet (SLVSDC9) for more details

2.3.2.4 Adjustable UVLO

The UVLO can be adjusted externally using R44 and R48. See the TPS54824 datasheet (SLVSDC9) for detailed instructions for setting the external UVLO. Additionally, the TPS54824 provides adjustable soft start and a power good output.

See the TPS54824 datasheet and TPS54824 EVM user's guide (SLVUAX8) for the detailed design instructions and recommendations. See the Texas Instruments WEBENCH Design Center for generating solutions using this part.

2.3.3 1.2-V and 1.8-V Generation Using DC-DC Converter + LDO

图 5 shows the TPS54122 DC-DC + LDO combo circuit to generate 1.2 DVDD from a 5.6-V input. The TPS54122 is designed to provide up to 2 A. With the TPS54122's flexibility of having a DC-DC converter and an LDO in a single device, it is possible to obtain maximum LDO efficiency by setting LDO input just above the dropout voltage. This demonstrates the printed circuit board (PCB) space saving compared to standalone switcher and LDO topologies. The TPS54122 device combines the efficiency of a step-down switching (DC-DC) converter with a high power-supply rejection (PSR), low-noise, LDO to provide an ultra-low-noise power supply that delivers quiet supply rails. LDO is kept 0.5 V for good PSRR with a DC-DC converter output of 1.7 V.

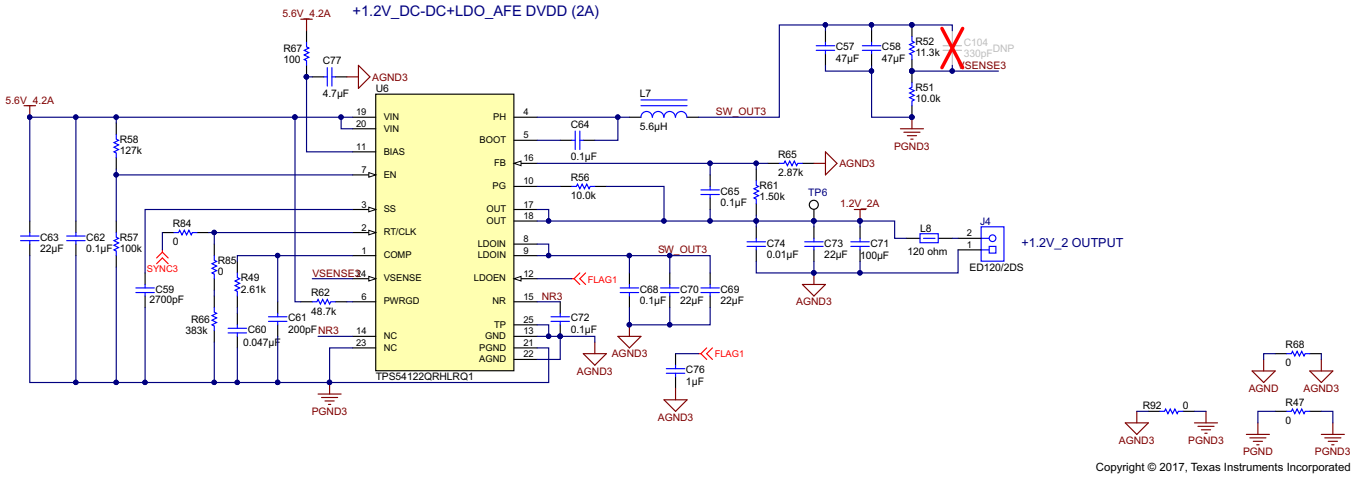


图 5. 1.2-V Generation Using TPS54122

2.3.3.1 DC-DC Converter Output Voltage Set Point

The switcher output voltage can be set using 公式 5.

$$R52 = R51 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (5)$$

Where:

- R52 = 11.3 kΩ
- R51= 10 kΩ
- V_{REF} = 0.827 V

Substituting R52, R51, and V_{REF} in 公式 5 gives:

$$V_{OUT} = \left(\frac{11.3\,k\Omega}{10\,k\Omega} + 1 \right) \times 0.827\ V = 1.76\ V$$

2.3.3.2 LDO Output Voltage Set Point

The LDO output voltage can be set using 公式 6.

$$R61 = R65 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (6)$$

Where:

- R61 = 1.5 kΩ
- R65= 2.87 kΩ
- V_{REF} = 0.8 V

Substituting R61, R65, and V_{REF} in 公式 6 gives:

$$V_{OUT} = \left(\frac{1.5\,k\Omega}{2.87\,k\Omega} + 1 \right) \times 0.8\ V = 1.218\ V$$

2.3.3.3 Adjustable Switching Frequency and Synchronization (RT/CLK)

In RT mode, the R66 (RT) resistor is connected between the RT/CLK pin and GND. The switching frequency of the device can be adjustable by using a resistor R66 (RT) of value, which ranges from 350 to 450 kΩ based on the inductor rating chosen for the DC-DC converter. To determine the value of the RT resistor for a given switching frequency (F_{SW}), use 公式 7.

$$R_T\ (k\Omega) = 311890 \times F_{sw}\ (kHz)^{-1.0793} \quad (7)$$

Where:

- R_T = R66 = 383 kΩ

Substituting R_T = 383 kΩ in 公式 7 gives F_{SW} = 500 kHz.

2.3.3.4 CLK Mode

In CLK mode, an external clock is connected through the clock buffer (U11) to the RT/CLK pin. The DC-DC converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The DC-DC converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 300 kHz and 2 MHz and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 75 ns. The clock signal amplitude must transition to less than 0.6 V and to greater than 1.6 V. The PH rising edge is synchronized to the RT/CLK pin falling edge. In applications where the RT mode and CLK mode are required, the device can be configured to have an RT resistor and an external clock connected at the same time to the RT/CLK pin. If no external clock is present, the device functions in RT mode and the switching frequency is set by the R66 (RT) resistor.

The EN pin of the 1.2-V LDO is connected to the output (Flag1) of LM3881 as per the sequencing requirement of AFE5818 mentioned in 节 2.3.6.

In this reference design, 0-Ω resistors R84 and R85 are used on board to select between RT/CLK mode. Placing an R84 resistor sets external sync and placing R85 sets CLK mode.

2.3.3.5 Soft-Start of DC-DC Converter

The rate at which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin. The CSS capacitor is connected between the SS pin and ground. The size of the capacitor determines the soft-start ramp-up time (t_{SS}, 10% to 90%), as shown in 公式 8.

$$t_{SS}\ (ms) = \frac{\left(C_{SS}\ (nF) \times V_{REF}\ (V)\right)}{I_{SS}\ (\mu A)} \quad (8)$$

Where:

- V_{REF} (V) = 0.827 V
- C_{SS} (nF) = 2.7 nF
- I_{SS} (µA) = 2.2 µA

Substituting V_{REF} (V), C_{SS} (nF), and I_{SS} (µA) in 公式 8 gives:

$$t_{SS} = \frac{(2.7 \times 0.827)}{2.2} = 1.01\ ms$$

The device has an internal pullup current source (I_{SS}) of 2.2 µA that charges the external soft-start capacitor, C_{SS}. The voltage reference, V_{REF}, for this device is 0.827 V. By sourcing a constant current onto the capacitor, the device linearly ramps up the voltage on the SS pin that corresponds to the voltage on the FB pin, and thus, the output voltage of the switcher. When the voltage on the SS pin exceeds the value of the internal reference, the device starts regulating to the internal reference value. If the input UVLO is triggered (or the EN pin is pulled below 1.21 V or a thermal shutdown event occurs), then the device stops switching and enters low-current operation. At the subsequent power-up when the shutdown condition is removed, the DC-DC does not start switching until the SS pin is discharged to ground, ensuring proper soft-start behavior.

2.3.3.6 NR Soft-Start Time and LDO Start-Up

The primary purpose of the NR capacitor is to filter the noise from the LDO band gap and thereby reduce the LDO output noise. However, the NR capacitor affects the start-up time of the LDO. The TPS54122 device has a soft-start circuit to charge CNR at a controlled rate for a monotonic soft-start. The controlled voltage ramp of the output reduces peak inrush current during start-up.

The soft-start ramp time depends on the soft-start charging current (I_{NR}), the external noise-reduction capacitor (CNR), and the internal voltage reference of the LDO and can be calculated as shown in 公式 9.

$$t_{SS}\left(ms\right) = 1096 \times CNR\left(\mu F\right) \tag{9}$$

Where:

- CNR (µF) = 0.1 µF

Substituting CNR (µF) in 公式 9 gives:

t_{SS} (ms) = 1096 × 0.1 µF = 109.6 ms

In this reference design, the delay between 1.2 V and all other rails (1.8 AVDD, 1.8 DVDD, 5 AVDD, 3.3 AVDD) is set as 50 ms by choosing the Tadj capacitor (C75) as 47 nF. The LM3881 is powered using the 3.6-V TPS7A84 LDO. Keep the delay sufficiently large such that the tolerances of the capacitors do not make the second voltage override the first due to the soft start.

See the TPS54122 datasheet (SLVSDC9) and TPS54122 EVM user's guide (SLVUAX8) for the detailed design instructions and recommendations. See the Texas Instruments WEBENCH Design Center for generating solution using this part. The DC-DC converter equivalent part for the TPS54122 is the TPS54319, which can be used in webench for simulation.

Both the switcher and the LDO have independent protection and control features such as internal current limit, thermal shutdown, power good signal, and enable circuitry.

图 6 shows the TPS54122 DC-DC + LDO combo circuit to generate 1.8 DVDD/1.8 AVDD from a 5.6-V input. The TPS54122 is designed to provide up to 2 A. With the TPS54122's flexibility of having a DC-DC converter and LDO in a single device, it is possible to obtain maximum LDO efficiency by setting LDO input just above dropout voltage. This demonstrates the PCB space saving compared to standalone switcher and LDO topologies. The TPS54122 device combines the efficiency of a step-down switching (DC-DC) converter with a high PSR, low-noise LDO to provide an ultra-low-noise power supply that delivers quiet supply rails. The LDO is kept 0.5 V for good PSRR with a DC-DC converter output of 2.3 V.

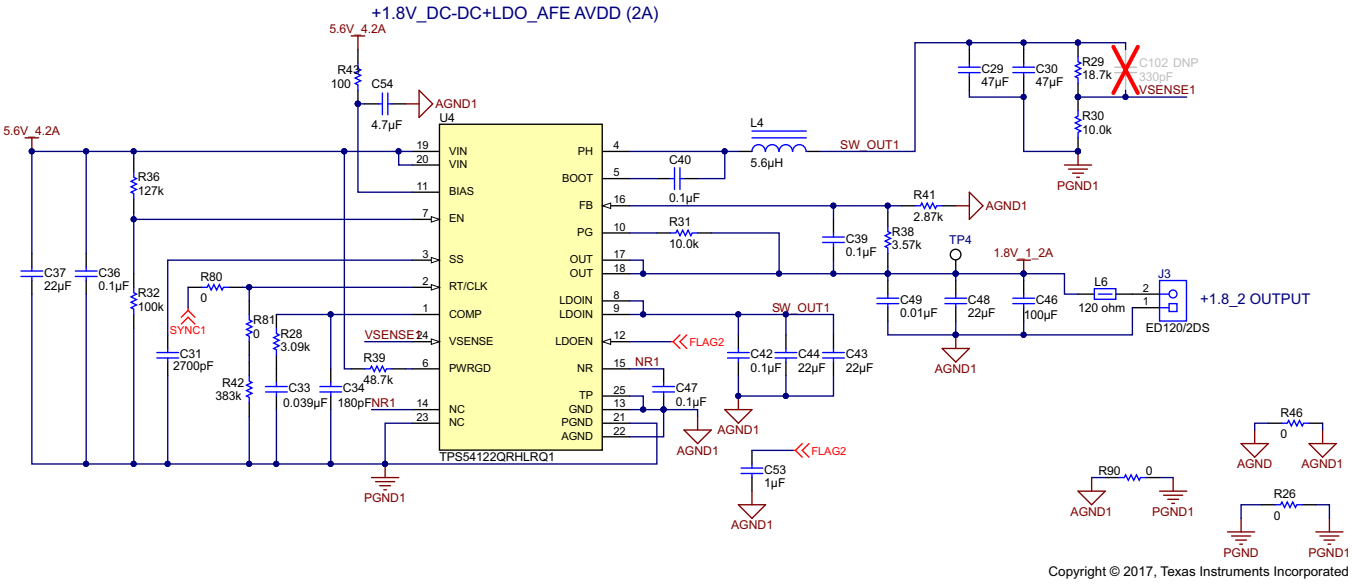


图 6. 1.8-V Generation Using TPS54122

2.3.3.7 DC-DC Converter Output Voltage Set Point

The switcher output voltage can be set using 公式 10:

$$R29 = R30 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (10)$$

Where:

- R29 = 18.7 kΩ
- R30= 10 kΩ
- V_{REF} = 0.827 V

Substituting R29, R30, and V_{REF} in 公式 10 gives:

V_{OUT} = (18.7 /10 + 1) × 0.827 = 2.37 V $V_{OUT} = \left(\frac{18.7}{10} + 1 \right) \times 0.827\ V = 2.37\ V$

2.3.3.8 LDO Output Voltage Set Point

The LDO output voltage can be set using 公式 11:

$$R38 = R41 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (11)$$

Where:

- R38 = 3.57 kΩ
- R41 = 2.87 kΩ
- V_{REF} = 0.8 V

Substituting R38, R41, and V_{REF} in 公式 11 gives:

$$V_{OUT} = \left(\frac{3.57\ k\Omega}{2.87\ k\Omega} + 1 \right) \times 0.8 = 1.79$$

2.3.3.9 Adjustable Switching Frequency and Synchronization (RT/CLK)

In RT mode, the R42 (RT) resistor is connected between the RT/CLK pin and GND. The switching frequency of the device can be adjustable by using a resistor R42 (RT) of value, which ranges from 350 to 450 kΩ based on the inductor rating chosen for the DC-DC converter. To determine the value of the RT resistor for a given switching frequency (F_{SW}), use 公式 12.

$$R_T\,(\text{kHz}) = 311890 \times F_{sw}\,(\text{kHz})^{-1.0793} \tag{12}$$

Where:

- R_T = R42 = 383 kΩ

Substituting R_T = 383 kΩ in 公式 12 gives F_{SW} = 500 kHz.

2.3.3.10 CLK Mode

In CLK mode, an external clock is connected through the clock buffer (U11) to the RT/CLK pin. The DC-DC converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The DC-DC converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 300 kHz and 2 MHz and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 75 ns. The clock signal amplitude must transition to less than 0.6 V and to greater than 1.6 V. The PH rising edge is synchronized to the RT/CLK pin falling edge. In applications where the RT mode and CLK mode are required, the device can be configured to have an RT resistor and an external clock connected at the same time to the RT/CLK pin. If no external clock is present, the device functions in RT mode and the switching frequency is set by the R42 (RT) resistor.

The EN pin of the 1.8-V LDO is connected to the output (Flag2) of LM3881 as per the sequencing requirement of AFE5818 mentioned in 节 2.3.6.

In this reference design, 0-Ω resistors R80 and R81 are used on board to select between RT/CLK mode. Placing R80 resistor sets external sync and placing R81 sets CLK mode

Both the switcher and the LDO have independent protection and control features such as soft start, internal current limit, thermal shutdown, power good signal, and enable circuitry.

See the TPS54122 datasheet (SLVSDC9) and TPS54122 EVM user's guide (SLVUAX8) for the detailed design instructions and recommendations. See the Texas Instruments WEBENCH Design Center for generating solution using this part. The DC-DC converter equivalent part for TPS54122 is TPS54319, which can be used in webench for simulation.

2.3.4 3.3-V Generation Using LDO

图 7 shows the LDO circuit to generate 3.3 V from a 3.6-V input using the TPS7A84. Two such circuits are used to provide the total 5-A requirement of eight AFEs. To have an optimal PSRR, 0.3-V LDO is set for the TPS7A83.

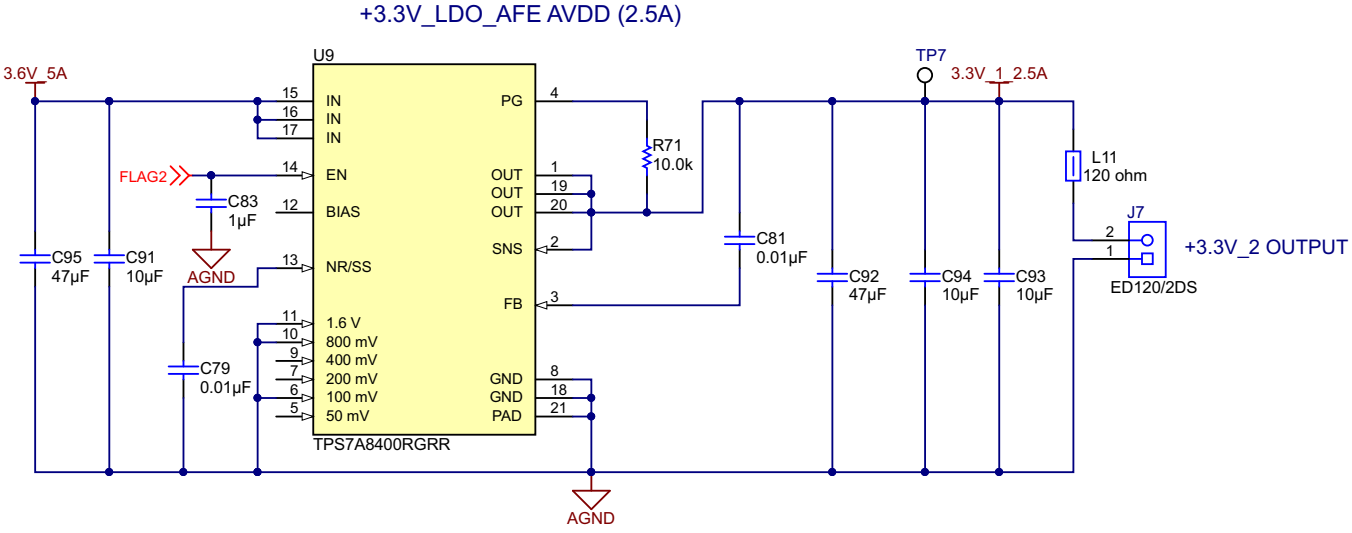


图 7. 3.3-V Generation Using TPS7A84

2.3.4.1 Output Voltage Set

The TPS7A84 can use either external resistors or the internally-matched ANY-OUT feedback resistor network to set output voltage. The ANY-OUT resistors are accessible through pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin is can be connected to ground (active) or left open (floating), or connected to SNS. ANY-OUT programming is set by 公式 13 as the sum of the internal reference voltage (VNR / SS = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin. In this reference design 1.6 V (pin 11), 800 mV (pin 10), 100 mV (pin 6) plus V_{REF} of 0.8 V gives a 3.3-V output; the voltages at each pin are 50 mV (pin 5), 100 mV (pin 6), 200 mV (pin 7), 400 mV (pin 9), 800 mV (pin 10), or 1.6 V (pin 11). 表 3 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF}.

$$V_{OUT} = V_{REF} + (\varepsilon \text{ ANY OUT Pins to Ground}) \quad (13)$$

表 3. ANY OUT Programmable Output Voltage

PIN	VALUE
Pin 5	50 mV
Pin 6	100 mV
Pin 7	200 mV
Pin 9	400 mV
Pin 10	800 mV
Pin 11	1.6 V

There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected to ground using 0-Ω resistors (or left open), or hardwired by the given layout of the PCB to set the ANY-OUT voltage. Using the ANY-OUT network allows the TPS7A8300 to be programmed from 0.8 to 3.95 V. The EN pin of the 3.3-V LDO is connected to the output (Flag2) of the LM3881 as per the sequencing requirement of the AFE5818 mentioned in 节 2.3.6.

See the TPS7A84 datasheet (SBVS233) and TPS7A84 EVM (SBVU028) for detailed design instructions and recommendations. See the Texas Instruments WEBENCH Design Center for generating solution using this part.

2.3.5 5-V Generation Using LDO

图 8 shows the LDO circuit to generate 5 V from a 5.6-V input using the TPS7A83. To have an optimal PSRR, 0.6-V LDO is set for the TPS7A83.

2.3.5.1 Output Voltage Set

The TPS7A8300 can be used either with the internal ANY-OUT network or using external resistors. Using the ANY-OUT network allows the TPS7A8300 to be programmed from 0.8 to 3.95 V. To extend this range of output voltage operation to 5.0 V, external resistors must be used. 公式 14 shows how to set the output voltage in adjustable output operation.

$$R73 = R72 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (14)$$

Where:

- V_{REF} = 0.8 V

- R73 = 105 kΩ
- R72 = 20 kΩ

Substituting V_{REF}, R73, and R72 in 公式 14 gives V_{OUT} = 5 V. The EN pin of the 5-V LDO is connected to the output (Flag2) of the LM3881 as per the sequencing requirement of the AFE5818 mentioned in 节 2.3.6.

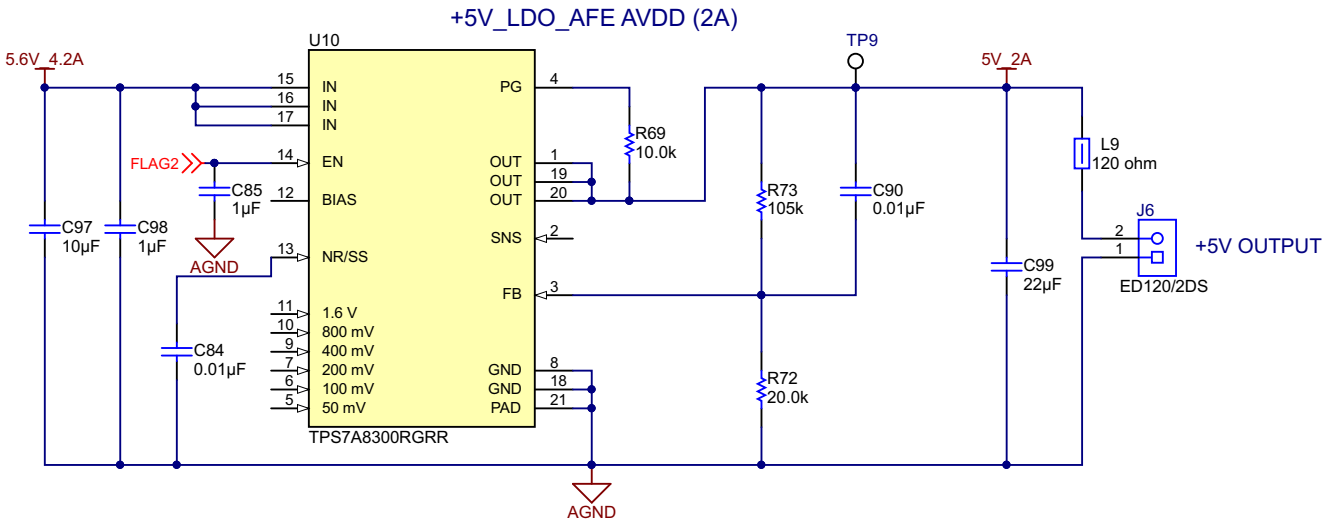


图 8. 5-V Generation Using TPS7A83

See the TPS7A83 datasheet (SBVS197) and TPS7A83 EVM (SLVU919) for detailed design instructions and recommendations. See the Texas Instruments WEBENCH Design Center for generating solution using this part.

2.3.6 Power Sequencer and 3.3-V Generation for Power Sequencer

图 9 shows the power sequencing circuit for the power supplies of this reference design using the LM3881.

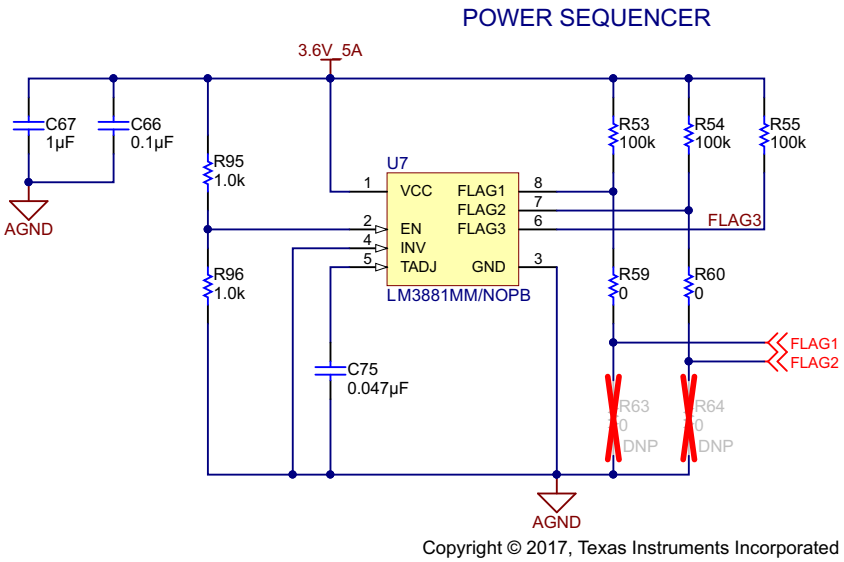
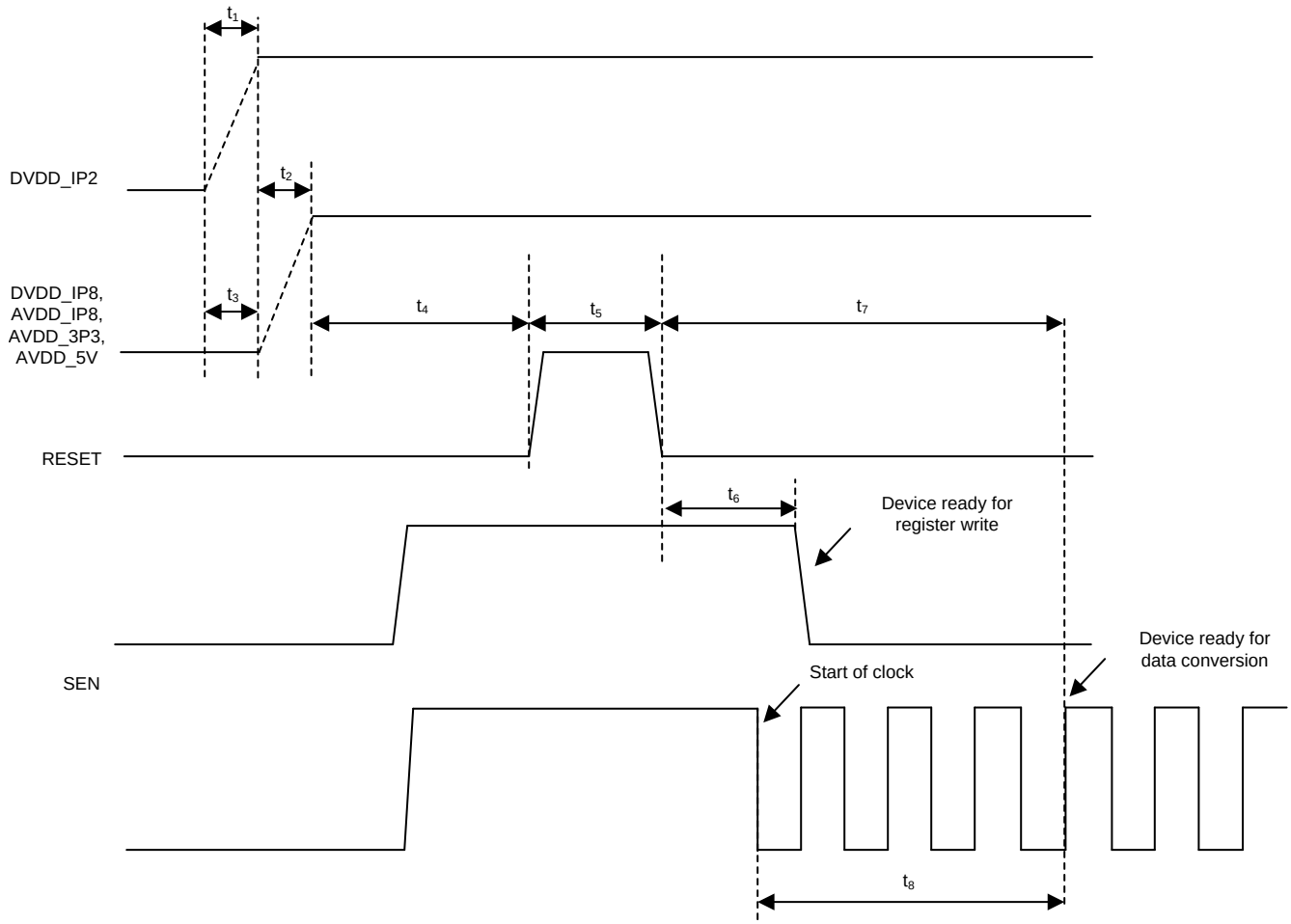


图 9. Power Sequencing Circuit

The requirements for power sequencing the AFE5818 is as shown in 图 10:

- The DVDD_1.2V supply must rise before the AVDD_1.8V supply.
- If the AVDD_1.8V supply rises before the DVDD_1.2V supply, the AVDD_1.8V supply current is 8 to 12 times larger than the normal current until the DVDD_1.2V supply reaches a 1.2-V level.



Note: 10 µs < t_1 < 50 ms, 10 µs < t_2 < 50 ms, t_3 > t_1, t_4 > 10 ms, t_5 > 100 ns, t_6 > 100 ns, t_7 > 4 ADC clock cycles, and t_8 > 100 µs

图 10. Power Sequencing of AFE5818

In this reference design, the delay between 1.2 V and all other rails (1.8 AVDD, 1.8 DVDD, 5 AVDD, 3.3 AVDD) is set as 50 ms by choosing the Tadj capacitor (C75) as 47 nF. The LM3881 is powered using a 3.6-V TPS7A84 LDO. Keep the delay sufficiently large such that the tolerances of the capacitors do not make the second voltage override the first due to the soft start. See the LM3881 datasheet (SNVS555) and LM3881 EVM (SNVA322) for design details. See the Texas Instruments WEBENCH Design Center for generating solution using this part.

2.3.7 Clock Buffer and 3.3-V Generation

图 11 shows the clock signal fan out buffer using the CDCLVC1106, a 1:6, 3.3-V LVCMOS, high-performance, low-skew, general purpose clock buffer that supports frequencies up to 180 MHz. In an ultrasound system, the switching frequencies are in the range of 100 to 500 kHz, hence the CDCLVC1106 is selected for this reference design. It is recommended to place 15-Ω series resistors close to the driver to minimize signal reflection.

See the CDCLVC1106 datasheet (SCAS895) and CDCLVC1106 EVM (SCAU041) for detailed information.

图 12 shows the circuit to generate the 3.3-V supply for the CDCLVC1106 using the LDO TLV70433.

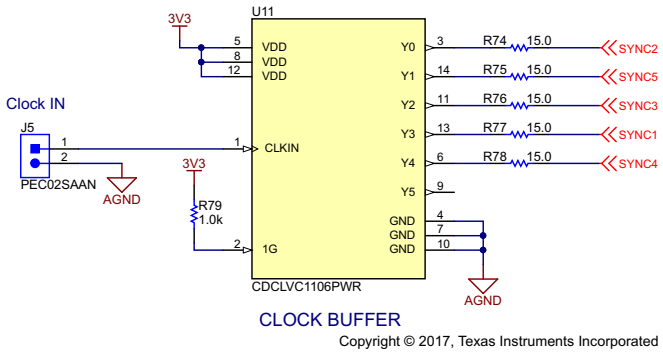


图 11. Clock Signal Fan Out Buffer

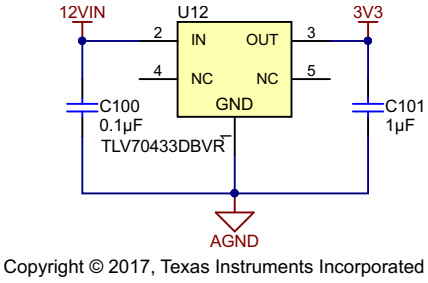


图 12. 3.3-V Generation

See the TLV70433 datasheet (SBVS148) for more details.

2.3.8 eFUSE

图 13 shows the eFuse circuit for this reference design using the TPS259260, a 12-V eFuse protection switch.

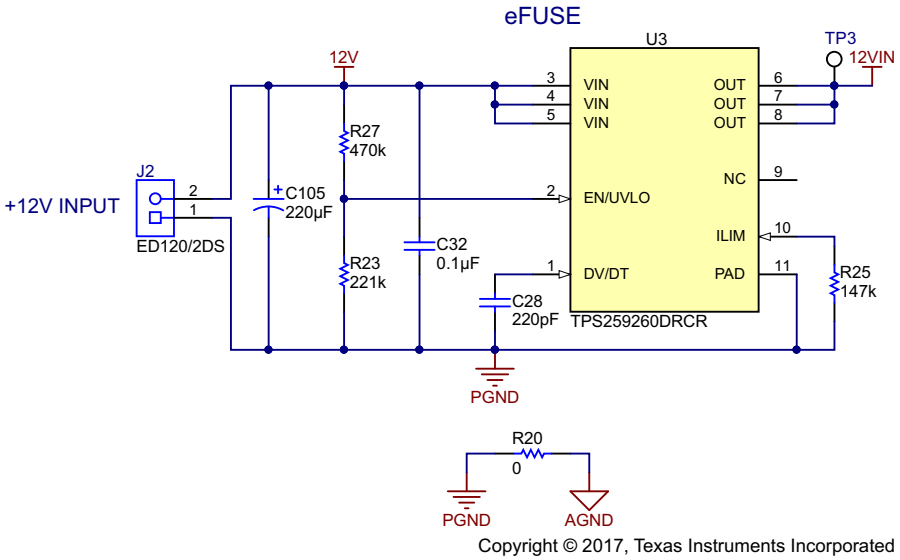


图 13. eFUSE Circuit for TIDA-01466

2.3.8.1 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set to I_{OL} (overload current limit). ILIM can be calculated using 公式 15:

$$I_{OL} = 0.7 + 3 \times 10^{-5} (RILIM) \quad (15)$$

Where:

- R_{ILIM} = 147 kΩ

Substituting R_{ILIM} in 公式 15 gives I_{OL} = 4.2 A.

2.3.8.2 UVLO Set Point

The UVLO trip point is adjusted using the external voltage divider network of R27 and R23 as connected between IN, EN/UVLO, and GND pins of the device. UVLO can be calculated using 公式 16:

$$V_{UR} = \frac{R27 + R23}{R23} \times V_{ENR} \quad (16)$$

Where:

- V_{ENR} = 1.4 V
- R27 = 470 kΩ
- R23 = 221 kΩ

Substituting V_{ENR}, R27, and R23 in 公式 16 gives V_{UR} = 4.37 V.

2.3.8.3 Setting Output Voltage Ramp Time ($T_{dV/dT}$)

The total ramp time ($T_{dV/dT}$) for 0 to V_{IN} can be calculated using 公式 17:

$$T_{dV/dT} = 10^{16} \times V_{IN} \times (C_{dV/dT} + 70\ pF) \quad (17)$$

Where:

- V_{IN} = 12 V
- $C_{dV/dT}$ = C28 = 220 pF

Substituting V_{IN}, $C_{dV/dT}$ in 公式 17 gives $T_{dV/dT}$ = 3.26 ms.

2.3.8.4 Inrush Current (I_{INRUSH}) Setting

Inrush current can be set using 公式 18:

$$I_{INRUSH} = \frac{C_{OUT} \times V_{IN}}{T_{dV/dT}} \quad (18)$$

Where:

- C_{OUT} = 100 µF (total output capacitance)
- V_{IN} = 12 V
- $T_{dV/dT}$ = 3.26 ms

Substituting C_{OUT}, V_{IN}, and $T_{dV/dT}$ in 公式 18 gives I_{INRUSH} = 0.37 A. See the TPS259260 datasheet (SLVSCQ3) and design calculator for more details.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

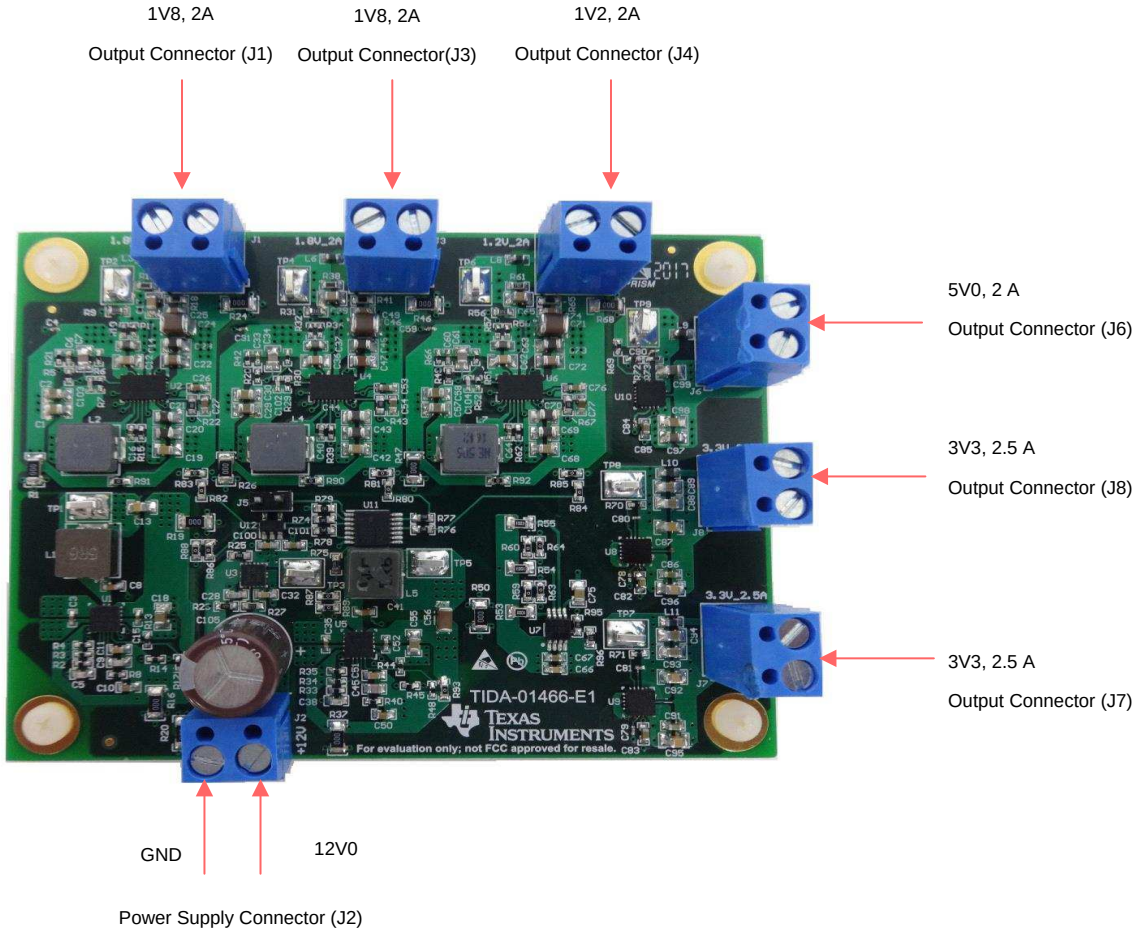


图 **14. TIDA-01466 PCB Connectors**

表 **4. TIDA-01466 Connector Description**

SIGNAL	CONNECTOR	FUNCTION
+12V Input	J2	This pin is used to connect the input power supply. Set power supply to 12 V with a 5-A current limit.
Clock IN	J5	Clock IN for sync mode operation
+1.8V_1 Output	J1	1.8-V_1, 2-A output connector
+1.8V_2 Output	J3	1.8-V_2, 2-A output connector
+1.2V_2 Output	J4	1.2-V, 2-A output connector
+3.3V_1 Output	J8	3.3-V_1, 2.5-A output connector
+3.3V_2 Output	J7	3.3-V_2, 2.5-A output connector
+5V Output	J6	5-V, 2-A output connector

3.2 Testing and Results

3.2.1 Test Setup

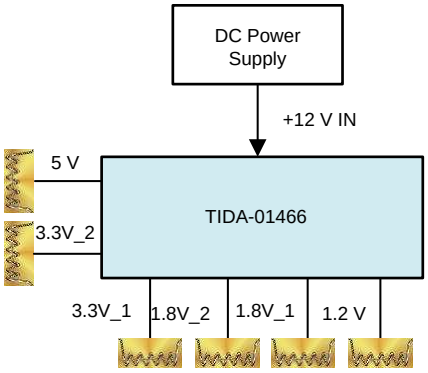


图 **15. TIDA-01466 Test Setup**

图 15 shows the test setup of the reference design for load test and ripple measurement. The following tests are conducted to evaluate the reference design using this test setup.

3.2.1.1 Load Regulation

In this test, heater filaments are used as load resistors for each output, and output voltages are observed under no load and full load conditions. Load regulation is calculated as per 公式 19, and 表 5 shows the value of the resistors used for each voltage output. See 节 3.2.2 for test results.

$$\text{Load regulation}\,(\%) = \frac{(V_{NL} - V_{FL})}{V_{FL}} \times 100 \tag{19}$$

表 **5. Load Resistors**

OUTPUT VOLTAGES	LOADS (Ω)
5 V	2.50
3.3 V_1	1.32
3.3 V_2	1.32
1.8 V_1	0.90
1.8 V_2	0.90
1.2 V	0.60

3.2.1.2 Output Ripple Measurement

图 16 shows the test setup used to measure the output voltage ripple. Measurements are taken using PXA Signal Analyzer N9030B 3 Hz to 44 GHz in dBm. See 节 3.2.2 for the test results.

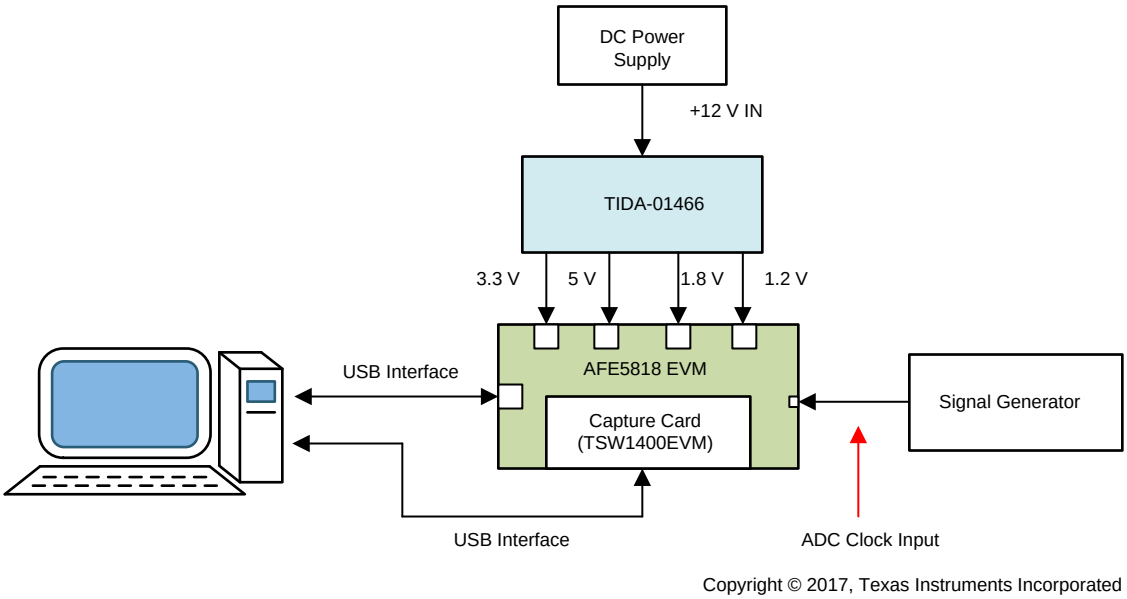


图 16. TIDA-01466 Test Setup For Test With AFE Integrated

图 16 shows the test setup to evaluate the performance of TI AFE AFE5818 EVM using this reference design. Following test was conducted to evaluate the performance.

3.2.1.3 Test With AFE Integrated

This test evaluates the performance of AFE5818 EVM using this reference design. The test is conducted by disconnecting the onboard EVM power supplies (linear regulators) and by connecting the reference design supplies. Tests are carried out in both TGC and CW mode. In TGC mode, the test is conducted to mimic the beam forming feature of the AFE5818 in the system by coherently summing the outputs of all the 16 channels. These results are averaged and FFT is taken to evaluate the correlated noise. There is no difference observed in the test results between the onboard AFE5818 EVM power supply and the reference design. In this test, 60M clock is used for the AFE ADC provided by the signal generator SG382 and the coherently sampled results are taken. In this test, AFE5818 EVM is controlled using HMC-DAQ GUI. The TSW1400 EVM is also required for capturing data from the AFE5818 EVM and its analysis using the graphical user interface (GUI), called High Speed Data Converter Pro (HSDCPro). The USB connections from the AFE5818 EVM and TSW EVM to the PC are used for communication from the GUIs to the boards. The TSW1400EVM is a complete pattern generator and data capture circuit board used to evaluate most of Texas Instruments' high speed ADCs and DACs. The TSW1400EVM features a high-speed LVDS bus capable of providing 16 bits of data at 1.5 GSPS. The board comes with 1GB of memory, which provides a 16-bit sample depth of 512 MB. This improved memory enables better FFT frequency resolution and larger capture sizes for more realistic tests. HSDC PRO GUI is an easy-to-use GUI that allows users to conduct time domain tests, single- or multiple-tone frequency tests, and even load their own test patterns. See the AFE5818 EVM and TSW1400 EVM for more details.

In CW Mode, summing amplifier output was measured using the signal analyzer PXA Signal Analyzer N9030B 3 Hz to 44 GHz. This test is carried out with an input signal of 15 kHz, 4 dBm. See 节 3.2.2 for test results.

3.2.2 Test Results

3.2.2.1 LDO Output Voltage Spectrum: 1.8 V, 1.2 V, 3.3 V, and 5 V

图 17 shows the output voltage noise spectrum for the TPS54122 with LDO V_{OUT} = 1.8 V, SW OUT = 2.3 V, V_{IN} = 5.6 V. The max peak is –50.23 dBm at 480 kHz with a 2-A load.

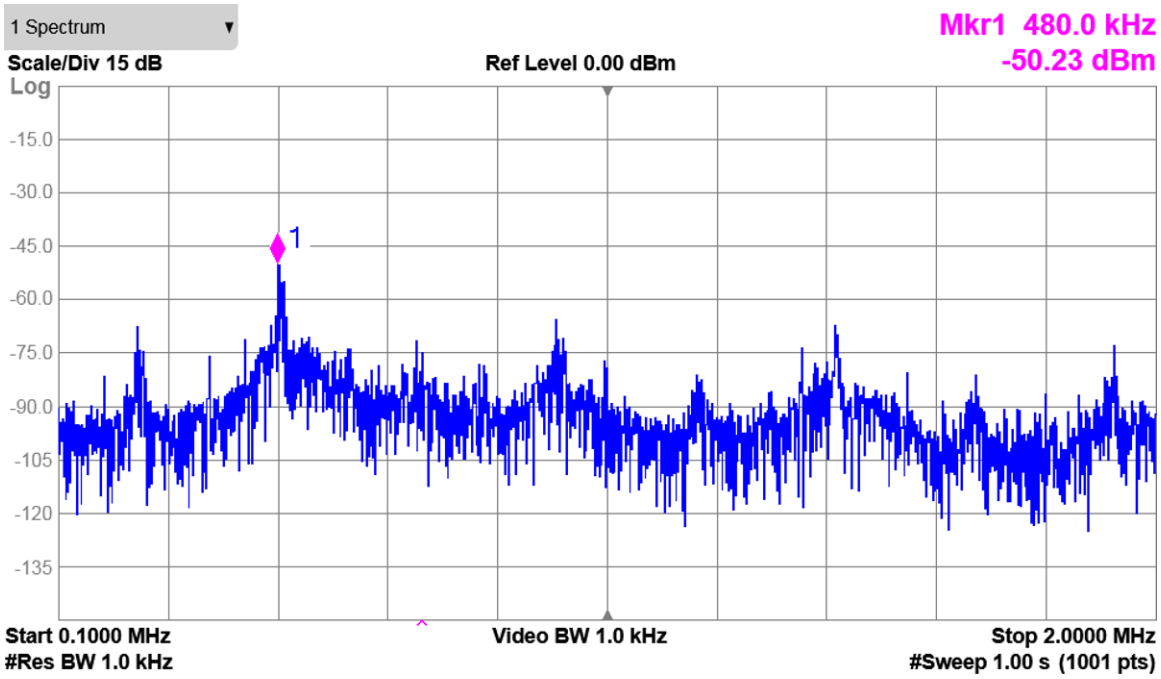


图 17. Output Voltage Spectrum of TPS54122 With LDO V_{OUT} = 1.8 V, 2-A Load, –50.23 dBm Max Peak at 476 kHz

图 18 shows the output voltage noise spectrum for the TPS54122 with LDO V_{OUT} = 1.2 V, SW OUT = 1.7 V, V_{IN} = 5.6 V. The max peak is –60.47 dBm at 476 kHz with a 2-A load.

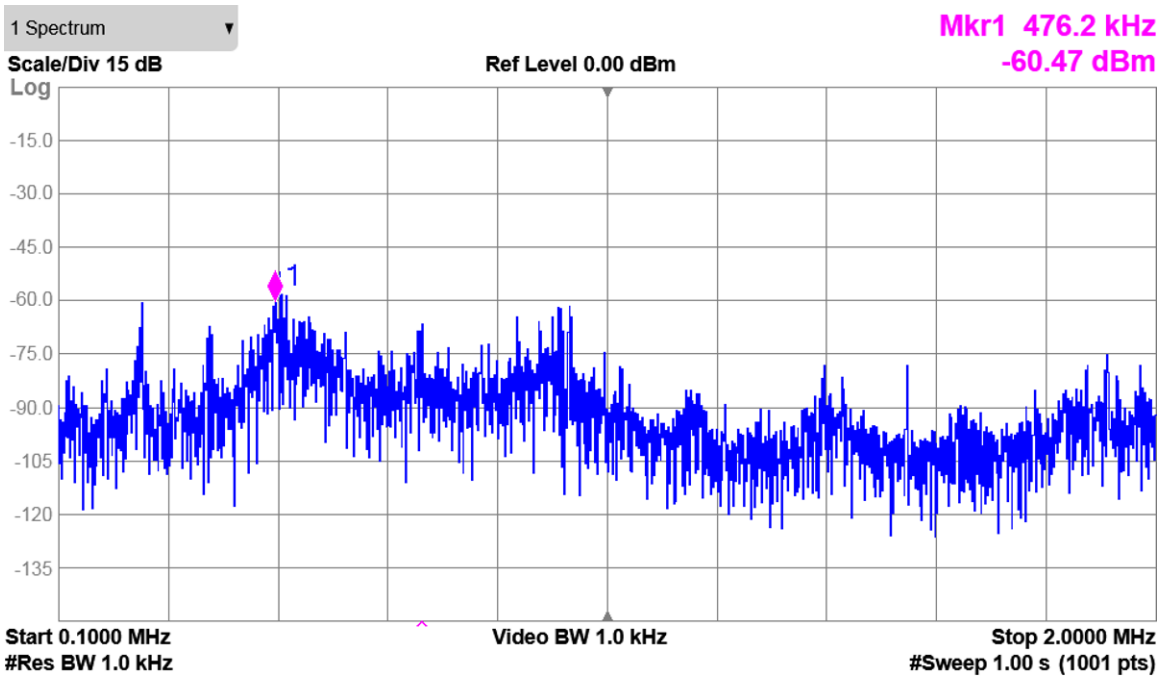


图 18. Output Voltage Spectrum of TPS54122 With LDO V_{OUT} = 1.2 V, 2-A Load, –60 dBm Max Peak at 476 kHz

图 19 shows the output voltage noise spectrum for the TPS7A84 with LDO OUT = 3.3 V, VIN = 3.6 V. The max peak is –73.23 dBm at 524 kHz with a 2.5-A load.

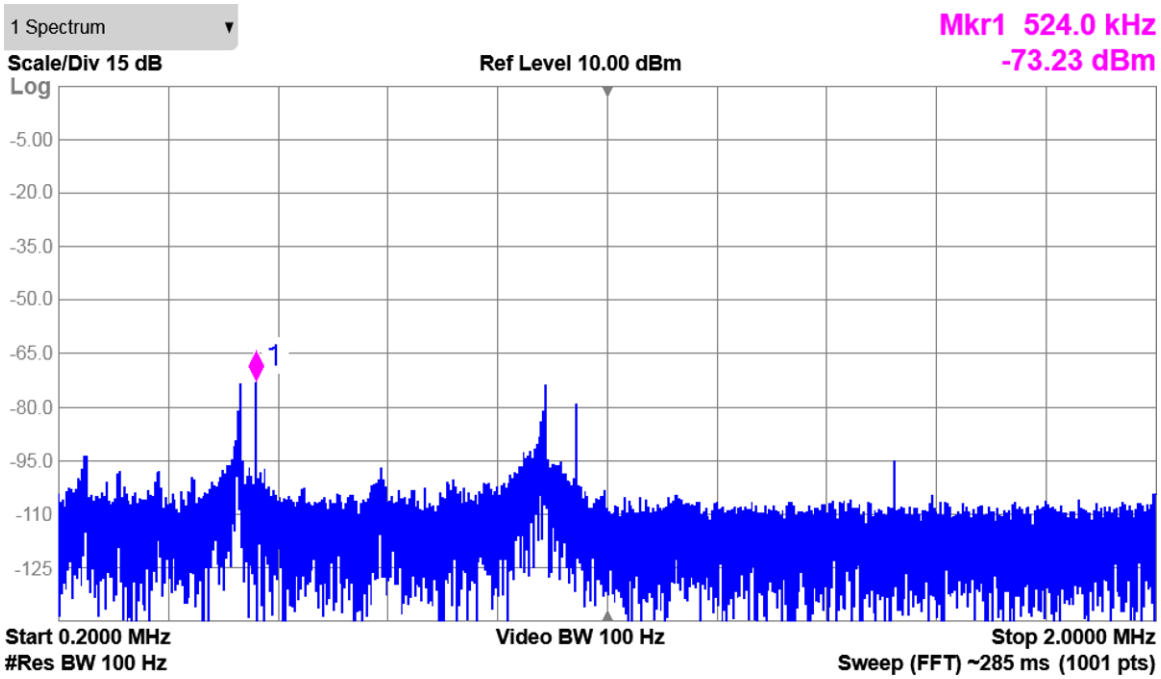


图 19. Output Voltage Spectrum of TPS7A84 With LDO V_{OUT} = 3.3 V, 2.5-A Load, –73.23 dBm Max Peak at 524 kHz

图 20 shows the output voltage noise spectrum for the TPS7A83 with LDO V_{OUT} = 5 V, V_{IN} = 5.6 V. The max peak is –60 dBm at 524 kHz with a 2-A load.

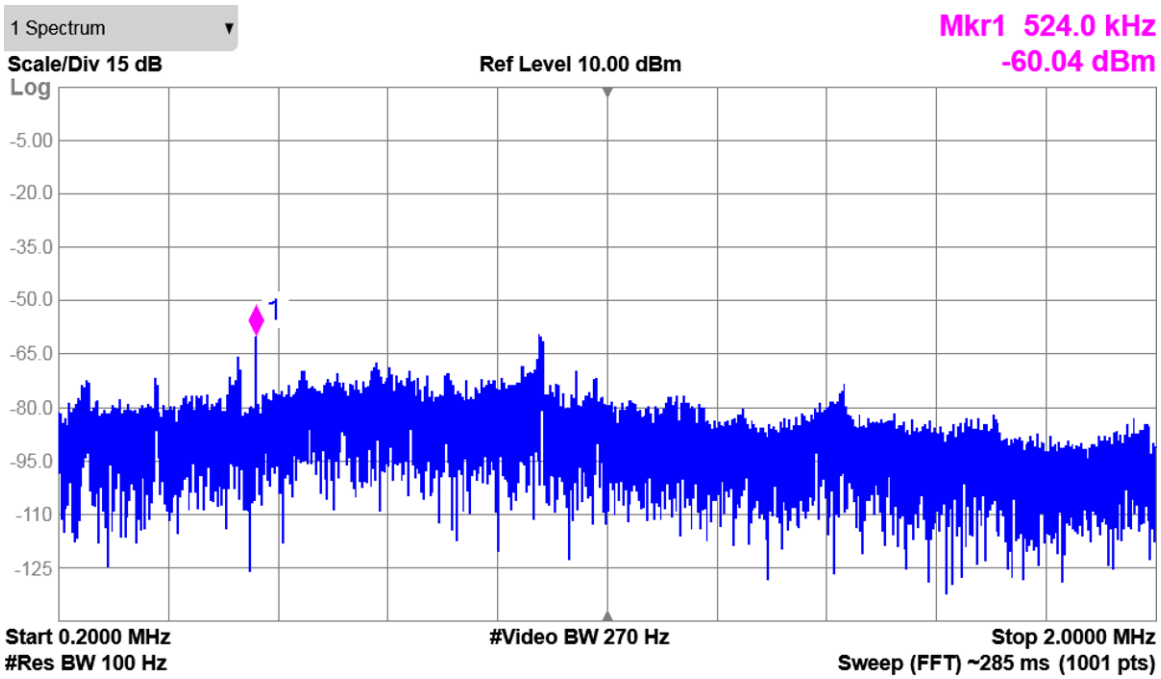


图 20. Output Voltage Spectrum of TPS7A83 With LDO V_{OUT} = 5 V, 2-A Load, –60 dBm Max Peak at 524 kHz

3.2.2.2 Load Regulation

表 6 shows the load regulation of this reference design.

表 6. Load Regulation of TIDA-01466 Power Supplies

OUTPUT VOLTAGES	NO LOAD VOLTAGES (V)	FULL LOAD VOLTAGES (V)	LOAD REGULATION
1.8 V_1	1.811	1.797	0.780%
1.8 V_2	1.811	1.798	0.723%
1.2 V	1.228	1.217	0.900%
5 V	4.972	4.970	0.040%
3.3 V_1	3.297	3.294	0.091%
3.3 V_2	3.301	3.299	0.060%

3.2.2.3 Test Results With AFE5818 Integrated (For TGC and CW Mode)

3.2.2.3.1 In TGC Mode

图 21 shows the AFE5818 EVM test result for TGC Mode with total gain of 42, and the calculated SNR is 70.12. With the AFE5818 EVM onboard power supply, SNR is 70.95. Gain settings of the TGC Mode are as shown in 表 7.

表 7. TGC Mode Gain Settings

LNA	ATTN	PGA	TOTAL GAIN
18	0	24	42

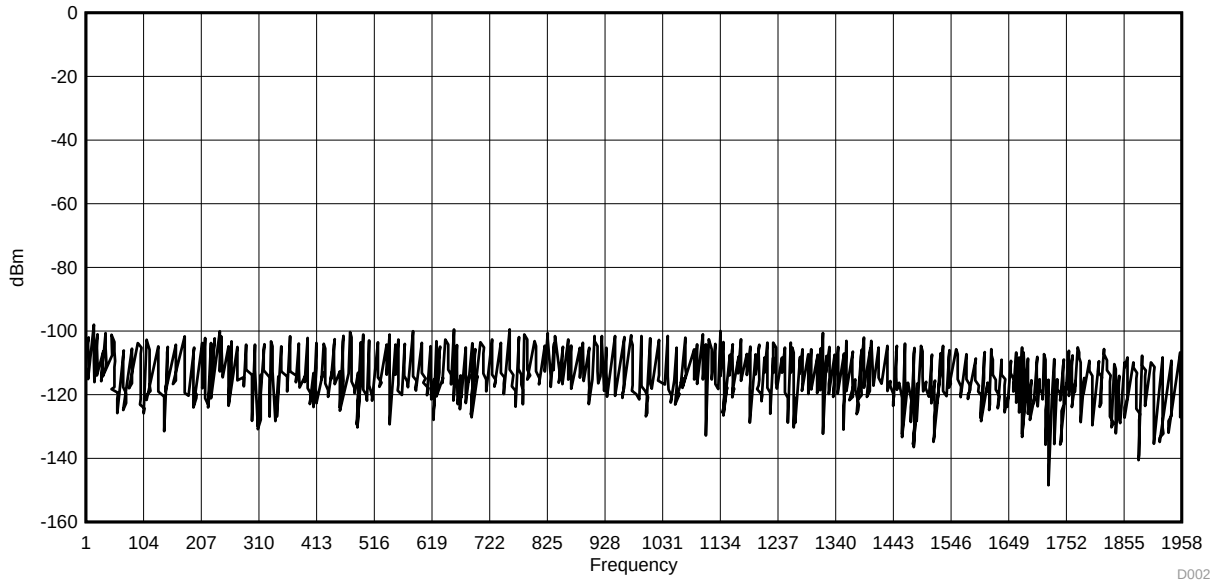


图 21. AFE TGC Path Result With Total Gain of 42, SNR = 70.12

3.2.2.3.2 In CW Mode

图 22 shows the CW summing amplifier output measured using signal analyzer. The input signal used for this test is a 15-kHz, –4-dBm sine wave. First and second harmonic are –96.7 dBm and –77.8 dBm, respectively.

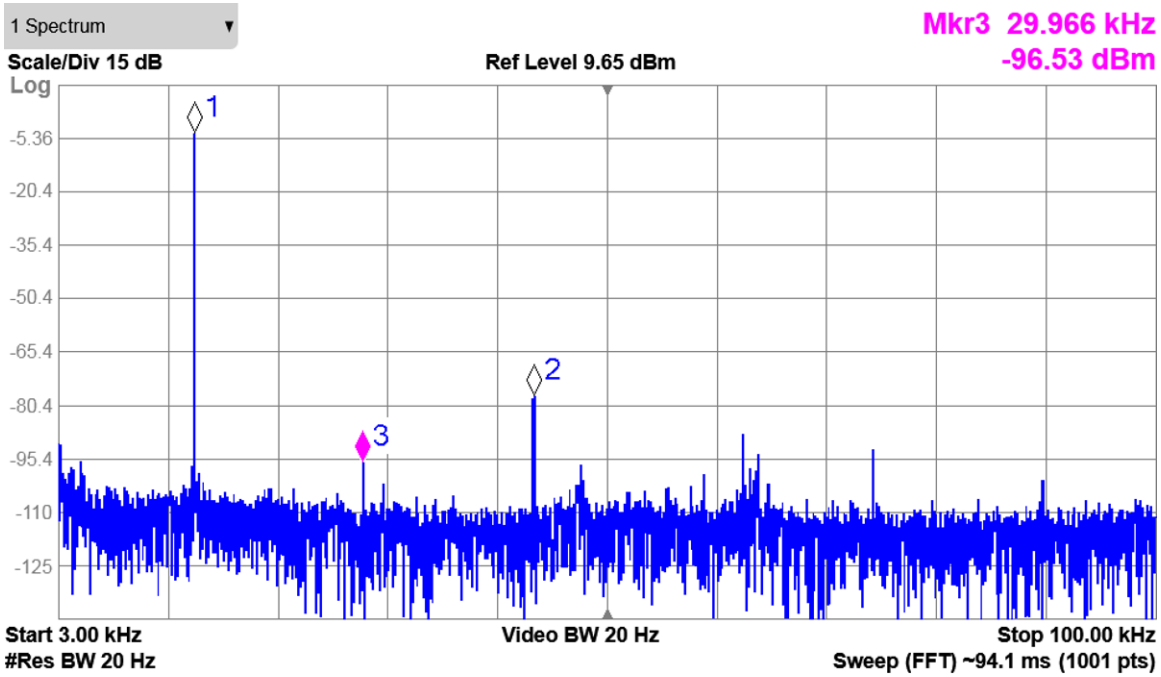


图 22. AFE5818 CW Summer Output With TIDA-01466 Integrated; First Harmonic = –96.7 dBm, Second Harmonic = –77.8 dBm

3.2.2.4 Power Sequencing

图 23 shows the power sequencing of this reference design with regards to 1.2 V and 1.8 V. All other output voltages appear at the same instant as 1.8 V .There is a 50-ms delay between 1.2 V and all other voltage rails.

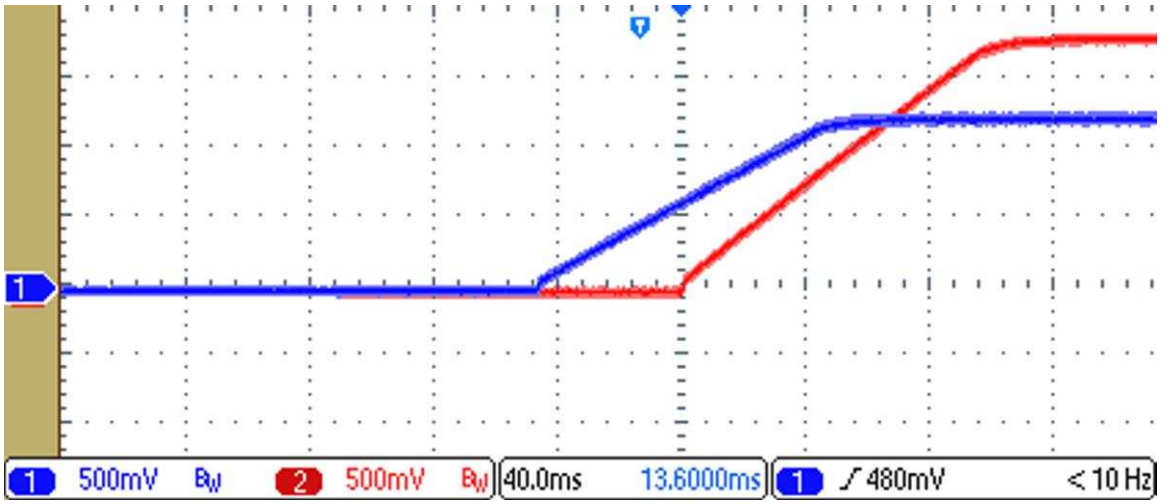


图 23. Delay Between 1.2 V and 1.8 V is 50 ms, Soft Start is 100 ms

3.2.2.5 Thermal Shot

图 24 shows the thermal shot of this reference design under full load condition. The maximum temperature measured is 76.5°C.

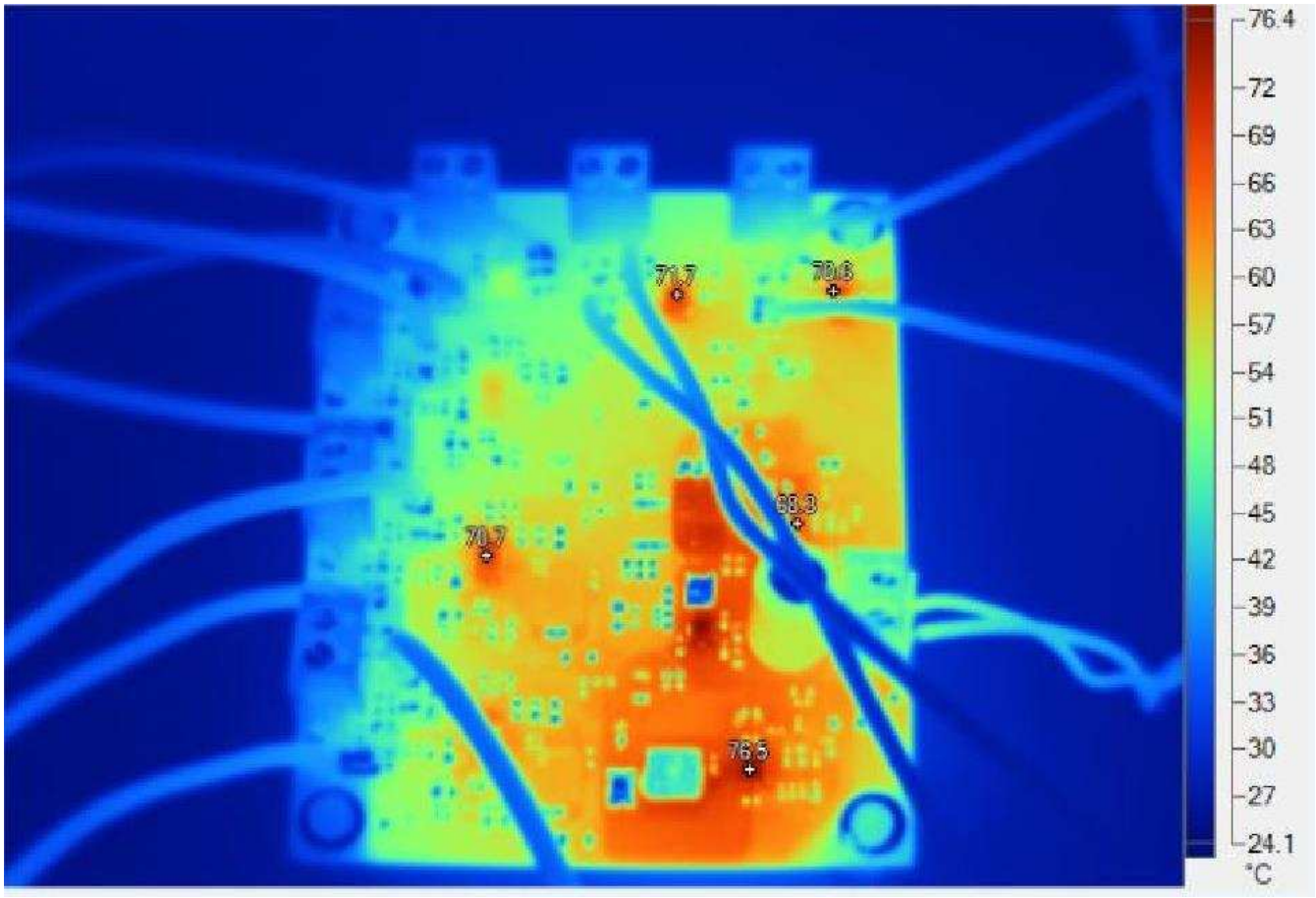


图 **24. TIDA-01466 Thermal Shot**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01466.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01466.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01466.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01466.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01466.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01466.

5 Software Files

To download the software files, see the design files at TIDA-01466.

6 Related Documentation

1. Texas Instruments, *AFE5818 16-Channel Analog Front End Evaluation Module (EVM Rev. C)*, User's Guide (SLOU430)
2. Texas Instruments, www.ti.com/tool/TSW1400EVM

6.1 商标

7 About the Author

LENI SKARIAH is a systems engineer at Texas Instruments, where she is responsible for developing subsystem design solutions for the Medical, Healthcare and Fitness sector. Leni brings her experience in precision analog and mixed signal designs to this role. Leni earned her bachelor of technology in electronics and communication engineering from the University of Kannur and her master of technology in digital electronics and communication systems from Visvesvaraya Technological University, Karnataka.

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