TI Designs：TIDA-01401
用于绝对编码器的高 EMC 抗扰度 RS-485 接口 参考设计

说明

该高 EMC 抗扰度参考设计展示了用于驱动器和编码器（如 EnDat 2.2、 BiSS®、 Tamagawa™等）的 RS-485 收发器。EMC 抗扰度（尤其对是逆变器开关噪声抗扰度）对于工业驱动器中的位置编码器反馈系统而言非常重要。该设计支持 5 至 15V（标称值为 12V）宽输入电压范围（用作到编码器的输出电压），满足编码器的宽电源范围要求。该设计的电源根据所选编码器的电压范围提供了过压和短路保护，以防电缆短路期间造成损坏。采用 BoosterPack™插件模块外形，具有与 TI LaunchPad™开发套件兼容的连接器，可轻松评估 EnDat、BiSS 和其他系统（使用 C2000™MCU）。该参考设计已针对 EnDat 2.2 编码器进行测试，适用的电缆长度最大为 100m。

资源

TIDA-01401	设计文件夹
THVD1550	产品文件夹
SN74LVC2T45	产品文件夹
TPS62162	产品文件夹
TPS61240	产品文件夹
TPS22810	产品文件夹
LAUNCHXL-F28379D	工具文件夹

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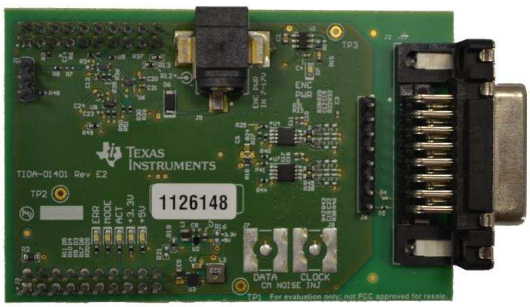
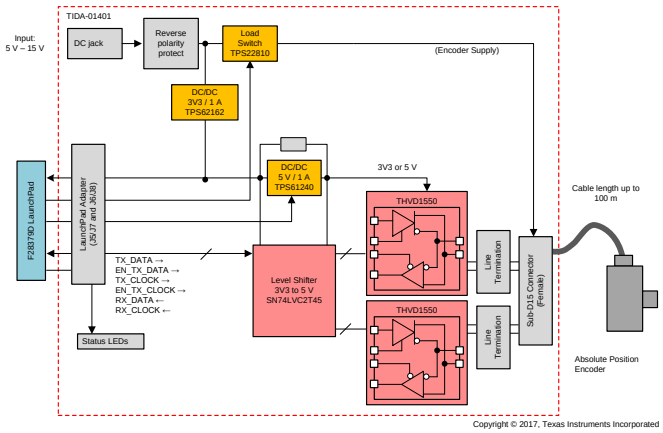


特性

- 带 16kV IEC-ESD 和 4kV EFT 的 50 兆波特 5V 半双工 RS-485 收发器 (THVD1550) 可省去外部 ESD 组件的成本。
- 设计实现了业界最高的 IEC 61000-4-4 快速电气瞬变抗扰度
- 支持 4 线制 RS-485 接口标准（如 EnDat 2.2 和 BiSS）或 2 线制接口标准（如 Tamagawa）
- 由于可配置时钟方向，硬件可用作驱动器和编码器接口
- 3.3V C2000 LaunchPad 接口，用于使用编码器协议轻松进行系统评估
- 设计符合 IEC 61800-3 EMC 抗扰度要求

应用

- 伺服 CNC 和机器人
- 交流逆变器和 VF 驱动器
- 位置传感器（编码器）
- 工业机器人



1 System Description

Absolute digital encoders are used to get absolute position or rotary angle and feedback typically in industrial drives like servo drives, CNC, and robotics EE.

There are multiple protocol standards based on RS-485 or RS-422 with synchronous or asynchronous communication and protocol specific encoder supply voltage range. Drive customers are looking for a universal RS-485 digital interface to enable their drive to support the absolute encoder that fits best to the system.

The trend is for more precise and robust control of motors, additional safety features, and predictive maintenance for lesser or complete avoidance of shutdown time.

Robustness against harsh industrial environment yield higher reliability and less down time:

- In real drives, the most critical noise is PWM switching noise coupled into the shield of the power cable during the high-voltage PWM switching transients. These transients can be 10 kV/µs with IGBT and up to 50 to 100 kV/µs with SiC in the future. These transients can couple typically as AC common-mode transients into the RS-485 differential signals. EFT and INS common-mode noise are closest to real impulse noise in drives.
- Corrupt communication (bit errors)—despite detected with CRC error—makes the current position or angle read data invalid and impacts the drives performance. In the worst case, the drive needs to shut down due to a lack of angle correct information.

It is expected that much more attention from the EMEA/U.S. drive and encoder customers is given to RS-485 immunity against ESD, surge, and especially EFT and INS. The trend to faster switching GaN and especially SiC with higher impulse noise than modern IGBT will further increase importance of RS-485 transceiver with high EMC (EFT) immunity.

图 1 shows a simplified system block of a hardware interface module supporting digital absolute position encoders. The design is shown as a subsystem of an industrial servo drive connected to the absolute position encoder. Here, the RS-485 transceiver is needed in both the encoder and the drive.

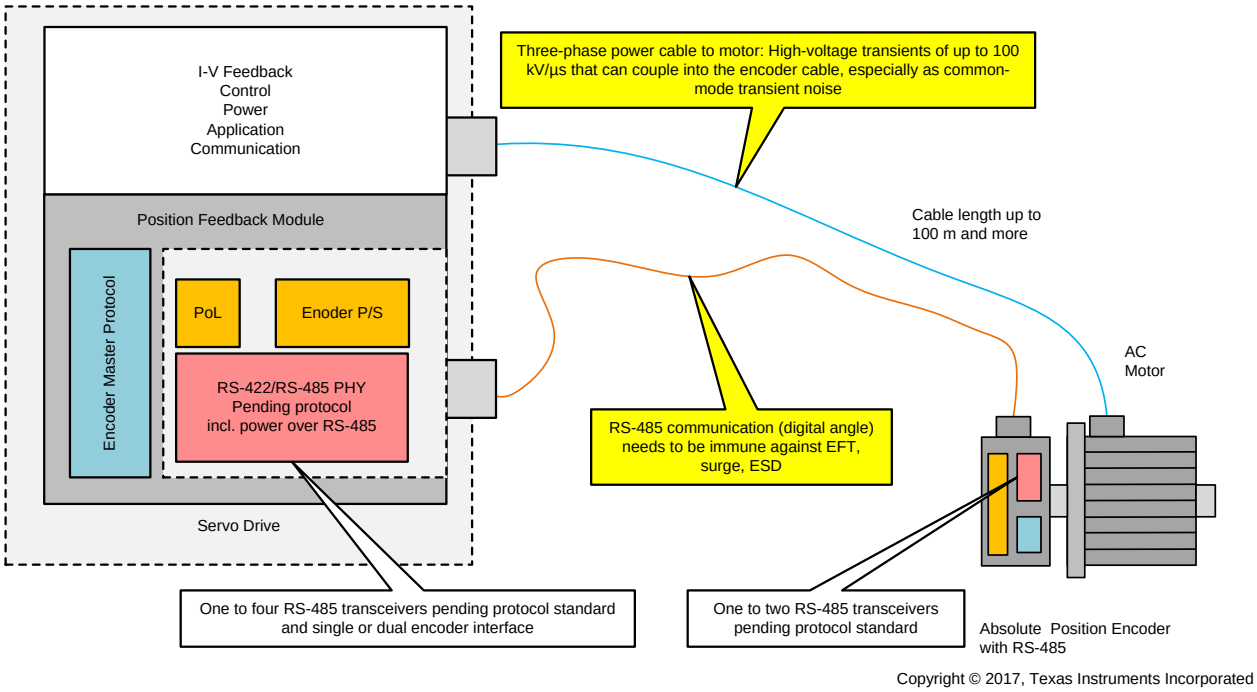


图 1. Industrial Drive With Digital Interface to Absolute Position BiSS or EnDat 2.2 Encoders

1.1 IEC61800-3 EMC Immunity Standard

When building an industrial drive, the designer must pass the compliance test of the IEC 61800-3 EMC standards. For more details on the IEC 61800-3 standard, see the TI Training material *Why EMI/EMC and isolation standards for Motor Drives*. This blog shows that several interfaces need to be tested.

Only the power port and the signal interface are tested for this design, which focuses on EFT immunity as a key concern when designing industrial drives.

表 1. IEC 618000-3 EMC EFT Immunity Requirements for Second Environment and Measured Voltage Levels and Class

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Ports for control lines and DC auxiliary supplies < 60 V	Fast transient burst (EFT)	IEC 61000-4-4	±2 kV/5 kHz, capacitive clamp	B
Power port	Fast transient burst (EFT)	IEC 61000-4-4	±2 kV/5 kHz, directly connected	B

The performance (acceptance) criterion is defined, as follows:

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module must continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after manual restart, or power off, or power on.

Depending on where in the world the drive is EMC tested there are other IEC standards for Electrical Fast transients.

For example Japan specifics an additional standard the NECA TR-28 for impulse noise(INS), this design was tested against IEC 61000-4-4.

1.2 Key System Specifications

表 2. TIDA-01401 System Specifications

PARAMETER	VALUE	COMMENT
DC input voltage	5 to 15 V	2.1-mm ID/5.5-mm ODM barrel DC jack; 12-V input to supply the board
RS-485 interface	2-channel half-duplex 5-V RS-485 transceiver	Can be configured for use in both Encoder and drive interface
Encoder power supply	DC input voltage	Same as DC input voltage, can be turned controlled using a load switch using I/O interface
Encoder data transfer to drives system	16 kHz or 32 kHz	One data transfer per PWM frequency of motor drive
I/O interface signaling voltage	3.3 V	BoosterPack for Launchxl-F28379D; for pin assignment, see 表 8
RS-485 transceiver power supply	3.3 V or 5 V	Flexible power supply for 3.3-V or 5-V versions of RS-485 transceivers
RS-485 transfer rate	50 MBaud	Supports all standard encoder protocols; 50 MBaud improves rate reach
Temperature range	–40°C to 85°C	Industrial temperature range of –40°C to 85°C; no heat sink required.
Electromagnetic compatibility (EMC)	According to IEC 61800-3	Designed to meet or exceed IEC 61800-3 EMC levels and pass criterion for ESD, EFT, and surge according to test method described in: • IEC 61000-4-2 • IEC 61000-4-4 • IEC 61000-4-5
Encoder connector	Sub D-15 or 10 pin header	Compatible to Heidenhain Sub D-15 adapter ID 524599-xx
Encoder standard	EnDat 2.2, BiSS, Tamagawa	Pending software from C2000
Indicator LEDs	Power rails and three I/O controlled	3.3-V, 5-V, and Encoder PS and LaunchPad LEDs for test and debug options

2 System Overview

This reference design implements an industrial temperature and EMC-compliant universal digital interface to absolute position encoder protocols like EnDat 2.2, BiSS, or Tamagawa.

The major building blocks of this reference design's hardware are: the 4-wire bidirectional RS-485 the encoder power supply and a 3.3-V digital interface to a host processor to run the corresponding encoder standard protocol. The host processor to run the corresponding encoder master protocol is not part of this design. The main features of this design are:

- Hardware to interface to EnDat 2.2 and BiSS encoders, supports all corresponding standard data rates up to at least 100-m cable length
- Input voltage range from 5 to 15 V. The input is protected against reverse polarity. Onboard DC/DC to generated 3.3-V and 5-V point-of-load
- Eliminates cost for external ESD components by using 5-V supply half-duplex RS-485 transceiver THVD1550 with 16-kV IEC-ESD and 4-kV EFT
- Encoder P/S with output voltage is equal to the input voltage range (5 to 15 V), which can be disabled through a load switch, compliant to EnDat 2.2 and BiSS encoders
- Host processor interface (3.3-V I/O) to processors C2000 MCU to run the EnDat 2.2 or BiSS master
- LEDs for status indication
- Exceeds EMC immunity for EFT with levels according to IEC 61800-3

The design has been tested for EMC immunity against fast transient burst (EFT) with levels specified per IEC 61800-3 and above the standard. For details on the EFT see 节 3.2.2.4.

There are multiple absolute position encoder protocol standards that use RS-485 or RS-422 based serial digital interfaces such as EnDat 2.2, BiSS, or HIPERFACE DSL. Further interface standards include PROFIBUS® DP and PROFIBUS IO as well as CAN- or Ethernet-based interfaces. Additional standards include proprietary, drive vendor-specific standards like Tamagawa, Fanuc Serial Interface, Mitsubishi® High-Speed Serial Interface, and more.

This reference design supports the most common industrial serial interfaces such as EnDat 2.2, BiSS, and SSI. For more details on the different standards, see the following reference designs, listed per protocol, as shown in 表 3.

表 3. Absolute Position Encoder Digital Interface TI Designs

ENCODER PROTOCOL	TI DESIGN
EnDat 2.2	TIDA-00172, TIDA-00179
BiSS	TIDA-00175, TIDA-00179
HIPERFACE DSL	TIDA-00177, TIDA-00179
HIPERFACE	TIDA-00202

2.1 Block Diagram

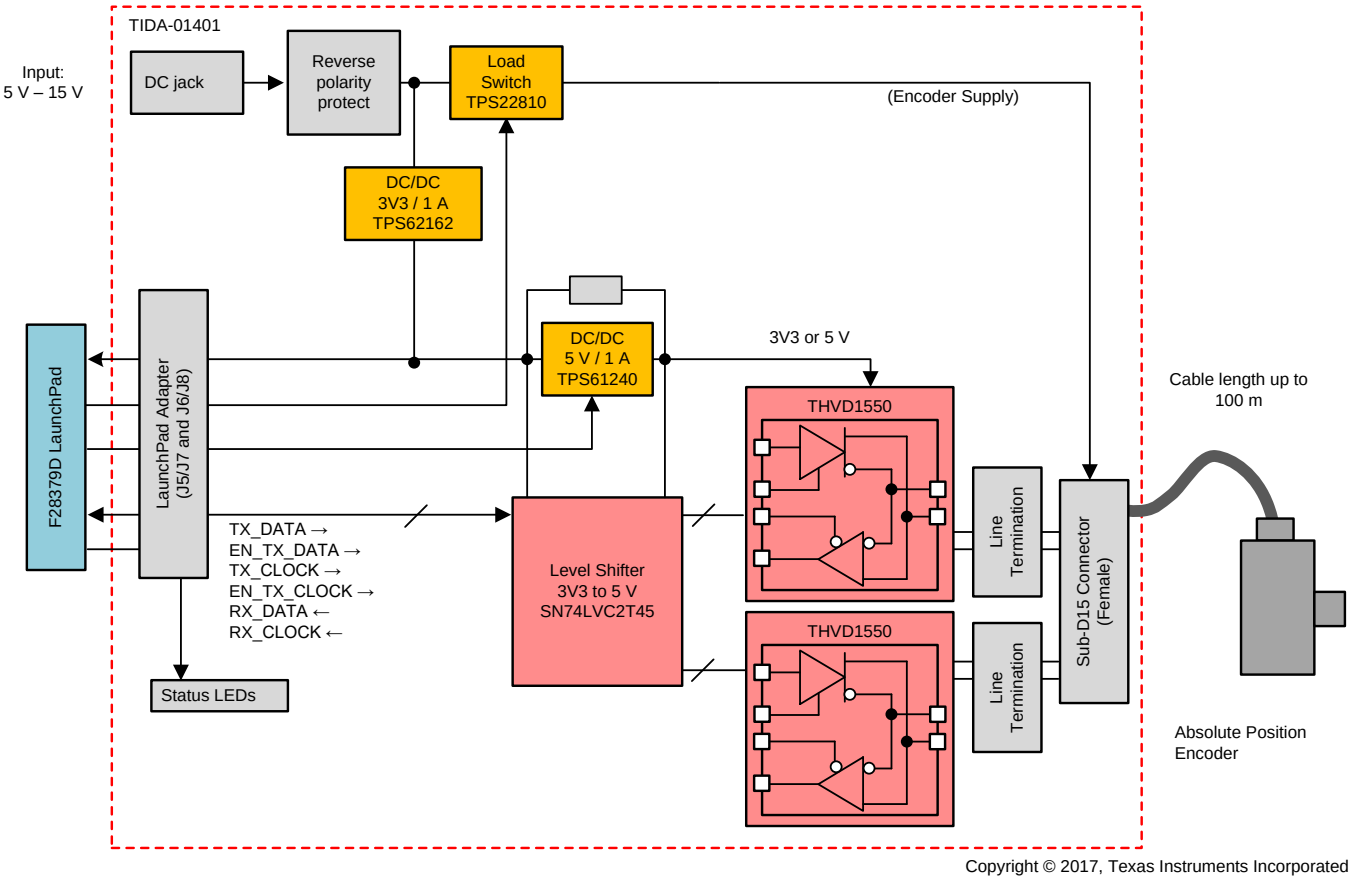


图 **2. System Block Diagram of TIDA-01401**

2.2 Design Considerations

This design has three major hardware blocks: the digital interface, the power supply for the digital interface, and the power supply for the encoder.

节 2.2.1 explains these three blocks. 节 2.2.3 provides a brief overview of the software needed to use this reference design.

2.2.1 Hardware Design

2.2.1.1 Digital Interfaces

2.2.1.1.1 Transceiver Circuits

When choosing the RS-485 device for EnDat 2.2, consider the relationship between baud rate and clock frequency. EnDat 2.2 is a synchronous communication with the data shifted out at the falling clock edge. Each clock period equals two bauds; the first half clock period equals a symbol as well as the second half period, meaning the baud rate must be at least twice the clock rate. Therefore, an EnDat 2.2 compliant RS-485 transceiver needs to be specified for a minimum baud rate of 32 Mbps.

When EnDat 2.2 is implemented without delay compensation at a maximum clock of 2 MHz, the entire loop propagation delay (master and encoder) must not exceed 250 ns. Parameters with regards to RS-485 transceivers taken into consideration are listed in 表 4.

表 4. RS-485 Parameters From Corresponding Datasheets (TBD)

PARAMETER	THVD1550
Supply voltage (recommended)	5 V
Baud rate (maximum)	50 Mbps
Receiver propagation delay (maximum)	40 ns
Driver propagation delay (maximum)	16 ns
Receiver rise and fall time (maximum)	6 ns
Driver rise and fall time (maximum)	6 ns
Supply current (quiescent) driver and receiver enabled	700 µA
IEC 61000-4-4 ESD (absolute maximum ratings)	±16 kV (CD)
IEC 61000-4-4 EFT (absolute maximum ratings)	±4 kV

Due to the high IEC 61000-4 immunity specification, the RS-485 device chosen is the THVD1550.

2.2.1.1.2 RS-485 Termination and Transient Protection

Instead of single 120-Ω/0.1-W resistors, two smaller resistors 0603 in series 0.1 W each have been chosen. A pulse-proof resistor is added to the A and B bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up. In data receive mode, due to the low input current of typical 240 µA, the voltage drop across the 10-Ω resistors is negligible. In the clock and data transmit direction, the voltage drop across both 10-Ω resistors is around 15%, which results in a slightly lower transmit differential voltage.

To further improve immunity against common-mode noise, two different circuits choice are shown in 图 3:

1. 220-pF bypass capacitors are added from each differential RS-485 outputs A and B to GND. See C19 and C22 in 图 9; these capacitors need to be high quality capacitors (NP0/C0G).
2. A 470-pF bypass capacitor is added at the center point of the termination resistors R42 and R43. This bypass capacitor removes the need to match the capacitors to have the same effect on the common mode during an event. Here, the difference of the resistor values affects the equal distribution of an event. The capacitor needs to be a high-quality capacitor (NP0/C0G).

The bus terminals of the THVD15xx transceiver family possess on-chip ESD protection against a ±30-kV human body model (HBM), ±16-kV IEC 61000-4-2 contact discharge, and ±4-kV IEC 61000-4-4 EFT, meaning no further protection is required.

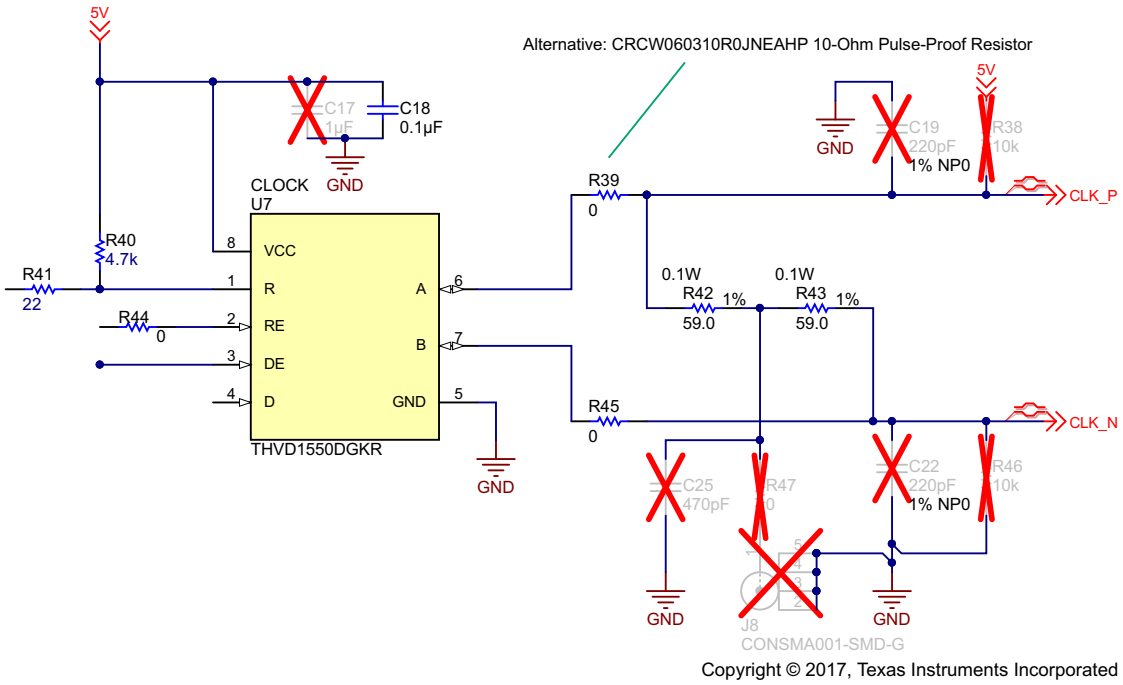


图 **3. Schematic of Clock Transceiver Circuit**

For the data transceiver circuit, the resistors mentioned are R28, R29, and R33 and the capacitors are C12, C15, and C16.

2.2.1.1.3 Common-Mode Noise Injection Circuit

In 图 3, R47, C25, and the J8 connector are defining this test circuit that can be used to test how well the RS-485 transceiver works with common-mode noise. J8 and R47 of this circuit are used for test purposes only. This circuit is only needed for test and debug and must be removed for a final design.

2.2.1.1.4 5- to 3.3-V Level Shifter

As the THVD1550 is a 5-V RS-485 transceiver, level translation between 5 V and 3.3 V is typically needed. This level shifter needs to have low propagation delay as this affects the system performance at long cable lengths. For this design, the SN74LVC2T45 is chosen. This device needs three integrated circuits (ICs), two for transmitting data and one for receiving data. VCCB is chosen as input and VCCA as output always of the level shifter. With this configuration and the voltage levels used the propagation delay is similar to what is presented in the SN74LVC2T45 datasheet.

表 **5. Maximum Propagation Delay From SN74LVC2T45 Datasheet**

VCCA	VCCB	DIRECTION	PROPAGATION DELAY (t_{PLH} / t_{PHL})
3.3 V	5 V	B to A	5.4 ns / 4.5 ns
5 V	3.3 V	B to A	3.9 ns / 3.5 ns

2.2.1.2 Power Supply for Digital Interface

The design needs two voltage rails: one 3v3 rail and one 5-V rail. This reference design has the 3v3 voltage rail done using a buck controller, and the 3v3 rail generates the 5-V rail using a boost controller. The 3v3 rail has a power requirement of around 1 A; this requirement includes the transceivers and the option of powering the LaunchPad from the 3v3 rail. The second requirement is what input voltage range to use.

As described in the TIDA-00179 design guide, the typical voltage rail of an encoder is either a 5-V rail or an 8- to 20-V rail. This range is why the input voltage of the design is chosen to be 5 to 15 V. Use caution when picking an encoder that can support the chosen input voltage of the reference design.

The TPS62162 has an input voltage range of 3 to 17 V providing a 1-A current. This device comes in a fixed output voltage or adjustable output voltage range. A fixed output voltage is chosen to minimize external components and PCB size.

Section 9.3.1 of the TPS6216x datasheet provides a schematic example of how to build a 3v3 voltage rail, which requires an input capacitor, an output capacitor, and an inductor as external components. 表 4 lists inductors already tested. For the two capacitors, X5R or X7R ceramic capacitors are recommended.

To generate the 5-V rail, a boost converter that boosts from the 3v3 rail is chosen. This is done to be able to have VIN down to 5 V without special considerations for generating the 5-V rail.

The TPS61240 has an input voltage range of 2.3 to 5.5 V, providing 600 mA of current. This device has a fixed output voltage, which minimizes external components and PCB size.

Section 10.2 of the TPS61240 datasheet provides a schematic example of how to build a 3v3 to 5-V rail, which requires an input capacitor, an output capacitor, and an inductor as external components.

Additionally for this design, a turnoff option of the 5-V rail is provided. This option is done by adding two resistors on the enable pin, one to GND, and one to VIN of the TPS61240. With this circuit, it is possible to test transceivers with both 5-V and 3.3-V_{CC} requirements.

2.2.1.3 Power Supply for Encoder

To power the encoder, use the V_{IN} voltage level to provide the encoder rail. This level needs to be remembered when connecting an encoder to the board.

To enable protection of the encoder and the board input voltage, a load switch is added to provide undervoltage lockout (UVLO) and thermal protection, which can be translated into an approximately 2-A current limit before the thermal protection shuts off the switch. This current limit depends on the package choice.

To calculate the current limit, see Equation 9 of the TPS22810 datasheet.

For an I_{INRUSH}, 200 mA is needed to supply the encoder, which means that the rise time defined on the CL pin needs to be smaller. Here, the choice of CL defines how fast the rise time needs to be.

$$dt = \frac{C_L \times d_{V_{OUT}}}{I_{INRUSH}} = \frac{2.2\,\mu F \times 9.6\ V}{200\ mA} = 106\ \mu s \quad (1)$$

With d_{Vout} being defined in Section 10.2.2.3 of the datasheet as 9.6 V.

To see what time needs to be set on CT pin, see Table 2 of the TPS22810 datasheet. A 470-pF capacitor is needed, which gives a rise time of 96 µs. With the smaller rise time, the I_{INRUSH} is 225 mA.

For this reference design, the device TPS22810 is chosen, which fits the voltage range of the TPS62162.

2.2.2 Hardware Updates

- Change direction of the level shifters so the propagation delay of the level shifters are the same. This change can be done because the level shifters are used in only one direction communication.
- Add resistors between the LaunchPad connector and level shifter to enable slave and master operation of the SPI peripheral of the C2000 microcontroller

2.2.3 Software Design

To test this design, the C2000 microcontroller is chosen due to its high-speed SPI, enabling up to a 50-MHz SPI clock and software library to enable the use of EnDat 2.2. To generate this example software, download the software package controlSUITE™. Here the position manager libraries enable many different digital and analog encoder interfaces. For more information on the Position Manager from C2000, see the C2000 product page.

For the tests of this design, two types of software are built: one to test an EnDat 2.2 interface, and one to generate eye diagrams and bit error tests.

The software provided is a demo version showing an EnDat 2.2 connection that sends the results back in Code Composer Studio™ (CCS). The EnDat 2.2 source software can be found in controlSUITE. There are two software versions: one for the IDDK and one for the LaunchPad. For questions on controlSUITE, visit the E2E™ forum: https://e2e.ti.com/support/microcontrollers/c2000/ For EnDat 2.2 documentation for C2000, see the C2000 user's guide[2].

2.3 Highlighted Products

2.3.1 THVD1550

These devices have robust drivers and receivers for demanding industrial applications. The bus pins are robust to high levels of IEC contact discharge ESD events, eliminating the need of additional system-level protection components.

Each of these devices operate from a single 5-V supply. The devices in this family feature a wide common-mode voltage range, which makes them suitable for multi-point applications over long cable runs. The THVD15xx family of devices is available in small VSSOP packages for space constrained applications. These devices are characterized from –40°C to 125°C.

Features:

- 4.5- to 5.5-V supply voltage
- Bus I/O protection
  - ± 30-kV HBM
  - ± 16-kV IEC 61000-4-2 Contact Discharge
  - ± 4-kV IEC 61000-4-4 EFT
- Extended industrial temperature range: –40°C to 125°C
- Large receiver hysteresis (80 mV) for noise rejection
- Low power consumption:
  - Low standby supply current: < 1 μA
  - I_{CC} <700-μA quiescent during operation
- Glitch-free power-up and power-down for hot plug-in capability

- Open, short, and idle bus failsafe
- 1/8 unit load options (up to 256 bus nodes)
- Small-size VSSOP packages save board space or SOIC for drop-in compatibility
- Low EMI 500-kbps to 50-Mbps data rates

2.3.2 TPS62162

The TPS6216x device family is an easy-to-use synchronous step-down DC/DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response and high output voltage accuracy by using the DCS-Control™ topology.

With its wide operating input voltage range of 3 to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. The TPS62162 supports up to a 1-A continuous output current at output voltages between 0.9 and 6 V (with 100% duty cycle mode).

Power sequencing is also possible by configuring the enable and open-drain power good pins.

In power save mode, the devices show quiescent current of about 17 µA from VIN. Power save mode, entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 µA.

The device is available in adjustable and fixed output voltage versions and is packaged in an 8-pin WSON package measuring 2.00 mm × 2.00 mm (DSG) or an 8-pin VSSOP package measuring 3.00 mm × 3.00 mm (DGK).

2.3.3 TPS22810

The TPS22810 is a single-channel load switch with a configurable rise time and an integrated quick output discharge (QOD). In addition, the device features thermal shutdown to protect the device against high junction temperature. Because of this feature, the safe operating area of the device is inherently ensured. The device contains an N-channel MOSFET that can operate over an input voltage range of 2.7 to 18 V. The SOT23-5 (DBV) package can support a maximum current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

The configurable rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. UVLO is used to turn off the device if the input voltage drops below a threshold value, ensuring that the downstream circuitry is not damaged by being supplied by a voltage lower than intended. The configurable QOD pin controls the fall time of the device to allow design flexibility for power down.

The TPS22810 is available in a leaded, SOT-23 package (DBV), which allows one to visually inspect solder joints. The device is characterized for operation over the free-air temperature range of –40°C to 105°C.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 PCB Overview

图 4 shows the top side of the TIDA-01401 PCB with the Launchxl-F28379D. The headers and default jumper settings are explained in 节 3.1.1.2.

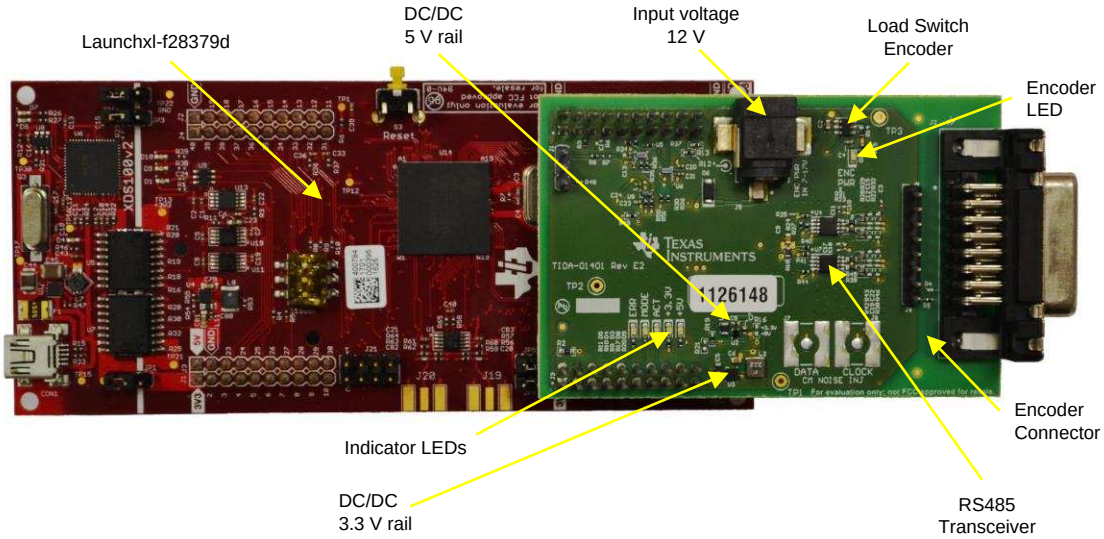


图 4. Hardware Overview

3.1.1.2 Connector and Resistor Settings

3.1.1.2.1 Connectors

The connector assignment and jumper settings are outlined in 节 3.1.1.3.2.

The 12-V nominal input voltage can be supplied through the connector J8. The chosen connector is an RAPC722X from Switchcraft®. This connector is expecting a 2.1-mm ID/5.5-mm OD mating barrel connector.

CAUTION

The input voltage of the board is directly connected to the encoder. Ensure that the encoder supports the applied voltage.

3.1.1.2.2 Default Resistor Configuration

Prior to working with the TIDA-01401 board, make sure that the correct resistor settings are applied (see 表 6). The default jumper configuration is shown on the board picture in 图 4.

表 6. Default Resistor Settings

HEADER	JUMPER SETTING
R2	Enables the 3.3-V intermediate rail connect to power the LaunchPad
R7 and R8	Configuration to use the BoosterPack as either slave or master configuration for the clock lines
R4 and R5	Configuration to remove the clock lines from the SUB-D connector; for test and debug

3.1.1.3 Design Evaluation

3.1.1.3.1 Prerequisites

The following hardware equipment and software are required to evaluate this reference design.

表 7. Prerequisites

EQUIPMENT	COMMENT
12-V DC power supply	12-V output power brick with at least 2-A output current capability. 2.1-mm ID / 5.5-mm OD mating barrel connector
TIDA-01401 hardware	With the default jumper settings per section 节 3.1.1.2.
TIDA-01401 firmware	Download from TIDA-01401 design folder
InstaSPIN-Motion F28379D LaunchPad	Available through TI Store
CCS v6	Download from TI.com
Encoder	ROQ437
Cables	ID 368 330-xx (xx for cable length)
Adapter between M8 and Sub-D 15	ID 524599-xx (xx for cable length)

3.1.1.3.2 Hardware Setup

表 8 shows the signals the TIDA-01401 BoosterPack uses to communicate with the C2000 LaunchPad.

表 8. Pinout of J3 and J4 Host Processor Interface

LAUNCHXL-F28379D				TIDA-01401 REV E2			
J5	J7	J8	J6	J3		J4	
3V3	5V	GPIO6	GND	3V3	NC	TX_CLK	GND
GPIO95	GND	GPIO7	SPIBCS/GPIO66	NC	GND	SPICLK	GND
GPIO139	ADCIN15	GPIO8	GPIO131	NC	NC	NC	NC
GPIO56	ADCINC5	GPIO9	GPIO130	NC	NC	TX_EN	NC
GPIO97	ADCINB5	GPIO10	RESETn	LED	NC	NC	NC
GPIO94	ADCINA5	GPIO11	SPIBSIMO/GPIO63	LED	NC	NC	SIMO
SPIBCLK/GPIO65	ADCINC4	GPIO14	SPIBSOMI/GPIO64	SPICLK	NC	NC	SOMI
GPIO52	ADCINB4	GPIO15	GPIO26	LED	NC	NC	NC
GPIO41	ADCINA4	DAC3	GPIO27	EN_CLK	NC	NC	Enc_Enable
GPIO40	ADCINA1	DAC4	GPIO25	NC	NC	NC	Enable 5V

3.1.2 Software

3.1.2.1 Software Setup

1. Use the controlSUITE "Position Manager" software framework for the LaunchPad "Launchxl-f28379d".
2. Pick the software library for EnDat 2.2 working on the connectors J5 to J8 of the LaunchPad.
3. Follow the example as described in controlSUITE to compile and run the code on the LaunchPad with the design connected as seen in 图 4.

For more information on the EnDat 2.2 library, see the C2000 user's guide[2].

For a user example, see the document sprui34, this document shows how to use the EnDat 2.2 software on the IDDK.

3.1.2.2 User Interface

The user interface of the standard example is the debug window of CCS.

For a user example, see the EnDat 2.2 user's guide[3]. This document shows how to use the EnDat 2.2 software on the IDDK.

To find this software, go to www.ti.com/controlSUITE.

3.2 Testing and Results

These tests characterize each individual functional block as well as the entire board. The following tests were conducted:

- Digital interface signal tests
- Power management
- System performance

The tests are done at room temperature (around 22°C) with a 16-kHz RS-485 data package repetition.

3.2.1 Test Setup

The following equipment are used to test this reference design:

表 9. Test Equipment for TIDA-01401 Performance Tests

TEST EQUIPMENT	PART NUMBER
Low-speed oscilloscope (suitable for power supply tests)	Tektronix TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Differential probes	Tektronix P6630
Single-ended probes	Tektronix P6139A
Active Probes	Tektronix P6245 TDS500/600
Power supply (12 V)	V-Infinity – 3A-181WP12 with 2.1-mm ID/5.5-mm OD mating barrel connector cable
Power supply (24 V)	Siemens LOGO!Power 6EP1331-1SH03
Power supply (24 to 10 V)	LM5010-EVAL
Power supply multi rail	EA-PS 2342-10B
True RMS multimeter	Fluke 179
General purpose PC (master)	Running CCS and Virtual com port
General purpose PC (slave)	Running CCS and Virtual com port
Encoder cables	ID 368 330-xx (xx for cable length)
Encoder Adapter cable (m12 to SUB-D 15)	ID 524 599-xx (xx for cable length)
Encoder	ROQ437 safety

For the different tests, some of the equipment are used as described in 表 9. A test setup used for system is shown in 图 5.

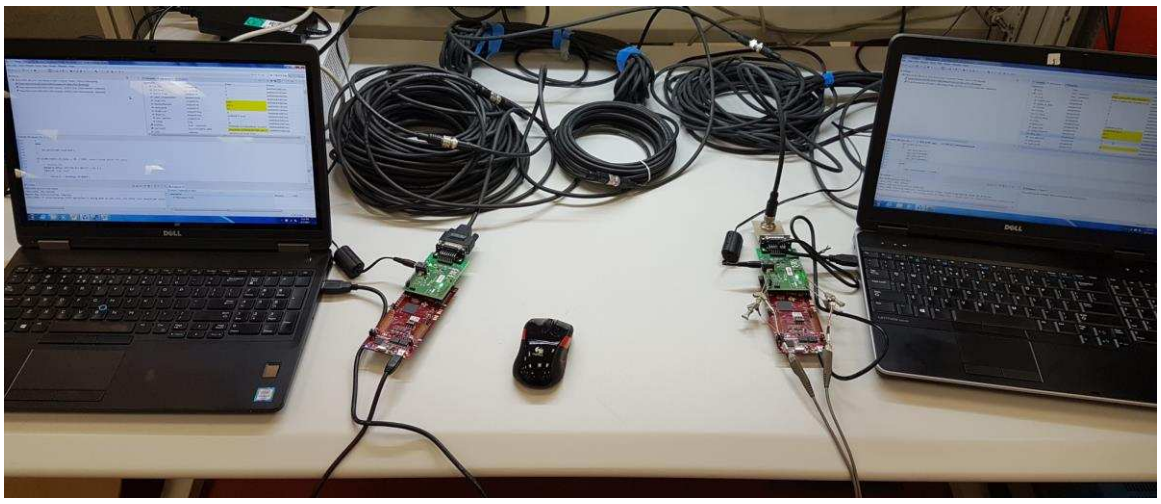


图 5. Picture of Test Setup for System Tests

3.2.2 Test Results

3.2.2.1 Digital Interface

3.2.2.1.1 Signal Tests of THVD1550

Understanding the system specification for the data protocol, it is important to know the system delay of the signal chain. There are two contributors to this delay: the RS-485 transceiver and the level shifter. To measure this system delay, the design board is measured from logic input to differential output for the driver and in the opposite order for the receiver.

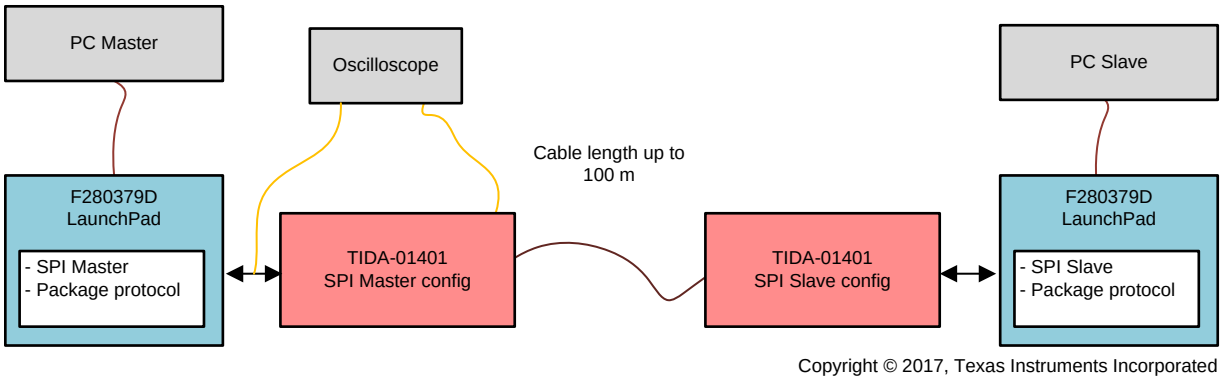


图 **6. Diagram of Test Setup Used for Propagation Delay Measurements**

Here the oscilloscope is connected on the connecter J6 for the differential data and J4 for the single-ended data signal. With this test setup, the following results are achieved.

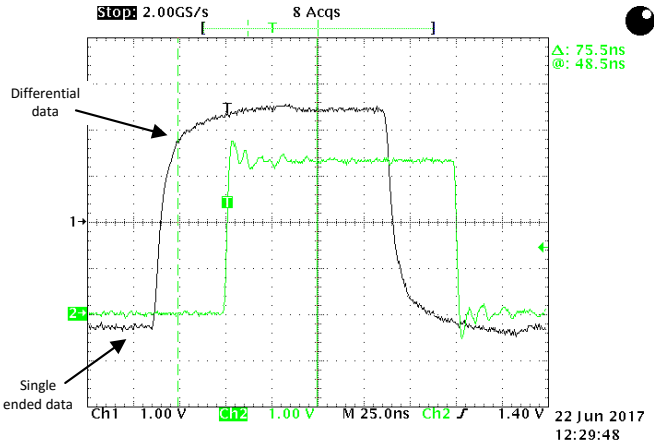


图 **7. THVD1550 Propagation Receiver**

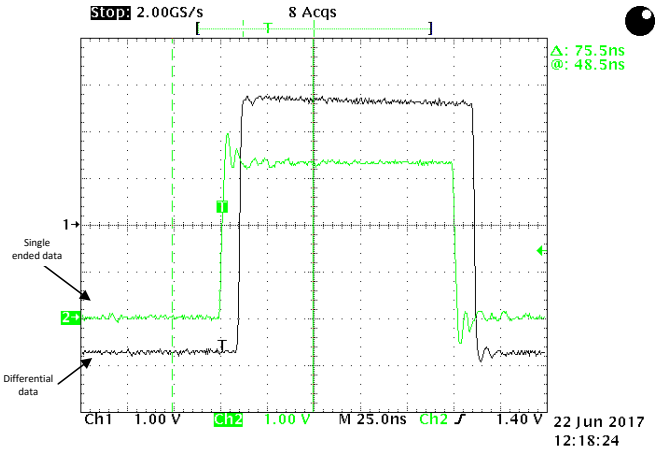


图 **8. THVD1550 Propagation Delay Driver**

There is a different time scale for driver and receiver measurements. The driver propagation delay measured is around 10 ns, and the receiver propagation delay is around 35 ns. The RS-485 master transceiver only contributes to 45 ns to the overall loop delay, which is well below the critical threshold for the configuration without delay compensation.

The propagation delay of the cable also needs to be considered. The cable propagation delay (around 5 m) is already dominant versus the RS-485 transceiver. For an 8-MHz clock frequency, the entire loop delay is approximately 1.1 µs. At an 8-MHz clock, this delay equals nine clock periods. In other words, the data is delayed by 9 bits at the master receiver side.

For more details on the cable delay, see the TIDA-00179 design guide. Considering the cable propagation delay, the delay caused by the design board is very small compared to the cable.

3.2.2.1.2 Eye Diagram of THVD1550

The data and clock signal is measured at a 120-Ω termination at the 30-m and 100-m cables. The measurement done is an eye diagram where an SPI generates a continuous random numbers in a bit pattern.

图 9 shows the test setup.

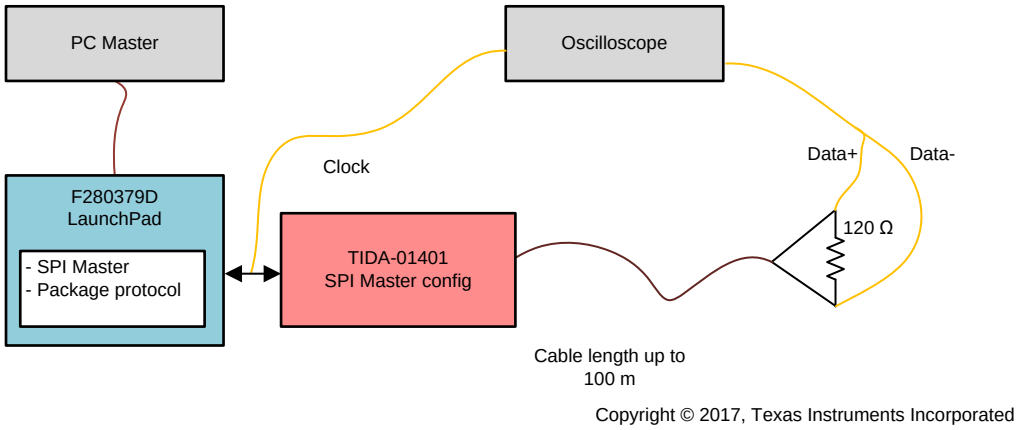


图 9. Diagram of Test Setup Used for Eye Diagram Generation Tests

Here the oscilloscope is connected to the resistor for the differential data and J3 for the single-ended clock signal. The eye diagram test is done for both the 20-m and 100-m cables.

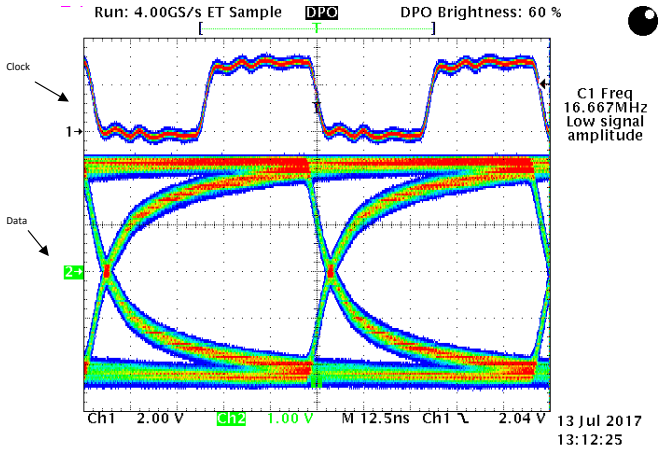


图 10. Eye Diagram of THVD1550 at Master Transmit, 20-m Cable Data Rate 16.66 MHz

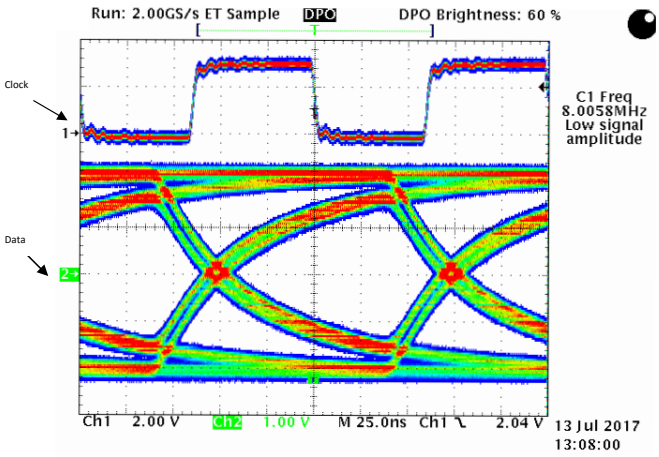


图 11. Eye Diagram of THVD1550 at Master Transmit, 100-m Cable Data Rate 8 MHz

The jitter of the received differential data at the cable with a 120-Ω termination at the maximum EnDat 2.2 clock frequency is around 10% (0.9 UI-open). The steady state differential voltage is around ±2.0 V (4.0 V_{PP}). However, the rise or fall time from 10% to 90% is exactly one clock cycle. Taking into account that the receive data is sampled at the falling clock edge (in the "middle" of the clock cycle), the effective worst case differential voltage is around ±1.0 V. Because EnDat 2.2 specifies the maximum clock frequency based on a 50% duty cycle, the maximum clock frequency needs to be reduced by 10%.

3.2.2.1.3 Bit Error Test per Cable Length

The clock signal is sent from the master to the slave. The data signal is either sent from the master to the slave or reversed. When the data signal is sent from the slave to the master, the delay between the master clock and the slave data needs to be compensated.

During the test, the patterns shipped is two time random noise, a counter and a dummy signal, which can be used for the delay compensation. A test suite is built that can detect clock error, error in the counter signals, and error in the random noise signal.

图 12 shows the test setup.

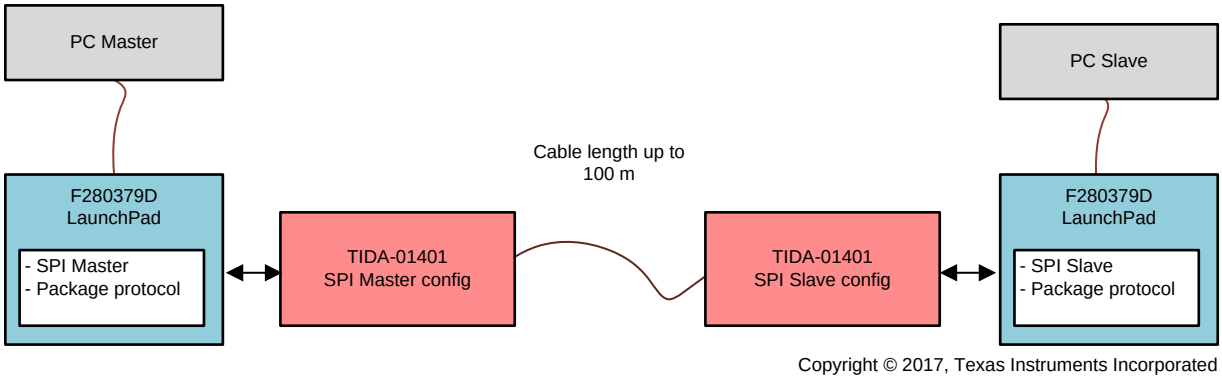


图 12. Diagram of Test Setup Used for Bit Error Generation Tests

图 13 shows the test results.

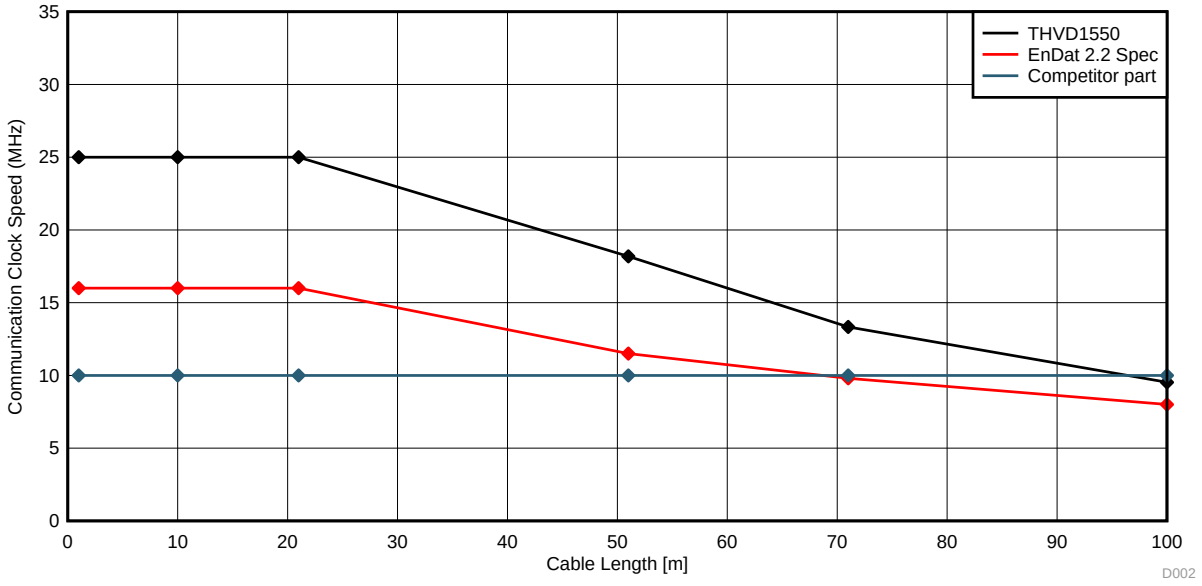


图 13. Test Results for Bit Error Generation Tests Transferring Data From Master to Slave

This test transmits data from the master to the slave and in the reverse order. During these tests, the first clock signal of the data transfer limits the transmission speed; due to this, both directions of the test get the same cable length.

Remember that the SPI clock is limiting the data transmission speed. For synchronous communication, the 25-MHz SPI clock frequency represents a 50-Mbps data transfer as the one clock signal is represented by one digital 0 and one digital 1 of the 50% duty cycle.

3.2.2.2 System Performance

These tests use the interface as an encoder interface. In this case, the EnDat2.2 protocol is used combined with an EnDat encoder. Remember that the EnDat master interface is a known RS-485 transceiver and the EnDat slave (encoder) is an unknown transceiver.

The EnDat protocol is tested at 8.33 MHz because this is the default frequency the LaunchPad will give. This frequency can be changed to 8 MHz by replacing the crystal of the LaunchPad from the 10- to 8-MHz crystal.

3.2.2.2.1 EnDat 2.2 Tests

This test uses the encoder ROQ437. 图 14 shows the test setup. The results of the performance tests can be seen in 图 15.

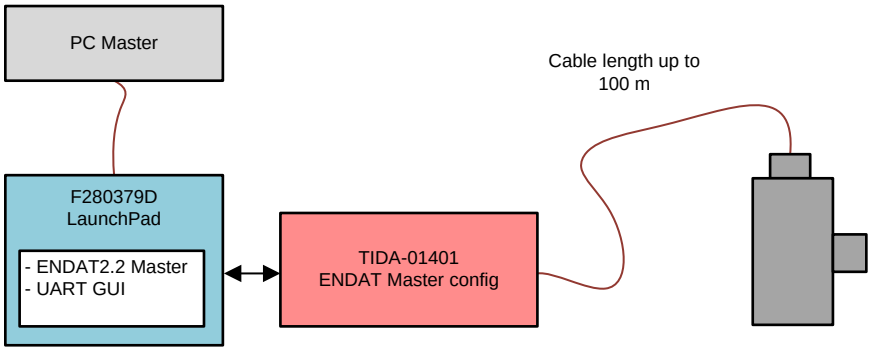


图 14. Diagram of Test Setup Used for System Performance Tests

These results are compared with the EnDat 2.2 cable length standards using two different EnDat 2.2 encoders.

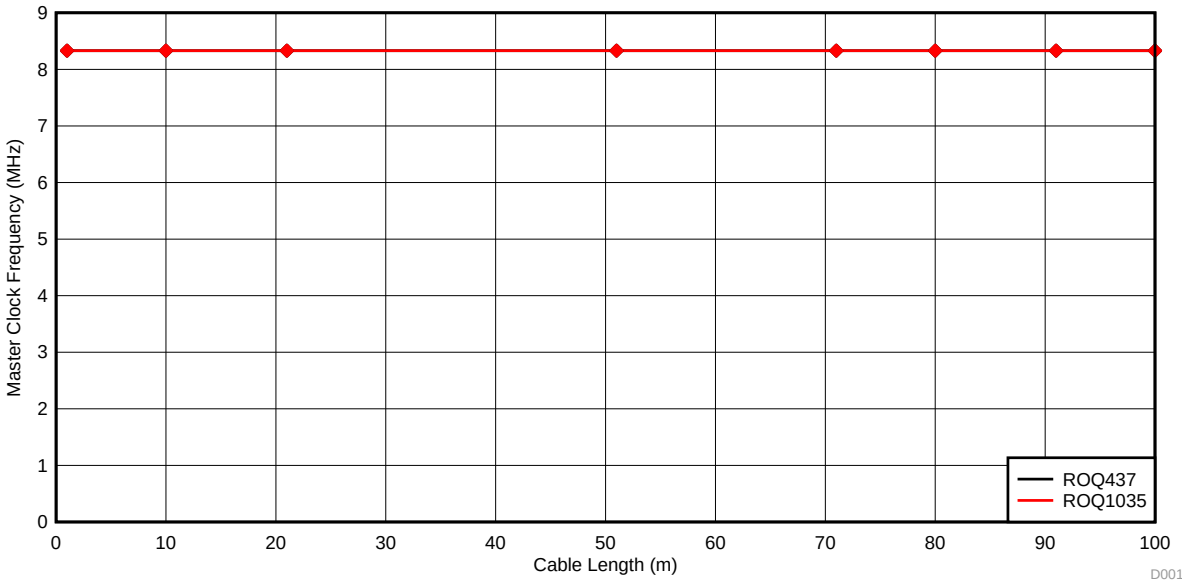


图 15. EnDat 2.2 Cable Length Tests at 8.33 MHz

注: Software works up to 8.33 MHz with the default crystal. For 8 MHz, change the crystal from 10 MHz to 8 MHz.

The solution works for EnDat 2.2 encoders up to 8 MHz. The 16 MHz for the short cables can be done using the hardware and is verified using the test result in 图 13, but the current software solution does not support this option.

With this test, the THVD1550 can run the EnDat 2.2 protocol from 0 up to 100 m as the protocol states.

3.2.2.3 Power Management

For the power management subsystem of the reference design board, the following tests are done:

- Testing the power-up sequence of the power rails
- Testing the power-down sequence
- Testing the current consumption on each power rail

These tests are performed with the test setup as shown in the following test sections.

3.2.2.3.1 Power-up Behavior of Onboard Supply Rails

The oscilloscope is connected on the connecter J6 for the 12-V encoder rail, J3 for the 3v3 rail, and on the 5-V rail of the board by hand.

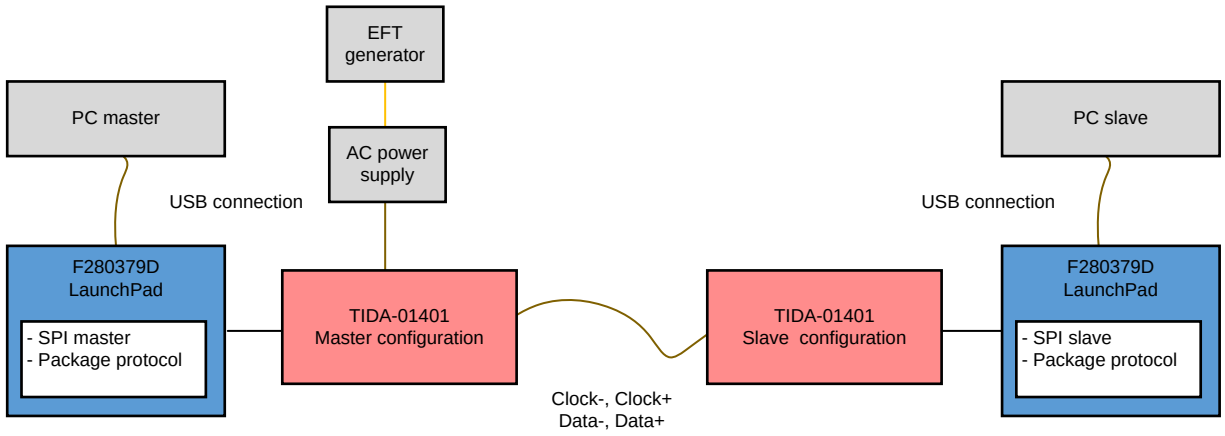


图 16. Diagram of Test Setup for Power Sequence Tests of Reference Design

As expected, the 5-V rail starts after the 3v3 rail is supplied. The 3v3 rail starts as soon as the input gets to 4 V.

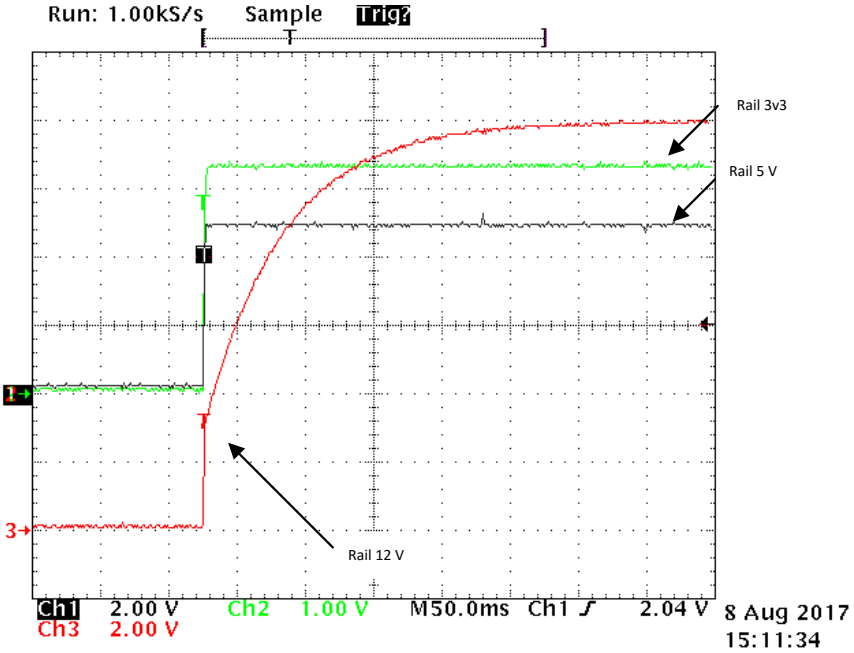


图 17. Power-up Sequence of Reference Design

3.2.2.3.2 *Power-Down Behavior of Onboard Supply*

The test setup is the same as used in 图 16.

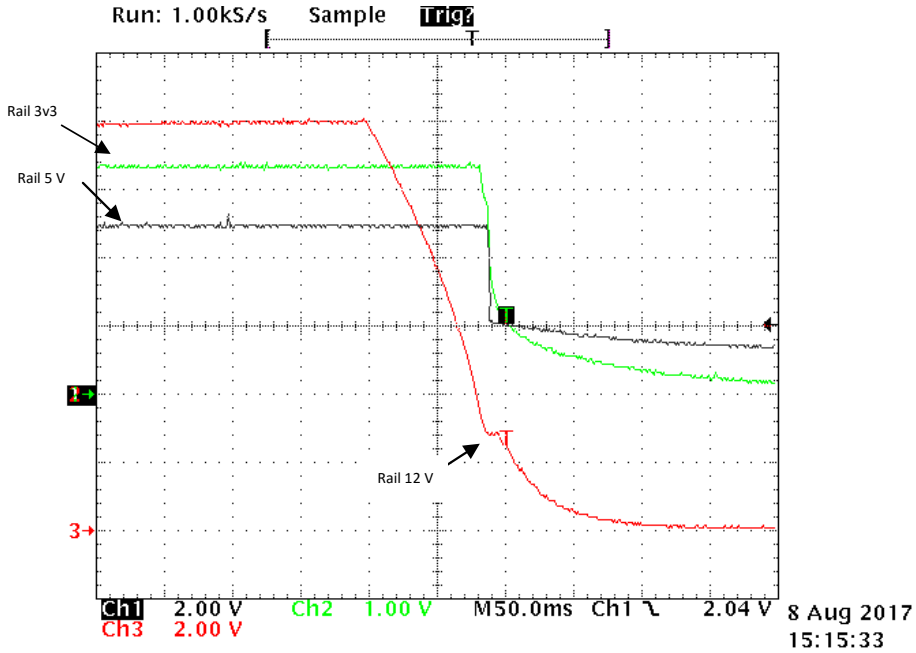


图 **18. Power-Down Sequence of Reference Design**

During power down, the 12-V rail ramps down as V_{IN} is ramping down. This triggers the 3v3 rail to ramp down, turning off the load switch of the 12-V rail. Then the 5-V rail starts ramping down as the 3v3 rail gets below 2.7 V as expected.

3.2.2.3.3 Power Consumption of System

图 19 shows the test setup for power consumption measurement. Here power to the LaunchPad is provided over the USB connection from the PC master.

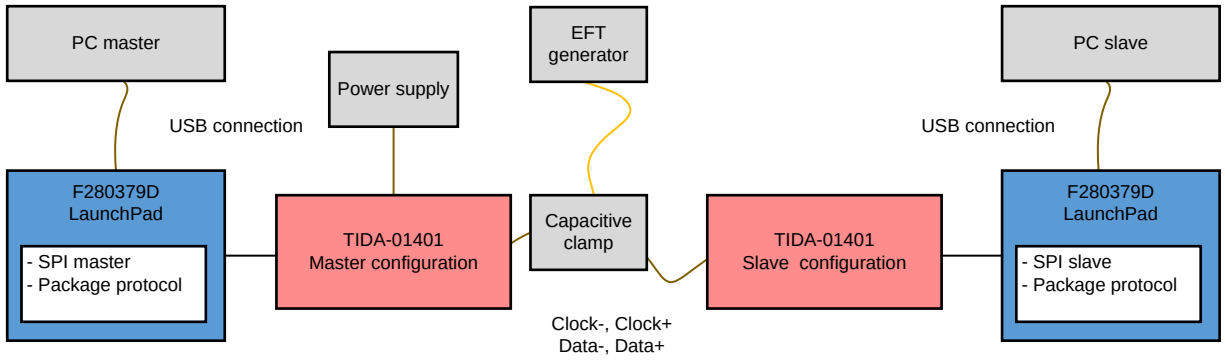


图 **19. Diagram of Test Setup for Power Consumption Tests**

For this measurement, the reference design is modified by disabling the 5-V boost converted, pulling the enable pin to ground, and removing the resistor R2 powering the LaunchPad externally.

表 10. Power Consumption

MEASUREMENT	TASK	5 V	3v3
Current (mA)	Idle	1.36 mA	2.34 mA
Current (mA)	Endat at 8.33 MHz	52.64 mA	2.54 mA

The power consumption is measured with the reference design running an EnDat 2.2 encoder at a 8.33-MHz clock frequency with a 16-kHz update rate.

3.2.2.4 EMC Test Results

For this design, only an EFT test according to the IEC 61800-3 and IEC 61000-4-4 is done due to the high need of passing.

This reference design is tested for IEC 61000-4-4 (EFT) with test levels and performance criterion specified in the standard IEC 61800-3 *EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems* (for more details, see 1.1 节).

The design is compliant to these EFT standards and exceeds the voltage requirements according to IEC 61800-3 EMC immunity requirements. A summary is shown in the following tables, and more details are in the following subsections.

表 11. IEC 618000-3 EMC EFT Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS					TIDA-01401 MEASUREMENTS		
PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION	LEVEL	PERFORMANCE (ACHIEVED) CRITERION	TEST
Ports for control lines and DC auxiliary supplies < 60 V	Fast transient burst (EFT)	IEC 61000-4-4	±2-kV/5-kHz, capacitive clamp	B	±4 kV	B	PASS (EXCEED)
Power port	Fast transient burst (EFT)	IEC 61000-4-4	±2-kV/5-kHz, directly connected	B	±2 kV	B	PASS

The tests are done with the following test setups. The first test setup is done using an encoder to test the EnDat 2.2 slave showing the test setup with the capacitive clamp.

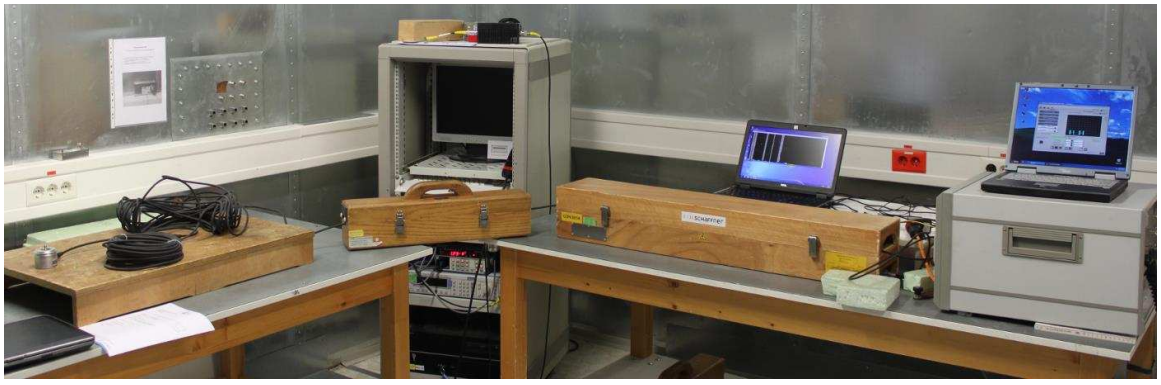


图 20. Picture of Test Setup for EMC Immunity Tests Using Encoder and Capacitive Clamp EFT Connection

The second test setup is done using the same RS-485 transceiver board for both the master and slave in the communication, showing the connection for the power test setup (see 图 21). The software used for the length testing is used to test the data transfer.

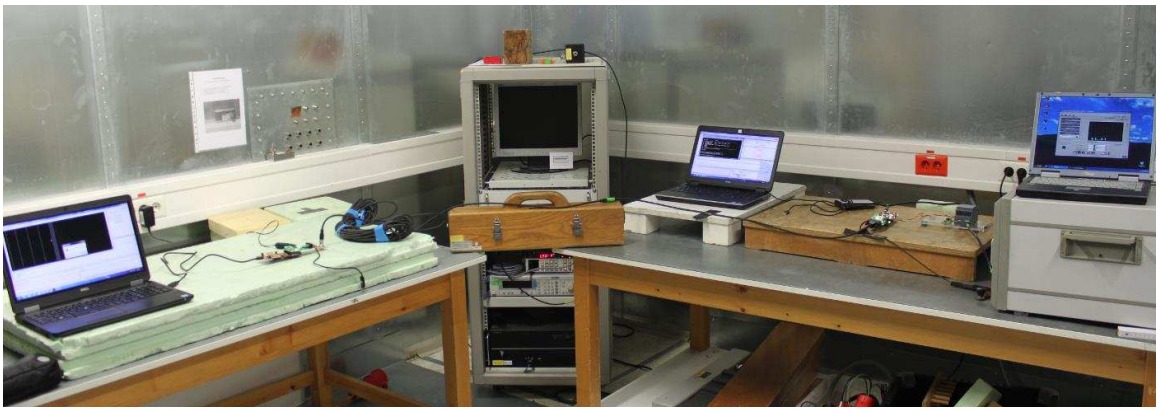


图 21. Picture of Test Setup for EMC Immunity Tests Using Same Transceiver and Direct EFT Connection

Here the software for both test setups is transmitting with a 16-kHz repetition. By transmitting 1,920,000 packets during the two minutes of the test with this value, the packet error rate is calculated.

3.2.2.4.1 EFT immunity Applied on Signal Ports

There are two setups to test the signal port. One setup uses the encoder as a slave as shown in 图 22.

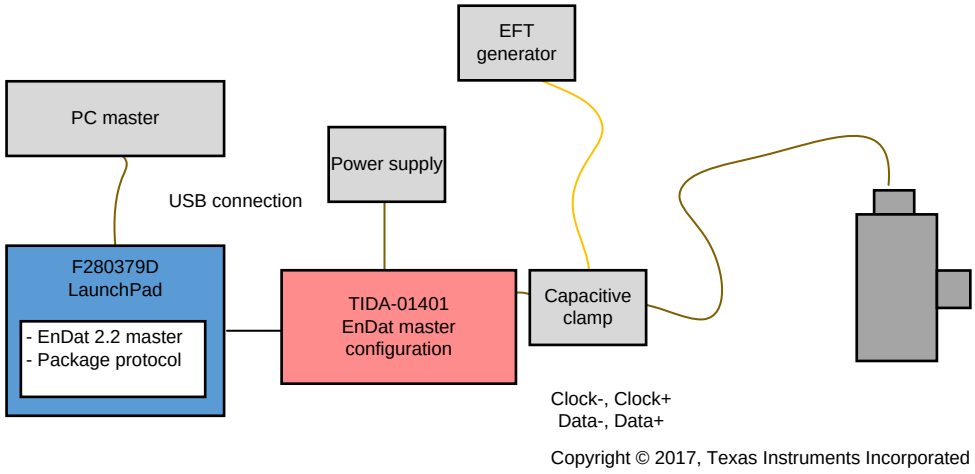


图 22. Diagram of Test Setup for EMC Immunity Tests on Signal Port Using an Encoder

One issue by doing this test is that the encoder is a black box with an unknown RS-485 transceiver. This transceiver can influence the performance of the device under test (DuT).

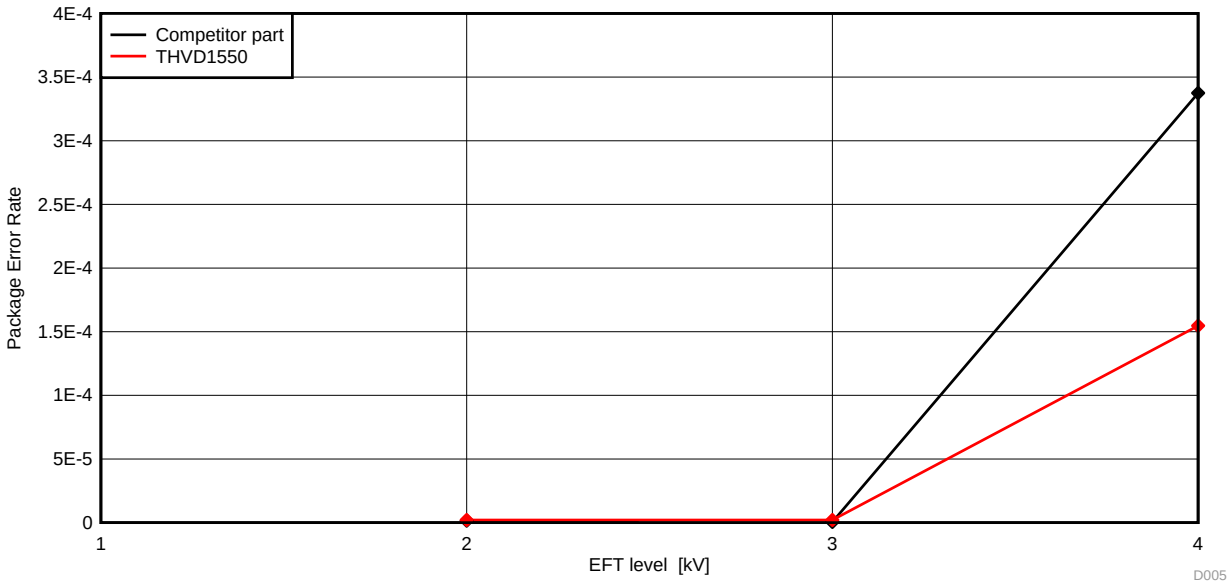


图 23. Test Result of EFT Test Using Encoder With 5 kHz

The system test using the encoder shows that this configuration is not class A, as it shows CRC errors on the communication. What is unknown is if this error comes from the data or the clock signal of the communication and if the error is coming from the master-to-slave transmission or the slave-to-master transmission.

Another thing to see is that the THVD1550 perform about 50% better than other high immunity RS-485 transceivers from completion.

The second test uses a known transmitter on both ends of the transmission, as shown in 图 24.

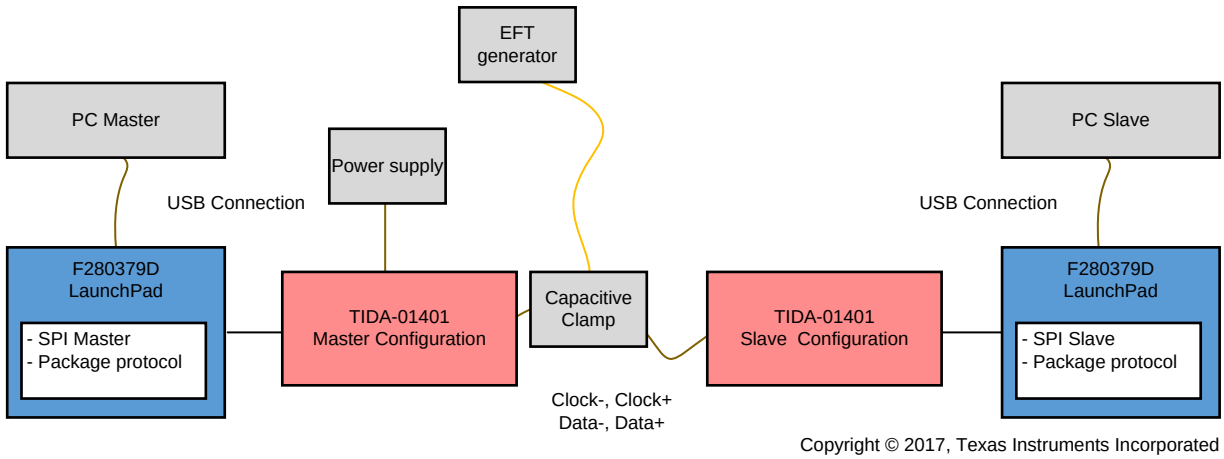


图 24. Diagram of Test Setup for EMC Immunity Tests on Signal Port Using Same Transceiver

Here with EFT on the signal port, the results shown in 图 25 are achieved.

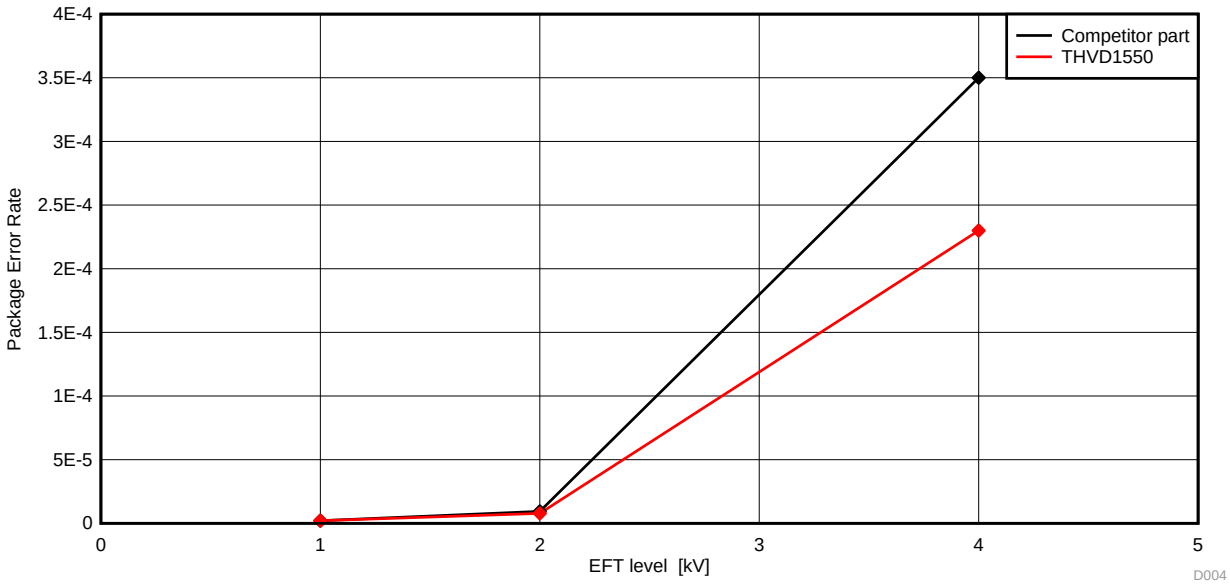


图 25. Test Result of EFT Test Using Same Transceiver on Signal Port With 5-kHz Frequency

3.2.2.4.2 EFT Immunity Applied on Power Ports

This test is done as shown in 图 26.

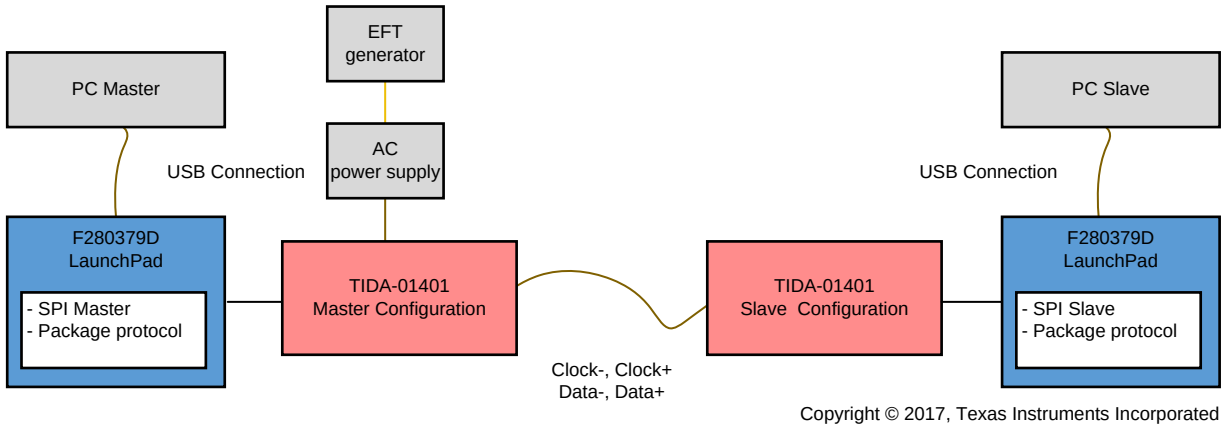


图 26. Diagram of Test Setup for EMC Immunity Tests on Power Port Using Same Transceiver

This test is done by only testing the data communication from the master to the slave. With this configuration, two EFT cases are tested: EFT on the signal port, and EFT on the power port of the system.

The power supply used for the power port EMC test option is a Siemens LOGO!Power 6EP1331-1SH03 generating the 24 V and the LM5010-EVAL evaluation module regulating the 24 V to 10 V.

In the test case with EFT on the power port the following results are achieved (see 图 27).

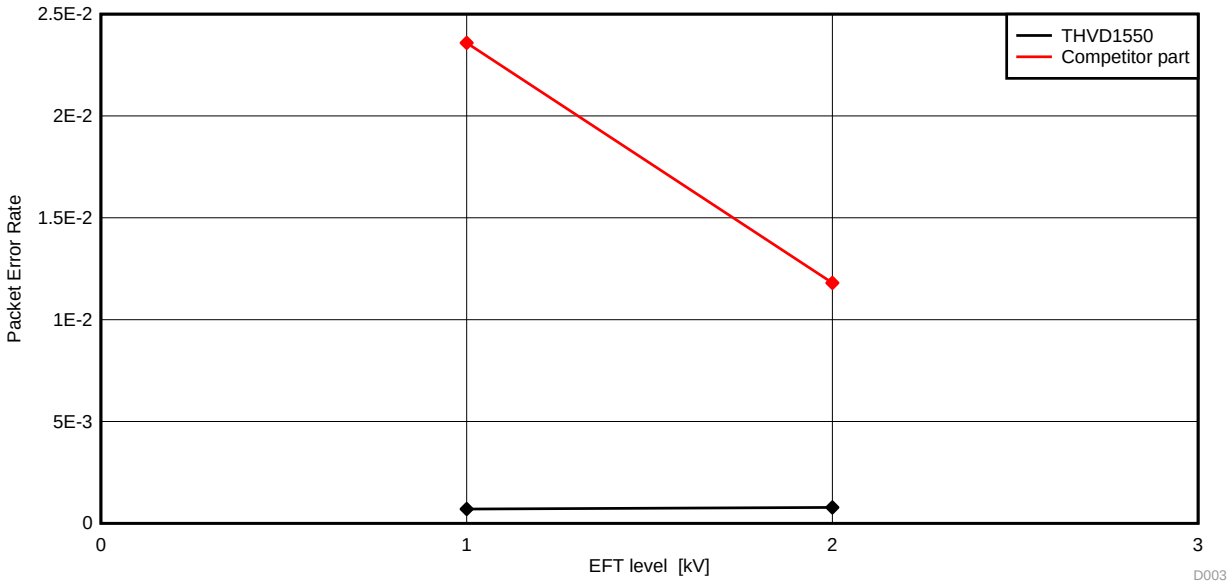


图 27. Test Result of EFT Test Using Same Transceiver on Power Port With 5-kHz Frequency

With this test, the THVD1550 works with fewer data errors during the EFT test than the leading competitor's part.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01401.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01401.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01401.

4.3.2 Layout Guidelines

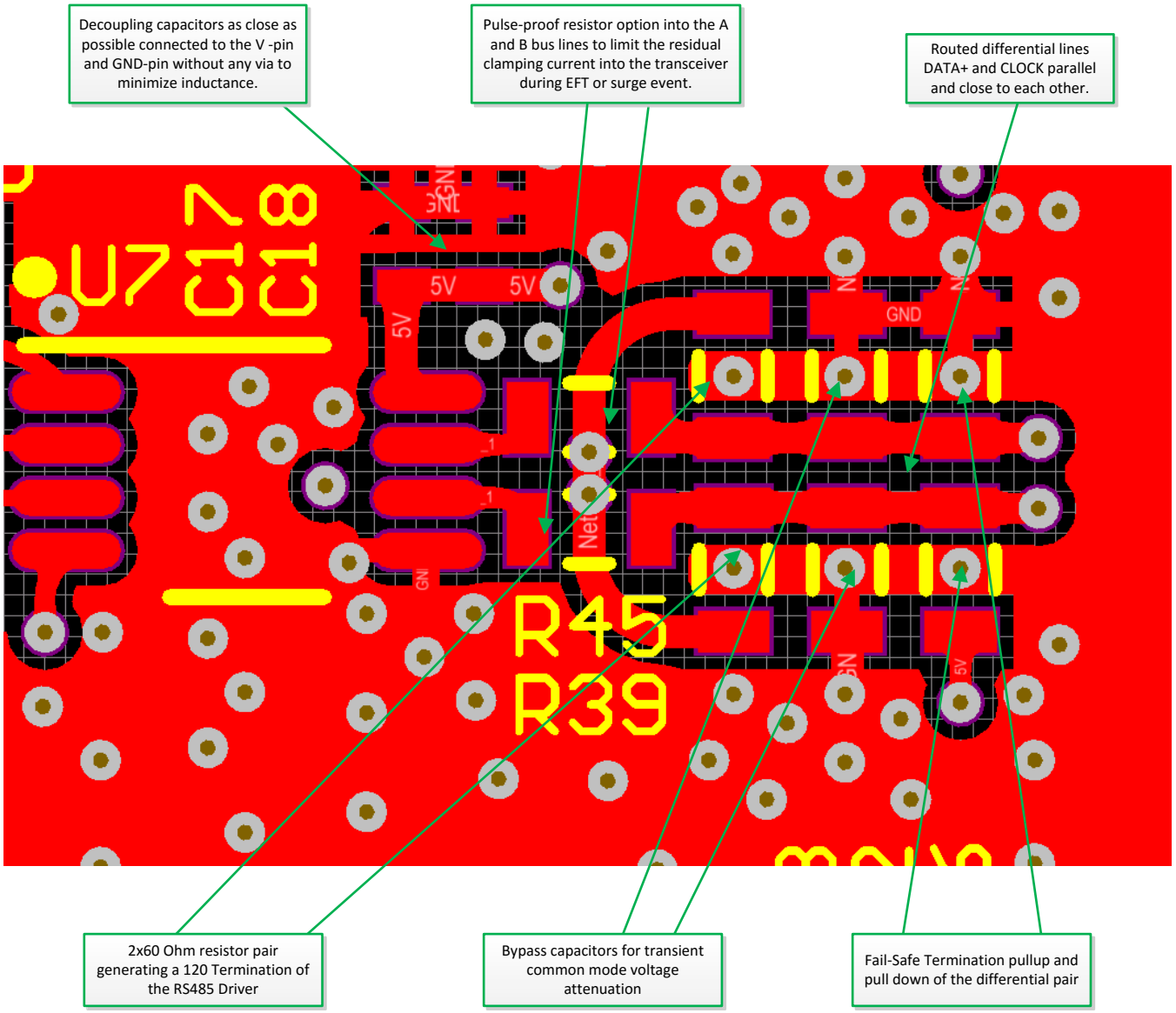


图 28. Transceiver Layout Guidelines

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01401.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01401.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01401.

5 Software Files

To download the software files, see the design files at TIDA-01401.

6 Related Documentation

1. Texas Instruments, *Universal Digital Interface to Absolute Position Encoders*, TIDA-00179 Design Guide (TIDUAN5)
2. Texas Instruments, *C2000™ Position Manager EnDat22 Library Module*, User's Guide (SPRUI35)
3. Texas Instruments, *Using Position Manager EnDat22 Library on IDDK Hardware*, User's Guide (SPRUI34)

6.1 商标

7 Terminology

EFT— Electrical fast transient

8 About the Authors

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